Electrical overstress failure in GaAs MESFET structures

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ELECTRICAL OVERSTRESS FAILURE
IN
GaAs MESFET STRUCTURES

by

Andrew John Franklin B.Sc. (Hons.), DIS

A DOCTORAL THESIS

Submitted in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy of Loughborough University of Technology.

1st March 1990.

How many roads must a man walk down  
Before you call him a man?  
Yes 'n' how many seas must the white dove sail  
Before she sleeps in the sand?  
Yes 'n' how many times must the cannon balls fly  
Before they're forever banned?  
The answer my friend, is blowin' in the wind  
The answer is blowin' in the wind.

ABSTRACT

An experimental and theoretical analysis has been carried out into the effects of electrostatic discharge and constant power electrical overstress in GaAs MES structures.

An experimental system has been set up to measure the electrical and physical characteristics of such devices when subject to electrical overstress. This system includes computer controlled equipment to analyse the electrical failure waveforms.

The results from the experimental study have been analysed to establish any patterns which characterise ESD breakdown. Using a new thermal breakdown model, analytical predictions of the power required to degrade these devices, for both constant power, and electrostatic discharge breakdown, have been carried out.
ACKNOWLEDGEMENTS

I owe my thanks to my colleagues in the Electronic Component Technology Group at Loughborough University for the many illuminating discussions. In particular I wish to thank my supervisor Professor David Campbell for his willingness to discuss this research and for his tremendous moral support over the past five years. I am indebted Dr. Vince Dwyer whose mathematical wizardry contributed significantly to the development of the thermal models presented in this thesis. Bill Young, formally of STC Components Group, who offered to original contract to the University back in 1984.

STC Technology Ltd and STC Paignton provided the wafers used in this study and my thanks to them, particularly Dr. Steve Bland and Dr. Richard Butlin who provided invaluable support during the early years of this work.

Over the past two and a half years the project has been sponsored by the Procurement Executive, Ministry of Defence I am grateful to them for the continued support. I would particularly like to thank Dr. John Woodward of RSRE for his valuable input on this and many related subjects.

During the course of my time at Loughborough there have been many people who have helped in some manner. I wish to thank Ajith, Tim von Ireland, Neil, Martin, Farzin, Jeff, Danny, Roger, Joe and many other friends for their encouragement and support over the past five years.

Finally, I would like to thank my mother and father for keeping me in touch with the "real world" and a special thanks to Nikki for being my constant companion during much of my time in Loughborough.
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</tr>
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<td>Cd</td>
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<td>HJBT</td>
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<td>I</td>
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<td>Indium Arsenide</td>
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<tr>
<td>InP</td>
<td>Indium Phosphide</td>
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<td>I₀</td>
<td>Peak Current</td>
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<tr>
<td>J</td>
<td>Current Density</td>
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<td>Jᵉ</td>
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<td>k</td>
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<td>kV</td>
<td>Kilovolts</td>
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<td>L</td>
<td>Contact Spacing</td>
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<td>LEC</td>
<td>Liquid Encapsulated Czochralski Growth Technique</td>
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<td>Lₜ</td>
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<td>MBE</td>
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<td>mₑₑ</td>
<td>Density of State for Electrons in Conduction Band</td>
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<td>mₑ₉</td>
<td>Density of State for Electrons in Valence Band</td>
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<tr>
<td>Mₑ</td>
<td>Number of Equivalent Minima in the Conduction Band</td>
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<td>MES</td>
<td>Metal-Semiconductor</td>
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<tr>
<td>Mg</td>
<td>Magnesium</td>
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<tr>
<td>mₑ</td>
<td>Electron Mass</td>
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<td>MOCVD</td>
<td>Metal Organic Chemical Vapour Deposition</td>
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<td>MTTF</td>
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<td>Nₐ</td>
<td>Acceptor Doping Level</td>
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<td>Nₑ</td>
<td>Donor Doping Level</td>
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<td>NDR</td>
<td>Negative Differential Resistance</td>
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<td>nₖ</td>
<td>Ideality Factor</td>
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<td>Positive Differential Resistance</td>
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<td>Contact Resistance</td>
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<td>R₉ₑₑ</td>
<td>Channel Resistance</td>
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<tr>
<td>Rₑₑₑ</td>
<td>Drain Resistance</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
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</table>
\( R_m \)  
Measured Resistance

\( R_s \)  
Source Resistance

\( R_{ac} \)  
Sheet Resistance Under Ohmic Contact

\( R_{sh} \)  
Sheet Resistance Between Ohmic Contacts

\( R(t) \)  
Reliability of a Component

\( S \)  
Defect Surface Area / Sulphur

\( s \)  
Seconds

\( Se \)  
Selenium

\( Si \)  
Silicon

\( S.I. \)  
Semi-Insulating

\( Si_3N_4 \)  
Silicon Nitride

\( SiO_2 \)  
Silicon Dioxide

\( T \)  
Temperature

\( t \)  
Time

\( T_o/T_a \)  
Ambient Temperature

\( t_{tr}, t_{b}, t_c \)  
Characteristic Diffusion Times

\( T_c \)  
Critical Temperature

\( t_f \)  
Failure Time

\( Te \)  
Tellurium

\( Ti \)  
Titanium

\( t_L \)  
Lower Failure Time

\( t_f^0 \)  
Time Intercept from the \( \log P_t \) vs \( t_f \) plot - Region III

\( t_{f}, t_{f} \)  
Failure Time for a Time Varying Pulse

\( T_{ss} \)  
Steady State Temperature

\( t_U \)  
Upper Failure Time

\( V \)  
Volts \ Group 5 Element

\( V_{bi} \)  
Diode Built-In Voltage

\( V_{br} \)  
Gate Reverse Breakdown Voltage

\( V_{ds} \)  
Drain-Source Voltage

\( V_{gs} \)  
Gate-Source Voltage

\( V_o \)  
ESD Charge Voltage

\( V_p \)  
Pinch-off Voltage

\( VPE \)  
Vapour Phase Epitaxy

\( v_e \)  
Electron Velocity

\( V_{sb} \)  
ESD Plateau Voltage

\( v_{sat} \)  
Saturation Velocity of Electrons

\( V_{th} \)  
Threshold Voltage

\( W \)  
Contact Width

\( W_g \)  
Gate Width

\( x \)  
Depletion Depth

\( x_o \)  
0.92413 - The Dawson Integral Turning Point

\( Zn \)  
Zinc

\( Z(t) \)  
Failure Rate

\( \alpha \)  
Bandgap Universal Function Constant

\( \beta \)  
Bandgap Universal Function Constant

\( \delta \)  
Slope of the \( 1/P_t \) vs \( \log t_f \) - Region III

\( \Delta \)  
Defect Volume

\( \epsilon_o \)  
Permittivity of Free Space - 8.854x10^{-12} \ Fcm^{-1}

\( \epsilon_r \)  
Relative Permittivity of GaAs = 13.1

\( \phi_b \)  
Barrier Height

(xi)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
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<tbody>
<tr>
<td>$R_{sh}$</td>
<td>Sheet Resistance Between Ohmic Contacts</td>
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<td>$\infty$</td>
<td>Infinity</td>
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<tr>
<td>$\lambda$</td>
<td>Failure Constant</td>
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<td>$\Omega$</td>
<td>Ohms</td>
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<tr>
<td>$\pi$</td>
<td>3.142</td>
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<td>$\rho$</td>
<td>Resistivity\Density</td>
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<td>$\sigma$</td>
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<td>$\mu$</td>
<td>$10^{-6}$</td>
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<tr>
<td>$\mu_h$</td>
<td>Electron Hall Mobility</td>
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<tr>
<td>$&lt;100&gt;$</td>
<td>Crystal Growth Direction</td>
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</table>
CHAPTER 1

INTRODUCTION

1.1 Historical Background

The origins of research into semiconducting materials can be traced back to the year of 1833[1] when Michael Faraday first investigated the properties of silver sulfide and found that it had a negative temperature coefficient of resistance[2]. Other conductors known at the time, all had resistances which increased with temperature. The next significant discovery was in 1874 when Braun found that the resistance of contacts between certain metals did not obey ohms law, and depended on the magnitude and the polarity of the applied voltage[3]. Schuster(1874) made the same discovery for contacts between tarnished and untarnished copper wires[4].

It was not until the 1930s and the advent of quantum mechanical analysis of atomic structures that a real understanding of the electronic processes in semiconducting materials began to evolve. The development of solid state physics based on the concepts of energy levels with one electron per level, electron spin, the Pauli exclusion principle, and Fermi-Dirac statistics, enabled the understanding of the behaviour of electrons, atoms and molecules to be greatly enhanced. Sommerfield[5] presented a free-electron model of metallic conduction based on quantum mechanics in 1928[6]. His quantum mechanical model of a solid semiconductor showed that the movement of electrons as waves throughout the solid set up interference patterns. Hence, certain energy levels were excluded(forbidden), leading to the concept of energy bands in solids.

In 1925, the first known transistor was designed by Lillienfield who filed patents for it in Canada and the USA[7,8]. Current flow was between two gold electrodes, through a copper sulfide channel and was controlled by a applying a
potential on a third electrode (aluminium). The principle is similar to that of the
MESFET (metal-semiconductor FET) so common today. He later filed for a
patent in 1928 for an improved FET design based on the insulated gate
electrode, as in the MOSFET (metal-oxide semiconductor FET). He used
Aluminium oxide as the insulator with copper sulfide again being used as the
semiconducting material. In 1928, Lillienfield also patented a metal-base bipolar
transistor which consisted of several layers of metals and semiconductors with
rectifying properties.

Shockley, Bardeen and Brattain, in 1947, constructed the first operational
transistor. It was a bipolar device based on germanium and was known as the
point contact transistor. They also made a vast contribution to the development
of the present theoretical understanding of semiconductors[9-12].

Theoretically, the FET was still the most logical structure to form an
amplifying device. Experimentally it was impossible to obtain efficient devices,
and the measured gain was far below that which was predicted. It was not until
the importance of surface energy states was realised that any workable FET was
constructed and described by Shockley in 1952[13]. Majority carriers formed the
current in those early devices, making them unipolar transistors.

Insulated gate transistors (IGFETs) had to wait until the advances in
semiconductor processing allowed controlled growth of passivation layers,
specifically SiO₂, in 1959. The first metal oxide semiconductor FET (MOSFET)
was proposed by Kahng and Atalla in 1960[7]. Hofstein and Heiman, in the early
1960’s further developed this device to include enhancement and depletion mode
transistors, capable of operating with different polarity gate voltages[14]

1.2 Semiconductor Devices into the 21st Century

The shrinking of semiconductor devices has been one of the greatest
advances in technology of recent times. Very Large Scale Integration (VLSI) has
made it possible to fabricate large numbers of active devices into very small
areas of the base semiconductor. Today, commercially available VLSI circuits in
Silicon can have >800 devices per mm². Such circuits are capable of performing
a host of complex functions, ranging from high speed computation to automated
control systems.

Research in semiconductors is still concentrating on making the transistor even smaller[15-18]. The reasons behind this are basically economic. The cost of the semiconductor itself makes up the major portion of a manufacturers budget, so it stands to reason that, by increasing the density of transistors on the base substrate, the overall device becomes more cost effective. Large packing densities, as found in VLSI circuits, have the added advantage of enabling complex circuitry to be designed with the minimum of external connections. Internal connections are more reliable and hence VLSI design can increase the reliability of complex circuits.

Recently, a great deal of attention has been focused on the III/V group of elements in the periodic table. With the advances in epitaxial and growth techniques, semiconductors such as GaAs, InP, InAs, AlAs, etc are readily grown. The most widely used of these III/V semiconducting materials is GaAs[19] which has certain properties, in particular the high electron mobility, which make it more suitable for switching systems and high frequency amplification than silicon. Improvements in modern fabrication techniques has allowed very complex integrated circuit structures and novel transistor structures to be realised from this material. But, in order for these new devices to become a commercial success, they must be relatively cheap and at least as reliable as their Silicon counterparts. Thus, any new device must undergo extensive reliability testing in order to the improve the device structure/fabrication techniques, to allow these devices to achieve maximum reliability.

1.3 Study Synopsis

The study presented in this thesis relates to electrically induced breakdown in GaAs MES devices. An experimental study is presented which assesses the EOS and ESD degradation and burnout thresholds in GaAs MES structures.

A theoretical analysis of the conditions required for thermal breakdown in such structures is presented for constant power electrical overstress (EOS), and electrostatic discharge stress (ESD). These models have been investigated
experimentally and conclusions have been drawn as to the validity of these models for the GaAs MES structures.

The thesis has been broken down into 9 Chapters, a brief explanation of each chapter is described below.

Chapter 1 - This chapter contains a brief history of semiconductor devices. It also contains the study synopsis and chapter breakdown.

Chapters 2/3 - These provide the background for the thesis. Chapter 2 provides a review of some GaAs properties and its use in field effect transistors. Chapter 3 discusses reliability analysis techniques and presents much of the existing reliability literature available for GaAs MESFETs.

Chapter 4 - This chapter describes the measurement apparatus and experiments undertaken to assess the ESD sensitivity of GaAs MES devices.

Chapter 5 - This chapter contains the results from the experimental study.

Chapter 6 - This chapter discusses the experimental results and proposes the possible failure mechanisms operating in these devices.

Chapter 7 - This chapter describes the thermal breakdown models derived as part of this study to predict the thermal runaway characteristics in all semiconductor devices. Analytic equations are presented which predict the constant power overstress (EOS) threshold, and the electrostatic discharge (ESD) threshold for GaAs metal-semiconductor (MES) devices. A further experimental study is described to verify these thermal breakdown models.

Chapter 8 - This chapter describes the development of a PSPICE circuit model to characterise the ESD pulsing apparatus and to assess the forward breakdown characteristics of GaAs MES Diodes.
Chapter 9 - This chapter draws the conclusions for the complete study and describes a future programme in order to improve the models presented in this thesis and to quantify many of the effects discovered during the course of the study.

1.4 References


CHAPTER 2

GALLIUM ARSENIDE

2.1 Introduction

The basic crystallographic and electronic properties of GaAs and its use in metal-semiconductor (MES) devices are outlined in this chapter. Due to the nature of the study undertaken in this thesis, special emphasis on the effects of temperature and high electric fields on the electronic conduction properties are discussed. The reader is referred to reference [1], for a more comprehensive review of the crystallographic, electrical, and thermal properties of GaAs.

2.2 Crystal Structure

The crystal structure of GaAs[2] is composed of two sublattices, each of which is a face-centred cubic (fcc). This fcc structure, and the unit cube for the GaAs lattice are shown in figs. (2.1) and (2.2). The GaAs fcc structure consists of atoms at the corners of the cube and also at the centre of each face of the cube. The Ga sublattice is arranged in the same fashion as the As sublattice. These two sublattices are offset with respect to each other by half the diagonal of the fcc cube. Such a crystal configuration is called the cubic phalorrate or zincblende, and has fcc translational symmetry.
Fig. (2.1) GaAs Face Centred Cubic (fcc) Structure

Fig. (2.2) Unit Cube of the GaAs Crystal Lattice
2.3 Band Structure

An analysis of the energy band structure can explain why materials have insulating, conducting or semiconducting properties. Any single atom has a series of discrete energy levels associated with its electron cloud. These energy levels dictate the effective energy of electrons contained within this level. Theory predicts[3] that an electron can adopt an energy which matches any level, but cannot adopt an energy between the levels. If a material is formed many atoms become very close to each other, the number of discrete levels becomes very large, and broaden into a series of bands. For the characterisation of materials these bands are separated into two types, the valence band and the conduction band. The valence band consists of the lowest electron energy levels in which electrons cannot be used for conduction. The conduction band is the lowest energy, and above, which electrons can be used for conduction. The energy difference between these levels is termed the forbidden or bandgap. In insulators, the energy difference between the valence band and the conduction band is very large, thus accounting for its insulating properties. In a metal, the conduction band and the valence band overlap thus allowing easy conduction. In the most common semiconductors the forbidden band is of the order of 1eV, which is small enough to allow stimulated electrons to traverse the forbidden gap and thus be used for conduction. Stimulation of electrons from the valence band to the conduction band in a semiconductor can be achieved by heating[4], electron injection[5], and photon stimulation[6].

At room temperature and under normal atmospheric conditions the value of the band gap for intrinsic GaAs is 1.42eV[7]. This value has been shown to decrease with temperature[8], according to the universal function:

\[ E_g(T) = E_g(0) - \alpha T^2/(T+\beta) \]  

(2.1)

where \( E_g(0) \) is the bandgap at absolute zero, 1.519eV  
\( \alpha \) is 5.405x10^{-4} eV K^{-1}  
\( \beta \) is 204 K

Fig. (2.3) shows this variation with temperature in GaAs.
The carrier density ($n_i$) per cm$^3$ within an intrinsic semiconductor is related to $E_g$ by the equation[9]:

$$n_i = 4.9 \times 10^{15} (m_{de} m_{th}/m_o)^{0.75} M_e^{0.5} T^{1.5} \exp(-E_g/2kT)$$  (2.2)

where

- $m_{de}$ is the density-of-state effective mass of the valence band.
- $m_{th}$ is the density-of-state effective mass for electrons.
- $m_o$ is the free electron mass.
- $M_e$ is the number of equivalent minima in the conduction band.
- $T$ is the absolute temperature.
- $E_g$ is the bandgap energy in eV.
- $k$ is Boltzmann's constant.

and consequently the numbers of electrons in the conduction band and holes in the valence band will increase with temperature. This is an important result if the semiconductor is heated to well above its normal operating temperature.

The modelling of band structures, and the excitation of electrons from the valence band to the conduction band is complex and involves calculations of both the energy and momentum. GaAs is a direct bandgap material, in contrast to Si, which means electrons require no change in momentum when sufficient energy is given for transference to the minimum energy characteristic of the conduction band. This makes GaAs an efficient material for the simulated emission of photons, and hence can be used for optoelectronic devices such as lasers and light emitting diodes[10,11].

### 2.4 Electronic Transport

#### 2.4.1 Donor and Acceptor Impurities

The technique of impurity doping can be used to create energy levels acceptor impurities[12]. The introduction of Si, Se, S or Te atoms within the
Fig. (2.3) GaAs Bandgap Variation vs Temperature[8]

![Graph showing GaAs Bandgap Variation vs Temperature](image)

\[ Eg(0) = 1.519 \text{ eV} \]
\[ \alpha = 5.405 \times 10^{-4} \]
\[ \beta = 204 \]

Fig. (2.4) Carrier Density vs Temperature for Doped GaAs[9]

![Graph showing Carrier Density vs Temperature](image)

\[ n_i = 10^{17} \text{ cm}^{-3} \]
\[ n_i = 10^{13} \text{ cm}^{-3} \]
GaAs[13] creates an electron levels just below the conduction band minimum by residing on vacant Ga sites. These electrons are thermally excited into the conduction band at room temperature, thus allowing a controlled number of electrons to be used for conduction. Semiconductors which have been doped in this way are termed n-type. The higher the doping density, in general, the higher the conductivity. Conversely the introduction of Mg, Be, Zn, or Cd in GaAs create an acceptor level, which is an energy level void of electrons (termed holes) which also can be used for conduction. In a large number of GaAs devices, including the devices used in this study, the conducting region is created by the introduction of a donor level using ion-implanted Si[13].

The introduction of donor impurities within a semiconductor changes the local carrier concentration within the doped layer of the material. This doping, after activation, yields carrier densities in GaAs of the order of $10^{15}$ to $10^{18}$ carriers cm$^{-3}$ at room temperature. The semi-insulating region beneath the active layer has an intrinsic carrier density in the order of $10^{13}$ carriers cm$^{-3}$. Hence, by the introduction of donor impurities, a high conduction region has been created while the rest of the material remains in a semi-insulating form.

It has been shown that the carrier density in semiconductors is fairly stable with temperature until the point where the intrinsic carrier density equals the doping density[14,15]. At this point the carrier density follows the intrinsic curve to well above 1000 K. The predicted carrier density vs temperature relationship for GaAs with n-type doping of $10^{17}$ carriers cm$^{-3}$ and the semi-insulating form are shown in fig. (2.4).

**2.4.2 Mobility**

If an external potential is applied to a n-doped semiconductor the free electrons in the conduction band are subject to a force which allows them to move through the crystal and giving rise to a drift current. At low electric fields the drift velocity is proportional to the field and is the proportionality constant is defined as the mobility $\mu$. The basic equation which models the drift velocity is:

$$v_s = \mu_n E$$

(2.3)
where $v_d$ is the drift velocity
$\mu_n$ is the electron mobility in cm$^2$ (V-s)$^{-1}$
$E$ is the electric field.

At high electric fields the mobility and hence the drift velocity becomes non linear[16]. This effect is demonstrated in fig. (2.5) which shows the electron drift velocity as a function of applied field for intrinsic GaAs at 300 K, as calculated using a time-of-flight and microwave technique[17,18]. The graph shows that the drift velocity, $v_d$, reaches a maximum of $\approx 2 \times 10^7$ cm s$^{-1}$ at around 3.5 kV cm$^{-1}$, and then decreases as the field continues to rise. At high enough fields the velocity tends to a constant value of $\approx 1 \times 10^7$ cm s$^{-1}$.

Fig. (2.6) shows the electron mobility, at varying doping densities, increasing with temperature. This experimental data was obtained using a technique based on the Hall effect[16]. The graph shows that the Hall mobility rises to a maximum value of $\approx 3 \times 10^5$ cm$^2$ (V-s)$^{-1}$ at 70 K and then decreases with temperature. From a consensus of experimental results[19] the empirical equation which describes the decrease in the Hall mobility from 100 K to 1000 K is given by:

$$\mu_h = 400(300/T)^{2.3}$$

(2.4)

where $\mu_h$ is the Hall mobility
$T$ is the absolute temperature

### 2.4.3 Resistivity

The resistivity $\rho$ is defined as the proportionality constant between the electric field $E$, and the current density $J$. The equation which models the resistivity is given by:

$$E = \rho J$$

(2.5)

Its reciprocal value is the conductivity, $\sigma$, and hence:

$$J = \sigma E$$

(2.6)

where $E$ is the electrical field
$J$ is the current density
$\rho$ is the resistivity
$\sigma$ is the conductivity
Fig. (2.5) GaAs Electron Drift Velocity at 300K
Dashed line - Time of Flight Technique
Dash-Dotted Line - Microwave technique
Continuous Line + Data - See Ref. [17,18]

Fig. (2.6) GaAs Hall Mobility vs Temperature
Full circles - \( N_d = 4.61 \times 10^{13} \) cm\(^{-3}\), \( N_n = 3.66 \times 10^{13} \) cm\(^{-3}\)
Triangles - \( N_d = 1.91 \times 10^{13} \) cm\(^{-3}\), \( N_n = 2.61 \times 10^{13} \) cm\(^{-3}\)
Curves - Theoretical, see ref. [17,18]
In n-doped semiconductors, as in the majority of GaAs devices, electrons are the dominant carriers the resistivity can be shown to be:

\[ \rho = \frac{1}{(nq\mu_h)} \]  \hspace{1cm} (2.7)

where

- \( n \) is the carrier density
- \( q = 1.602 \times 10^{-19} \text{ C} \)
- \( \mu_h \) is the electron Hall mobility

Combining equations (2.2), (2.4) and (2.7) and fixing the doping density at \( 10^{17} \) per cm\(^3\), until the intrinsic curve passes this value, the approximate resistivity as a function of temperature can be plotted for GaAs. This is shown in fig. (2.7) and in fig. (2.8) is a similar plot for Si. From the results it is clear that the resistivity increases with temperature until an intrinsic temperature is reached after which it decreases rapidly as the temperature continues to increase. This behaviour is due to the changes of the dependence in the resistivity of the mobility and carrier density. The intrinsic temperatures, as predicted from equation (2.7), is approximately 875°C for GaAs and 550°C for Si. In reality the intrinsic point will not be abrupt and hence the turnover temperature will not be well defined. The Si results approximately match the predictions made by Runyan using similar techniques[20]. The above results are important when the temperature of a device is increasing to well above its normal operating temperature by, for example, joule heating. In principle, heating a device from room temperature to the intrinsic temperature will cause the measured current to decrease, at a given applied potential. When the intrinsic temperature is attained, the current will increase dramatically causing the device temperature to rise very fast. The temperature of the device will continue to increase until the melt temperature is reached, or the structure of the material is changed by the indiffusion of metallic impurities or by dissociation of the base elements.

It has been previously suggested by Buot[21] that the critical temperature for thermal runaway in a GaAs MESFET is between 500°C and 550°C and is initiated at the active layer-substrate interface (up to 5μm beneath the surface). This temperature is lower than the 875°C intrinsic temperature predicted above.
Fig. (2.7) GaAs Resistivity vs Temperature

Fig. (2.8) Si Resistivity vs Temperature
A simple model to explain the effect of substrate conduction on the breakdown characteristics of a MESFET device is to consider the active layer and the substrate as two parallel resistors, with initial doping levels of $10^{17}$ cm$^{-1}$ and $10^{13}$ cm$^{-1}$, and to analyse the effect of temperature on the resistance of each layer. The resistance of each layer is given by:

$$R_l = \frac{\rho L_d}{A_d}$$  \hspace{1cm} (2.8)

where $\rho$ is the layer resistivity, $L$ the device length and $A$ is the cross-sectional area. Combining equations (2.7) and eqn. (2.8) and analysing the effect of increasing the depth of the substrate layer, it can be shown that the intrinsic temperature of the parallel combination decreases to $525^\circ$C, provided substrate conduction takes place up to $\approx 1\mu$m into the substrate[22].

### 2.5 GaAs MESFET Device Technology

#### 2.5.1 Introduction

In this section, specific areas a MESFET\MES device which effect the operation of a device under normal and stressed conditions shall be described. This knowledge is important in order to evaluate which device properties effect the electrical characteristics of a device and those which are likely to change as a result of overstress reliability testing.

#### 2.5.2 Contact Technology

##### 2.5.2.1 Gate Contacts

The theoretical basis of how the gate contact modulates the depletion region in FET structures is based on the simple physics of Schottky barrier formation and operation under bias. These are described in detail in refs. [23] and [24].

When a metal is placed in contact with a wide band gap semiconductor
with a moderate doping density \((10^{16} < N_d < 10^{18})\), the resulting contact is rectifying in nature and can be considered similar to that of the normal p-n diode in its electrical operation. The current density the across the contact region, under forward bias may be expressed by:

\[
J = A'^* T^2 \exp(-q\phi_b/kT) \exp(qV/n_i kT) \quad (V >> kT/q) \quad (2.9)
\]

or

\[
J = J_r \exp (qV/n_i kT) \quad (2.10)
\]

where \(J\) is the current density, \(J_r\) is termed the reverse current saturation value, \(A'^*\) is Richardson's constant, \(T\) the absolute temperature, \(q\) electron charge, \(\phi_b\) is the barrier height, \(k\) is Boltzmann's constant, \(V\) the applied voltage and \(n_i\) is the ideality factor. The ideality factor is a coefficient which would be 1 if the diode contact were perfect and has been added to the equation to describe the, "quality", of the interface. In practice this value can be between 1.1 and 1.3. The ideal forward bias current/voltage characteristic is shown in fig. (2.9)

A direct consequence of placing a metal contact on a wide band gap semiconductor, with n-type doping, is that the portion of semiconductor beneath the contact becomes depleted of carriers and a depletion region is created. This is analogous the formation of the depletion region in a p-n diode structure. The reverse situation, where the active layer has p-type doping, is equally valid.

The depth to which this depletion region extends within the substrate is a function of the material permittivity, \(\varepsilon\), the doping density, \(N_d\), electron charge, \(q\), the built in voltage, \(V_{bi}\), and the applied voltage, \(V\). The equation which gives the depletion depth, \(x\), for a uniformly doped semiconductor is given by:

\[
x = (2\varepsilon_\varepsilon_0 (V_{bi} - V)/qN_d)^{1/2} \quad (2.11)
\]

The built in voltage represents the voltage required to forward bias the contact, and hence make depletion depth tend to zero. All values must be taken as positive. The band diagram for a theoretical n-type metal-semiconductor contact under various bias conditions is shown in fig. (2.10).
Fig. (2.9) Diode Current - Voltage Characteristics

\[ KT/q = 0.0259V \]

\[ I_0 = 1 \mu A \]

\[ I = I_0 \exp\left(\frac{qV}{nKT}\right) \]

Fig. (2.10) Metal - Semiconductor Band Diagram

Metal

Semiconductor

\[ q\phi_b \]

\[ E_F \]

\[ E_F \]

\[ E_C (V>0) \]

\[ E_C (V=0) \]

\[ E_C (V<0) \]
Under low-voltage (+0.7 < V < +1V) bias, current can pass from the metal to the semiconductor with relative ease. Under reverse bias conditions current flow is impeded by the depletion layer until impact ionisation occurs. From eqn. (2.11) the capacitance of the depletion layer may be calculated approximately using a parallel plate capacitor model, but of course its value will vary with applied voltage. Capacitance-voltage plots can in turn be used to show the variation in n-type layer doping as a function of depth. This technique will be described in section 2.6.4.

In principle any metal can be used for a gate contact but it must exhibit three practical properties, good adhesion, thermal stability over a wide range of temperatures and have a low diffusion rate into GaAs. These three practical criteria eliminate many metals. If a gate metal readily diffuses into the GaAs surface, the rectifying properties of the diode will be degraded. The use of pure gold has been eliminated for reasons of high diffusivity in GaAs and poor adhesion qualities. Metals meeting all three criteria in varying degrees are Al, Cr, Ti and Mo.

2.5.2.2 Ohmic Contacts

In order to allow an electrical current to flow into, or out of, a real device structure an ohmic contact must be laid down onto the semiconductor. This contact must have linear conduction properties, be stable over a wide range in temperature, and have as little parasitic resistance or capacitance as possible. These criteria, though seemingly simple, are very hard to achieve in practice and historically each manufacturer has developed his own technique of creating ohmic contacts.

Because ohmic contacts are so important in semiconductor devices substantial experimental effort has been directed toward developing practical metallisation and processing procedures.

As with the gate contact, when the ohmic metal is first placed on the semiconductor surface, a rectifying contact is created. From theory[23,24], the barrier height $\phi_b$ of the junction would be expected to be a function of the metal. This has been found not to be the case in practice, and all the metals used have
produced barrier heights in typical contacts of around 0.8 eV. This discrepancy has been attributed to the presence of surface states on the surface of the GaAs[25,26].

In order to create an ohmic contact the barrier width must be decreased allowing tunnelling to become the dominant conduction mechanism[27]. This is achieved by highly doping the surface of the GaAs. It has been found that the required doping density is in the order of $10^{19}$ donors/cm$^3$.

Almost any metal can be used to create an ohmic contact if the surface is doped highly enough, but these high doping levels are not easily achieved in practice and so the need to alloy the contact to the GaAs becomes apparent. Alloying an ohmic contact to GaAs allows some of the metal(s) to enter the material and so highly dopes the surface layers. Historically AuGeNi[28] has been used as the ohmic metal with the Ge acting as the dopant, the Ni as the wetting agent, and Au to decrease the overall resistance. Recently, the presence of Ni has been linked to successful diffusion of the Ge into the GaAs and so prevent "balling" on the surface subsequent to alloy[29]. The actual alloying process is normally carried out at around 450°C and can be accomplished by several methods including flash lamps, lasers, and furnace heating.

One important property of ohmic contacts which is relevant to this study is the measure of the distance into the ohmic contact at which a finite current is present. This distance is known as the transfer length, $L_t$[30,31]. Analytically, this value is a measure of when the current density falls to $1/e$ of its original value. In practical terms this means a contact over a few microns long can be regarded as semi-infinite. The measurement of this quantity is achieved using specially designed test patterns which have ohmic contacts spaced at varying distances. A typical such pattern is shown in fig. (2.11). The resistance values for each spaced contact can be plotted on a graph and the best straight line fitted to the data. The equations, derived from transmission line techniques, relating to these parameters are:

$$R_m = 2R_c + R_{sh}L/W \quad (2.12)$$

and

$$R_c = R_{sh}L_t/W \quad (2.13)$$

where $R_m$ is the measured resistance, $R_c$ the contact resistance, $R_{sh}$ is the sheet
Fig. (2.11) Ohmic Contact Test Pattern

Fig. (2.12) Graphical Measurement of Ohmic Transfer Length

\[
\frac{dR}{dL} = \frac{R_S}{W}
\]
resistance between the contacts, $L$ is the contact spacing, $W$ is the contact width, $R_{sc}$ is the sheet resistance under the contacts, and $I_\alpha$ is the transfer length. If the measured resistance is taken to zero, the equation becomes:

$$2R_c = -\frac{R_{sh}L}{W}$$

(2.14)

and if the contact distance tends to zero, the equation becomes:

$$R_m = 2R_c$$

(2.15)

If the quantities $R_{sh}$ and $R_{sc}$ are equal, the intercept on the x-axis is twice the transfer length, $I_\alpha$ and the intercept on the y-axis is twice the contact resistance, $R_c$. This technique is illustrated in fig. (2.12).

### 2.5.3 MESFET Device Structure

The MESFET has been the predominant device structure used in many applications requiring high frequency, low noise and high gain amplifiers. This structure was first proposed in 1966[32] and was first successfully fabricated in 1967[33].

Typical cross-sectional and plan views of a low noise FET are shown in figs. (2.13) and (2.14) respectively. The device consists of the two ohmic contacts, termed the source and drain which allow current to flow into and out of the active layer. Between these contacts is the gate, which is used for modulation of the current in the active layer using the Schottky depletion region formed when the gate metal is laid on the GaAs surface. For historical reasons the dimension of the gate parallel to the source drain edges is called the gate width $W_g$, and the dimension perpendicular to the ohmic edges is called the gate length $L_g$. The active layer of the device consists of an highly doped region directly beneath the contacts which is nominally up to 0.3μm deep. The device is isolated by etching, or proton bombardment, leaving only the region between the source and drain for current to flow. This structure is called a depletion mode or d-type MESFET. Usually the MESFET is made common at the source terminal and the drain is
biased from +4V to +10V. The gate can be used to modulate the current in the active layer by providing a bias from 0 to \(-V_p\). The pinch-off voltage \(V_p\) is that voltage which depletes the channel, under the gate, of virtually all carriers and thus causes the channel current to become negligible. Typical characteristics of a MESFET are shown in fig. (2.15). These show the active layer current, termed the drain current \(I_{ds}\), as a function of the source-drain bias voltage \(V_{ds}\), for different values of gate bias \(V_{gs}\). The drain current can saturate at different values depending on the applied gate bias. This current saturation is attributed to the electron velocity reaching its limiting value.

With a greater interest in the use of GaAs MESFETs for digital integrated circuits several logic families have emerged. The d-type MESFET has been used in IC's designed using Schottky diode FET logic and buffered FET logic[34]. The problems with these structures include high power consumption and large pinch-off voltages. Continued research into digital circuits made from GaAs MESFETs has allowed another device called the enhancement mode or e-type MESFET to emerge. This structure is fabricated similarly to the d-type structure but the active layer is very thin, or the gate recessed allowing the depletion region to extend across the n-type layer impeding current flow when the gate is unbiased. Positive polarity bias on the gate will decrease the width of the depletion region and turn the device on, allowing a current to flow. This type of device has a lower power consumption than the d-type device.

**Fig. (2.13) GaAs MESFET Cross-Sectional View**

![GaAs MESFET Cross-Sectional View](image-url)
Fig. (2.14) GaAs MESFET Plan View

Passivation

Drain

Lg

Wg

Gate

Source

Fig. (2.15) GaAs MESFET $I_{ds}$ vs $V_{ds}$ Characteristics

Variables:
$V_{DS}$ - Ch2
Linear sweep
Start: -0.000V
Step: 4.0000V
Step: 0.0500V

Variables:
$V_{G}$ - Ch3
Start: -0.000V
Stop: -1.0000V
Step: -0.1000V

Constants:
$V_{G}$ - Ch1: 0.0000V

ID (mA)

12.00

1.200

/ div

0.0000

0.4000/div (V)

4.000
2.6 Device Electrical Characterisation

2.6.1 Introduction

In this section the techniques of MESFET electrical characterisation and the equations which model MESFET\MES low-voltage operation are described. These are particularly important because they shall be used to characterise the devices in the experimental study in chapter 5. An appreciation of the electrical and physical parameters which are likely to effect the normal current\voltage characteristics is necessary in order to assess how these characteristics may change subsequent to the application of an electrostatic discharge pulse.

A qualitative model of MES diode operation under highly stressed positive and negative polarity stressed operation is also introduced.

2.6.2 MESFET $I_{ds}$ vs $V_{ds}$ Characteristics

Using standard MESFET equations[35] the electrical characteristics can be linked to the physical dimensions of the device structure. The three key electrical parameters are the saturated drain current($I_{dss}$), pinch-off voltage($V_p$), and the transconductance($g_m$).

The magnitude of the saturated drain current, $I_{dss}$, can be calculated from equation (2.16).

$$I_{dss} = qv_s W_g (d-h) N_d$$  (2.16)

where

- $I_{dss}$ = Saturation current in amps
- $q$ = 1.602E-19 C
- $v_s$ = Saturation velocity of electrons ($\approx 1.2 \times 10^5$ ms$^{-1}$)
- $W_g$ = Gate width
- $h$ = Depletion depth at $V_{gs} = 0V$, $\approx 0.1\mu m$
- $d$ = n-type layer depth
- $N_d$ = Average donor density in the n-type layer, $10^{23}$ carriers per m$^3$. 

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Any calculated values of saturation current can only be approximate because equation (2.16) is only valid for constant doping in the n-type layer.

The pinch-off voltage can be calculated from equation (2.11) with the applied voltage set to $V_p$ and the value of, $x$, set to the n-type layer depth, $d$. The definition to be adopted in this thesis for $V_p$ is that value of the gate voltage which sets the saturation current to $< 10\mu$A. The equation which predicts the pinch off voltage, $V_p$, is:

$$V_p = qN_d d^2/2\varepsilon_0 \varepsilon_r + V_{bi}$$

(2.17)

Again, all values must be taken as positive.

The value of the n-type layer depth can also be calculated by rearranging equation (2.17).

$$d = \frac{2\varepsilon (V_p - V_{bi})}{qN_d}$$

(2.18)

The transconductance, $g_m$, of a MESFET is defined by the equation:

$$g_m = \frac{\delta(I_{ds})}{\delta(V_{gs})}$$

(2.19)

To obtain $g_m$ the current difference, $\delta I_{ds}$, is measured for a fixed change in the gate voltage, $\delta V_{gs}$ at a fixed value of $V_{ds}$ taken to be 2V.

The channel resistance, $R_{on}$ which can be extracted from the initial slope of the $I_{ds}$ vs $V_{ds}$ characteristics at zero gate bias. This parameter may be expressed as:

$$R_{on} \propto L_g V_s / \mu_h I_d$$

(2.20)

where $L_g$ is the gate length, $\mu_h$ is the Hall mobility, and $I_d$ is the drain current. It has been difficult, however, to determine an exact expression for $R_{on}$ which is compact.
2.6.3 Diode Characteristics

2.6.3.1 Normal Operating Conditions

Assessment of the electrical characteristics of the gate-source MES diode within a MESFET structure can reveal properties of both the depletion region and the GaAs active layer. The three main parameters which can be measured are, the ideality factor, $n_i$, the barrier height, $V_{bi}$, and the source resistance, $R_s$.

The ideality factor and barrier height can be measured using the forward $I_{gs}$ vs $V_{gs}$ characteristics of the MES diode. Rearranging eqn. (2.9) yields:

$$\text{slope} = \frac{dV}{d(\ln J)} = \frac{q}{n_i kT}$$ (2.21)

and

$$V_{bi} = \frac{kT}{q \ln(A'' T^2 / J_o)}$$ (2.22)

The current, $I_{gs}$, is plotted on a log scale against the applied voltage, $V_{gs}$, and the best straight line is fitted to the linear region. $\ln (I_o)$ is obtained from the intercept on the current axis.

The source resistance is also measured from the forward characteristics of the MES gate-source diode of the MESFET. In this case, however, the linear plot of $I_{gs}$ vs $V_{gs}$ is used. The slope of the linear region at high forward bias is a direct measure of the source resistance. Care must be taken to include any external resistances to the device in the calculation because the value of $R_s$ can be in the order of ohms.

It has been previously observed that if the forward bias voltage on the gate is increased to well above normal operating levels current saturation is observed in the $I_{gs}$ vs $V_{gs}$ characteristic[36,37]. The current is limited by velocity saturation in the portion of the channel which lies between the gate and the source of the MESFET. The approximate value of current saturation can be calculated from eqn. (2.16) with the depletion depth, $h$, set to zero. Hence:

$$I_s = qv_s W_g dN_d$$ (2.23)
2.6.3.2 Positive High Voltage Operation

If the current increases above normal operating levels ($V > +2V$) in an MES structure it is likely that conduction between the gate(anode) and source(cathode) becomes limited by velocity saturation. As the current continues to increase the current may become space charge limited[38] because the injected electron density exceeds the intrinsic carrier density. The current will then gradually rise with a finite "space charge limited resistance" until the device becomes unstable and the current rises rapidly. This instability may be linked to either the onset of impact ionisation or the device entering a region of negative differential resistance, commonly observed in two-valley semiconductors. This is known as the transferred electron effect[39-42]. The impact ionisation threshold field in GaAs has been estimated to be $\approx 400 \text{kVcm}^{-1}[43]$, while the transferred electron effect would take place at $\approx 3.2 \text{kVcm}^{-1}[44]$. Therefore, a device would enter a region of negative differential resistance due to intervalley electron transfer well before the initialisation of impact ionisation.

A simple model for intervalley electron transfer, outlined in Sze[44], states the following conditions must be fulfilled for a device to exhibit negative differential resistance:

a) The lattice temperature must be low enough that, in the absence of an electric field, most electrons are in the lower conduction band minimum, or $kT < \Delta E$.

b) In the lower conduction band minimum the electrons must have high mobility, small effective mass and a low density of states.

c) The energy of separation between the two valleys must be smaller than the semiconductor bandgap so that avalanche breakdown does not set in before the electrons are transferred to the upper valleys.

There exists a well defined threshold field for the onset of negative differential resistance and the threshold field increases with increasing lattice temperature. Thus, if joule heating effects raise the lattice temperature, the
process will be inhibited. The actual effect on the voltage/current characteristics will depend whether the process is controlled by the device current or the device voltage[39]. When the voltage is used, travelling high field domains form within the device as observed in the Gunn effect[45]. When the current is used, current filaments will form along the direction of the field[39].

2.6.3.3 Negative High Voltage Operation

Under reverse bias high stress conditions the device current will remain relatively stable until the field is sufficient to induce impact ionisation within the depletion layer. The impact ionisation process is exponential in nature when the electrons have sufficient energy to overcome normal scattering effects such as impurity scattering and optical phonon interaction in GaAs[46]. The voltage across the depletion layer will now become effectively pinned, and any further increase in the driving voltage will appear across the bulk of the device because the current is limited by the resistance of that region. As the current increases further, joule heating effects within the depletion layer and the bulk will cause the temperature to rise. This will cause the ionisation rate to decrease and a greater voltage will be required to sustain the current[46]. The voltage across the device will continue to rise as the temperature increases until the device reaches the intrinsic temperature (see section 2.4.3). The current will then rapidly increase due to the positive feedback effect. If this condition is sustained, permanent damage will result.

2.6.4 Capacitance-Voltage (C-V) Profiling

The sophisticated device structures available today often require highly tailored impurity distributions for optimum operation of a device. The conventional methods of assessing the net doping level within these layers are Secondary Ion Mass Spectrometry (SIMS)[47], sheet resistivity and capacitance-voltage measurements[48]. However these techniques do not necessarily produce the same results for the impurity distribution with depth. SIMS will yield the profile of a particular impurity without details of its state of charge. Sheet
resistivity gives the number of electrically active impurities, but neglects deep levels. Capacitance-voltage measurements give the electrically active net majority dopant concentration or net impurity concentrations $N_d - N_a$.

In practice, impurity profiles can be obtained for p-n junctions or Schottky barriers from the edge of the depletion layer at zero bias to the edge of the depletion layer at the onset of avalanche breakdown. This criteria for accuracy corresponds to a finite distance into the depletion region. The capacitance is measured using a small, <10mV, sine wave superimposed on a DC bias signal. This bias must fulfil the criteria mentioned above. The differential capacitance is defined as:

$$C = \frac{dQ}{dV} = \varepsilon_r \varepsilon_0 \frac{Area}{x}$$  \hspace{1cm} (2.25)

where

- $Area$ is the diode area
- $\varepsilon_r \varepsilon_0$ is the relative absolute permittivity
- $x$ is the depletion depth.

The net impurity concentration at the edge of the depletion layer is given by:

$$N_d = \frac{-C^3/(q\varepsilon_r \varepsilon_0 Area^2)}{(dC/dV)^4}$$  \hspace{1cm} (2.26)

The simplest method of obtaining the capacitance-voltage profile is to record a large number of values of capacitance and voltage point by point by the use of a specialised bridge and a computer. Measurements are normally made at 1MHZ, suitable for free carrier response but not deep levels.

2.7 Summary

This chapter has discussed the principle properties of GaAs and its use in high speed transistor structures. Techniques of device characterisation have been discussed and the equations relating to the operation of a MESFET/MES structure under normal operating conditions have been introduced. The necessary conditions for a MES diode to exhibit negative differential resistance and impact ionisation under highly stressed conditions have also been described.
2.8 References


3.1 Introduction

A complete understanding of device failure mechanisms is important to semiconductor device designers, manufacturers and consumers. Such knowledge should enable consumers to develop effective procurement policies and the manufacturer to give realistic predictions of the lifetime of a device. Accurate information on reliability allows the manufacturer to ensure that the production techniques employed optimise quality, and cost effectiveness.

This chapter describes the known failure mechanisms in common semiconductor devices, the various techniques used to identify these failure mechanisms and how this data is used to predict the lifetime of a device. The existing literature on the failure mechanisms in GaAs low-noise and power MESFETs is reviewed in detail. This information allows an appreciation of the likely failure mechanisms to be encountered in GaAs devices and how device failure is characterised during reliability testing.

3.2 Failure Mechanisms

The mechanisms of semiconductor failure can be classified into three main areas:

1) Intrinsic Failure Mechanisms;
2) Extrinsic Failure Mechanisms;
3) In-Circuit Electrical Overstress Failure.
Intrinsic failure mechanisms are inherent of the semiconductor base material, implants, oxides, and passivations which go to make up a typical semiconductor device. Such mechanisms include crystal defects, dislocations and processing defects. Failures due to the above problems will be minimized in future generations of semiconductor devices due to the natural progression of growth techniques, yielding base materials which are closer to an ideal specification.

Extrinsic failure mechanisms are a result of device packaging and the interconnection processes in semiconductor manufacturing. Such mechanisms include, bond failures, encapsulation failures, and metal migration. As fabrication techniques mature the many problems associated with a immature technology, such as GaAs, will eventually be overcome and devices will be operating at their optimum efficiency, leaving only event dependant mechanisms, such as electrostatic discharge, to cause failure.

Electrical stress failures are event dependant mechanisms which are directly related to either poor the design of equipment leading to electrical over-stress, or careless handling of components leading to electrostatic damage. The normal cause of such failures is misuse, bad handling procedures and poor circuit design by the person or persons involved in the fabrication or utilisation of these devices. This area of semiconductor failure is of the upmost importance to the manufacture of devices and equipments. With proper training of the relevant personnel, failures due to these mechanisms, could be reduced to the absolute minimum.

3.2.1 Intrinsic Failure Mechanisms

3.2.1.1 Gate Oxide Breakdown

Failure in MOS gate oxides can be induced by high electric fields generated by electrical over-stress or static discharge which exceeds the oxide breakdown threshold and is followed by a large passage of current, and resultant failure[1,2]. Time dependant breakdown occurs at weak points within the oxide layer due to poor processing or uneven oxide growth. To screen for time
dependant failures involves the application of a drive voltage, 50% above the rated threshold for the device for 1 second. If the device survives this screening it has been shown by Crook[3] that a devices will have a subsequently lower failure rate as compared to unscreened devices.

3.2.1.2 Ionic Contamination

Many semiconductor devices are susceptible to contamination by mobile ions. Though the device are fabricated in so called "clean" environments many opportunities exist for contamination. The effect of this contamination will depend on the device structure.

The major contaminants in are Na\(^+\), Cl\(^-\) and K\(^+\), which have been identified by spectroscopic analysis in many Si semiconductor devices[4]. The presence of these ions within encapsulated devices is not surprising because Na\(^+\) is commonly available in the environment with the atmosphere, sweat, and breath carrying traces of NaCl.

The effects of contamination are most pronounced in MOS structures which rely on stored charge to maintain operating levels. Planar devices with poor device passivation can be rendered inoperable by leakage paths caused by ionic contamination.

Generally, a high temperature bake between 150°C and 250°C, and/or a reverse bias screen before encapsulation has been used successfully to eliminate such contamination in Si devices[5].

3.2.2.3 Charge Effects

Failure mechanisms which involve charge storage or charge movement tend to effect the MOS devices to a greater extent than the normal p-n junction based devices because the MOS families rely on strict charge placement and magnitude for correct operation.

The two major charge related effects reported in the literature are:
a) Surface charge spreading - Charge may spread out from biased conductors causing an inversion layer to be formed outside the active layer in MOS devices[6]. Such inversion may cause a conduction path between two previously insulated regions. Good design of the device as well as a high temperature reverse bias screen will decrease this effect.

b) Trapping - Interstitial trap sites at Si-SiO₂ interfaces, or surface traps in GaAs can cause depletion or inversion regions when electrons have enough energy to reach these traps. The susceptibility of a device will be dictated by the energy level magnitude(s). In GaAs, such a number of deep level traps have been observed[7]. Good quality material is the only real way of eliminating this failure mechanism.

3.2.1.4 Crystallographic Effects

Metallic shunt paths maybe created within a semiconductor device along crystal defects created during wafer processing. A common cause of these paths, or pipes as they are known in Si devices, is phosphorus or gold diffusion along crystal defects in the base semiconductor[8].

In planar Si bipolar devices the creation of pipes within the active layer can cause parametric shifts in the electrical characteristics. Resistance of the pipes tends to be linear only at low voltages. The effective resistance increases with current density until junction breakdown occurs.

Manufacturers have devised several ways of detecting and screening for crystal defects. Evidence of piping may be obtained by selecting sampling of junction areas, thereby reducing the number of continuity tests required. In addition, output leakage currents and monitoring the supply voltages is supplementary to the sampling tests.

A reduction in pipe defects may be achieved by better growth or implantation techniques to create the active layer. Dislocations within a device may give rise to similar electrical effects to those observed with piping, and have been linked to the gettering of dopants in areas of the active layer[9]. Dislocations have been identified as the main source of low-frequency noise in
Si bipolar transistors[10], and to cause shifts in the threshold voltage in GaAs MESFETs[11].

### 3.2.2 Extrinsic Failure Mechanisms

#### 3.2.2.1 The Packaging

Extrinsic failure mechanisms are greatly influenced by the packaging technology. The two main types of packaging used are:

a) Hermetic or CERDIP(ceramic dual-in-line package)
b) Plastics (PEDs)

A third variety of packaging, the hybrid package, includes many types of components within the same package. This includes passive components as well as semiconductors. The reliability of such packages is well documented in refs. [12-14].

Hermetic packages consist of a ceramic material which forms a protective shell around the semiconductor chip. This shell is filled with a non-reactive gas, usually \( \text{N}_2 \), which creates a sterile operating environment about the bare semiconductor device. Connections to the real world create possible leakage paths for contaminants, so 100% protection from the atmosphere cannot be guaranteed.

Plastic packages are formed by a moulding process. The semiconductor chip is attached to a lead frame and is encapsulated in plastic using a transfer moulding process, thereby creating a solid unit. One problem with this technique is that high temperatures are required to complete this process. Plastic compounds such as epoxy-novolac and silicon copolomers are porous to moisture and represent a serious reliability problem. Contamination of the epoxy can be transferred to the semiconductor surface giving rise to the charge related effects outlined in section 3.2.2.3. Mechanical stress generated during the moulding process has been found to change the properties of Si transistors[15].
Because of the chemical instabilities, plastic is not considered suitable for high reliability packaging, though many devices encapsulated in this way are available on the consumer market.

3.2.2.2 The Metallisation

There are four main areas in which the metallization can effect the reliability of a semiconductor device. These are:

a) Corrosion
b) Electromigration
c) Contact Migration
d) Mechanical stress relaxation

Each of these areas shall be considered in below.

3.2.2.2.1 Corrosion

Corrosion is an electrochemical mechanism which only occurs if all the criteria below are fulfilled:

i) moisture present
ii) DC bias operation
iii) Cl⁻ or Na⁺ ions present to act as a catalyst.

In the absence of any of these criteria corrosion will be inhibited. If Cl⁻ or Na⁺ ions are not present, corrosion will not take place[16].

3.2.2.2.2 Electromigration

If a sufficiently high current density is flowing in the metallization the continuous impact of electrons on the Al grains causes the grains to move in the direction of electron flow. If this continues a void will eventually be created at
one point in the track. An example is shown of an electromigration failure is shown in fig. (3.1). Here an open circuit in an Al interconnect is the failure mode in a typical Si transistor[17]. Electromigration is heavily influenced by the metallisation grain size. Smaller grain sizes are more easily transported.

Extensive work into the physics of this failure mechanism in Al on Si has been completed[18]. The predominant electromigration mechanism is considered to be the movement of atoms along the crystal grain boundaries. An activation energy of 0.45eV has been calculated and is used to characterise the temperature dependence of electromigration. Analysis of the mechanism can be enhanced by using a combination of both current density ($J > 10^6$ Acm$^{-2}$) and temperature, typically 180°C, in accelerated tests. As a consequence of intense research into electromigration this failure mechanism has almost been eliminated in many semiconductor devices.

**Fig. (3.1) Open Al Interconnect due to Electromigration[17]**
3.2.2.2.3 Contact Migration

This mechanism is another form of metallisation migration. The physical processes governing the movement of the metal atoms is different from that of electromigration.

The migrating species could either be Al in Si, or Au in GaAs. Depending on the contact depth and the contact size the failure mode manifests itself as a shorted junction or an open contact. For this reason it is also referred to as "spiking".

Much research is currently being conducted into the physical processes taking place at a metal-semiconductor interface. The physical bond formed at the contact boundary is ideally formed by the exchange of a few atoms of each element. However, if the exchange of atoms is not controlled then interdiffusion will continue and results in changes in the properties of the contact(s). This has found to be a dominant failure mechanism in early GaAs MESFET structures[19].

The solution to contact migration has to be the inhibition of the metal diffusion into the active layer of a device. This could be achieved by using several layers of different metals, specific layers having the properties of stopping the interdiffusion of the metal above. PtSi-Ti/W-Al has been shown to ensure good reliability in Si devices[20] and TiPtAu/TiWAu has been used with success in GaAs Devices[21].

Modern theories have succeeded in modelling this failure mechanism to some extent. However, for the system designer contact migration is modelled using electromigration theory[22] with an activation energy of 0.6eV.

3.2.2.2.4 Mechanical stress relief relaxation

This failure mechanism is another form of metal migration. The migration is due to atoms being transferred from areas of high stress in order to equalize the stress with the resulting deformation of the metal[23]. This phenomena is known as "whisker growth". It is characteristic of compressive stress and whiskers will grow until sufficient metal has been moved to equalize the stress.
Failure is caused by short circuits between metal tracks which lead to burn-out. Unfortunately, due to the nature of the failure, no trace of the original mechanism may be left.

3.2.2.3 Bonding

The bond may be considered to be one of the weakest areas of the device packaging. There are four areas which describe failures caused by bonding.

i) **Formation of intermetallics** - This is due to the interdiffusion between the bond pad and the bond wire metals. Since Au is the primary metal used for bonding in both Si and GaAs devices this represents a serious problem. If the bond is not of sufficient quality the result is the formation of a particular alloy called "purple plague"[24]. Other alloys may also be present and are known as "white plague". It is the presence of these that causes bond failure[25].

ii) **Bond Looping and Lagging** - During the bonding process a loop must be formed between the semiconductor bond pad and the lead frame. If the loop is too tight it creates tension at the heel and neck of the bond causing premature failure by slippage of the bond material. If the bond loop is too shallow the possibility of short circuits between adjacent bond wires is increased.

iii) **Bond Integrity** - Moisture has been found to aid metal migration by electrolysis[26]. Contamination by atmospheric impurities is also another factor which reduces the integrity of the bond wire[27]. Improved fabrication methods have improved bond integrity in recent years.

iv) **Bonding Pressure** - Incorrect bonding pressures can lead to bonds with low fracture strengths or other failure modes described in this section.
Poor bonds can exhibit a high contact resistance when first fabricated, or lead to premature failure when in the field or under accelerated lifetests. The use of multilayer bond pads or eutectic bond wires can reduce the formation of intermetallics and give better bond integrity. The other failure mechanisms are fabrication related, and design experience will lead to the elimination of these in the future.

3.2.2.4 Radiation Induced Failure

This is an event dependant failure mechanism and particularly relevant to semiconductor devices which are to be used on board spacecraft.

Radiation affects semiconductor devices through the generation of electron-hole pairs within the bulk of the device. There are two main types of radiation.

i) **External Radiation** - i.e., Gamma rays, cosmic rays and X-rays.

ii) **Intrinsic Radiation** - i.e., $\alpha$ particles and $\beta$ radiation.

Different semiconductor devices tend to be affected by radiation in different ways. Si bipolar and GaAs transistors show an increase in low frequency noise, higher leakage currents and a reduction in current gain. MOS devices show threshold voltage shifts, a reduction in transconductance and an increase "soft errors" in digital devices[28].

GaAs MESFETs, because they are majority carrier devices, are relatively radiation hard compared with Si devices. The absence of an oxide also makes GaAs devices less sensitive to incident radiation[29]. Zuleeg[30] presented a detailed study on the effects of radiation in GaAs devices, his conclusions were basically:

i) **Displacement** - where radiation generates defects in the crystal lattice by displacing lattice atoms, additional energy states introduced within the forbidden band which may act as traps. In severe cases, this would lead
to an effect similar to decreasing the net doping level in the channel of a MESFET.

ii) **Ionisation** - electron-hole pairs are formed thus increasing the leakage currents with a device.

For further information on radiation induced failure in GaAs devices the reader is referred to refs. [31-35].

In order to decrease the sensitivity of semiconductor devices to radiation induced effects several proposals have been put forward, these include the reduction in thickness of gate oxides and the formation of "shields" [36]. In GaAs, tailoring of the doping profile has been suggested to decrease sensitivity [29,30].

### 3.2.3 Electrical Overstress Failure Mechanisms

#### 3.2.3.1 Introduction

Electrical overstress is a result of the improper handling or application of a device. No operating environment is ideal, and a device which has been manufactured to a given specification is expected to tolerate overstress voltage or current pulses and hence increased temperatures within the active regions of a device for a short time [37].

#### 3.2.3.2 Electrical Overstress Failure Modes

Electrical overstress failures are usually associated with hot-spot development in the semiconductor active region. This is essentially due to an increase in current flow in order to accommodate the excess stress on the device. Hot-spot development is normally due to the current density at some point being sufficiently high to cause melting of the semiconductor, metal or oxide. Once the melting point has been reached a low resistance path is created by metal migration or the dissociation of base elements.
3.2.2.3 Second Breakdown

Prior to full burnout taking place in a semiconductor device a phenomena known as second breakdown may take place. This effect first reported in Si devices in 1958 by Thorton and Simmons[38]. They suggested that this effect was the cause of certain types of mysterious failures in standard circuits.

Alexander[39] described the second breakdown process in terms of the resistivity variation with temperature (see section 2.4.3). Fig. (3.2) shows the variation of the resistivity with temperature with various doping levels in bulk Si. It can be seen that the material initially has a positive temperature coefficient until a "turn-over" point is reached and then the material exhibits a negative temperature coefficient of resistivity. The rapid decrease in resistivity following the turnover point will result in an increase in current density in any region subjected to a constant voltage. The subsequent heating of the material, due to this positive feedback effect, will cause a temperature rise to the melting point. The result is irreversible damage.

When a p-n, or metal-semiconductor, junction is formed on the material the sequence for initiating damage is modified. Consider a p-n junction subjected to a constant reverse bias current which has driven the diode into reverse avalanche breakdown. The current will produce heating in the depletion region. This produces an increase in the avalanche voltage due to the increase in the ionisation coefficients[40]. However, the thermally generated current will also increase with temperature. At the temperature at which the thermal current dominates the total current the voltage across the junction goes to zero and the junction is said to have gone intrinsic. The total voltage across the diode may only decrease slightly because the junction has only gone intrinsic in a localised region(s). The voltage which was dropped across the avalanching junction is now likely to be dropped across the intrinsic Si resistance external to the junction. This intrinsic resistance is linked to the characteristics in fig. (3.2). If the current continues to flow the hot spot will extend further into the material until it reaches the metallisation contact or low resistivity layer. When the hot spot encounters the low resistivity material the current is no longer contained and a rapid increase in current is evident. This sequence of events is almost
instantaneous and results in permanent device damage due to the formation of a melt channel. In constant current stressing, certain portions of the voltage waveform across the device can be associated with hot spot formation. However, if constant voltage stressing is used the transition from hot spot formation to the full melt channel occurs simultaneously and the sequence of events cannot be discerned in the current waveform. The current and voltage waveforms for constant voltage stress are schematically shown in fig. (3.3) and (3.4). It can be seen that before the breakdown point, both waveforms are effectively constant. The current and voltage waveforms for constant current stressing are shown in figs. (3.5) and (3.6). In this case the voltage waveform can be seen to vary in accordance with the formation of the melt channel. This is an important point, because the experiments carried out in the study reported in this thesis used only constant voltage stressing.

The current waveforms, associated with forward bias second breakdown are expected to be similar to that for reverse breakdown except that the depletion region no longer exists and the hot spot formation is directly controlled by the intrinsic material temperature coefficient of resistivity shown in fig. (3.2). Further reviews on second breakdown in Si devices can be found in refs. [41-46].
Fig. (3.2) Si Resistivity vs Temperature[39]
Fig. (3.3) Voltage Waveform for Constant Voltage Stressing[39]

Fig. (3.4) Current Waveform for Constant Voltage Stressing[39]
Fig. (3.5) Voltage Waveform for Constant Current Stressing[39]

-50

Device Voltage (V)

-25

Voltage increase with Junction heating

Hot Spot Growth

Melt Channel Formation and Catastrophic Damage

Time (us)

0 1 2 3 4 5 6

Fig. (3.6) Current Waveform for Constant Current Stressing[39]

-500

Device Current (A)

-400

-300

-200

-100

0

0 1 2 3 4 5 6

Time (us)
3.2.2.4 Electrostatic Damage in Semiconductor Devices

A particularly important subsection of electrical overstress, relevant in this thesis, is damage induced by electrostatic discharge (ESD) pulses.

The theory and physics of static charge build-up is well known. The magnitude of the charge built up in typical working environment, and the potentials generated are less well known. Voltages ranging from 100V to 20kV are quite possible.

Studies on the static build-up potential of various media were carried out by Moss[47] and are shown in Tables 3.1, 3.2 and 3.3. From table 3.1, it can be seen that air is the most susceptible to positive charge build-up followed by human skin. Silicon rubber, teflon and silicon are capable of carrying the most negative charge. In the middle of the list are materials such as wood, steel and other metals which have a low susceptibility to charge build-up.

Table 3.1 - Electrostatic Triboelectric Series[47]

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<tr>
<th>Most positive (+)</th>
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<td>Human skin</td>
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<td></td>
<td>Asbestos</td>
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<td></td>
<td>Fur (rabbit)</td>
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<td></td>
<td>Glass</td>
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<td></td>
<td>Mica</td>
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<td></td>
<td>Human hair</td>
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<td>Cotton</td>
</tr>
<tr>
<td></td>
<td>Steel</td>
</tr>
<tr>
<td></td>
<td>Wood</td>
</tr>
<tr>
<td></td>
<td>Sealing wax</td>
</tr>
<tr>
<td></td>
<td>Hard rubber</td>
</tr>
<tr>
<td></td>
<td>Nickel, copper</td>
</tr>
<tr>
<td></td>
<td>Brass, silver</td>
</tr>
<tr>
<td></td>
<td>Gold, platinum</td>
</tr>
<tr>
<td></td>
<td>Polyester</td>
</tr>
<tr>
<td></td>
<td>Celluloid</td>
</tr>
<tr>
<td></td>
<td>Orlon</td>
</tr>
<tr>
<td></td>
<td>Polystyrene</td>
</tr>
<tr>
<td></td>
<td>Saran</td>
</tr>
<tr>
<td></td>
<td>Polyethylene</td>
</tr>
<tr>
<td></td>
<td>Polypropylene (foam)</td>
</tr>
<tr>
<td></td>
<td>Polyvinyl chloride</td>
</tr>
<tr>
<td></td>
<td>Silicon</td>
</tr>
<tr>
<td></td>
<td>Teflon</td>
</tr>
<tr>
<td></td>
<td>Silicone rubber</td>
</tr>
</tbody>
</table>
Other studies on the effects of humidity on static charge build-up have shown that various events, typical in the fabrication and application of semiconductor devices, will accumulate less static charge when in a high humidity environment. Table 3.2 shows the measured potentials from these typical events.

**Table 3.2 - Static Voltages as a Function of Humidity[47]**

<table>
<thead>
<tr>
<th>Action</th>
<th>20% RH (kV)</th>
<th>80% RH (kV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Walking across vinyl carpet</td>
<td>12</td>
<td>0.25</td>
</tr>
<tr>
<td>Walking across synthetic floor</td>
<td>35</td>
<td>1.5</td>
</tr>
<tr>
<td>Arising from a foam cushion</td>
<td>8</td>
<td>1.5</td>
</tr>
<tr>
<td>Picking up of a polyethylene bag</td>
<td>20</td>
<td>0.6</td>
</tr>
<tr>
<td>Sliding styrene box on carpet</td>
<td>18</td>
<td>1.5</td>
</tr>
<tr>
<td>Removing mylar tape from PC board</td>
<td>22</td>
<td>1.5</td>
</tr>
<tr>
<td>Shrinkable film on PC board</td>
<td>16</td>
<td>3</td>
</tr>
<tr>
<td>Triggering vacuum solder remover</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Aerosol circuit freeze spray</td>
<td>15</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 3.3 shows the variation in ESD sensitivity for a large cross-section of semiconductor devices. This table indicates the extent of the problem, and the need to successfully categorise each device structure to allow preventative measures to be taken.

**Table 3.3 - Component ESD Sensitivities[47]**

| Class | Unprotected MOS(discrete & IC) | Small geometry Schottky logic | Junction field effect devices | Low power Si rectifier | Microwave and VHF transistors | Precision IC voltage regulators | VLSIC's with dual level metal | Protected MOS (CMOS,NMOS,PMOS) | Standard schottky logic | Bipolar linear IC's | High speed bipolar logic | Low-power diodes and transistors | Low-speed bipolar logic (TTL) |
|-------|--------------------------------|--------------------------------|-------------------------------|------------------------|---------------------------|---------------------------------|-------------------------------|-----------------------------|------------------------|----------------|-----------------|-----------------------------|---------------------------|-------------------------|
| Class 1 | (0 to 1kV)                      |                                |                               |                        |                           |                                 |                               |                            |                        |                |                  |                             |                           |                         |
| Class 2 | (1 to 4kV)                      |                                |                               |                        |                           |                                 |                               |                            |                        |                |                  |                             |                           |                         |
| Class 3 | (4 to 15kV)                     |                                |                               |                        |                           |                                 |                               |                            |                        |                |                  |                             |                           |                         |

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3.2.2.5.1 Electrostatic Discharge Modelling

In order to model the electrostatic discharge event, several models have been developed. The major models are the "human body model"[48] and the "charged device model"[49]. The human body model, as described in MIL. STD. 883C specification[50], consists of a 100pF "body capacitance" which is charged to the "ESD voltage" and subsequently discharged through a 1500Ω "body resistance" through a device under test. This circuit is shown in fig. (3.7). The specification for the current pulse from the circuit is shown in fig. (3.8). The pulse should be of \( \approx 10\,\text{ns} \) risetime, with the minimum of ringing in the waveform. Standard apparatus has now been developed to reproduce this pulse consistently[51]. The "charged device model" consists of charging the device with a fixed amount of charge and then discharging this to ground. The most common model in use today is the "human body model".

Fig. (3.7) Human Body ESD Circuit
3.3 Reliability Assessment

3.3.1 Introduction

The theoretical performance of semiconductor devices can be predicted using the geometry of a device, the metallisations and the fundamental properties of the semiconducting material. This will give a manufacturer an insight into the performance of his devices when subject to normal operating conditions.

Device reliability does not lend itself so readily to prediction. A designer can only use the existing literature, and his experience, to produce a device which will survive its full lifetime in the field. If the designer is using a relatively new material, as in the case with GaAs, the existing literature is not always available. Available literature can sometimes be misleading, because rival manufacturers are not always willing to reveal their full fabrication process, any part of which may have an major effect on the reliability of the device.
3.3.2 Definitions of Failure

The definition of failure of a device is important for the correct analysis of any data relating to reliability testing experiments. Failure are generally separated into two groups:

(1) **Degradation Failures** - where a parameter of a device drifts far from its original value so that a device no longer operates to its stated specification.

(2) **Catastrophic Failures** - when a device has reached the end of its life and no longer functions.

Degradation failures are normally characterised by a device's electrical characteristics changing over period of time due to particular failure mechanisms. This types of failure are called time dependant, while catastrophic failures tend to be the result of extensive degradation or by a single stress event, such as electrostatic discharge. This type of failure is called event dependant.

3.3.3 Statistical Analysis

O'Connor defines reliability as, "The probability that an item will perform a given function under stated conditions for a stated period of time"[52]. This definition therefore means that the reliability of a device can be modelled as a probability distribution.

Reliability distributions have existed long before semiconductor based devices were invented and the common distributions[52,53] which are used extensively are the normal, lognormal, gamma, and Weibull distributions.

The probability of a component surviving to a time \( t \) is the reliability, \( R(t) \), of that component, and is expressed as:

\[
R(t) = \frac{\text{Number surviving at time } t}{\text{Number at time } t}
\]  

(3.1)
The failure rate, $Z(t)$, can be expressed as:

$$Z(t) = \frac{\text{Number failing per unit time at instant } t}{\text{Number surviving at instant } t} \quad (3.2)$$

The failure rate is therefore defined as the probability of failure per unit time of a component which is still functioning satisfactorily.

For a constant failure rate, $\lambda$, $R(t)$ is given by:

$$R(t) = \exp(-\lambda t) \quad (3.3)$$

$R(t)$ is therefore an exponentially varying function of time.

The failure rate $Z(t)$, is given as numbers failing per unit time. In practice the number of components failing per second is a small fraction of a percent, and in order to obtain more manageable figures the units are scaled. $\lambda(t)$ may therefore be expressed as the $\%$ failures per $10^6$ working hours or as the number of devices failing in $10^9$ working hours. The later unit is commonly known as the FIT and is defined as the unit of reliability:

$$1 \text{ FIT} = 1 \text{ failure in } 10^9 \text{ device hours} \quad (3.4)$$

When modelling failures, confidence limits are put on the distributions indicating the validity of the predictions made from this data. Clearly reliability predictions made from one device failure in $10^9$ hours would have lower confidence level than a prediction made from $10^5$ failures in $10^{12}$ hours.

### 3.3.4 Accelerated Lifetesting

#### 3.3.4.1 Acceleration Conditions

Accelerated lifetesting of any new structure needs to be carried out to give the manufacturer enough data to give a realistic estimate of the lifetime of a device in the field. However until comparative data is received from the field...
no lifetest results can be said to model the expected lifetime of a device.

Typical accelerated tests use temperature between 75°C and 250°C, although higher or lower temperatures may be required depending on the failure mechanism(s) under investigation. A device could be subject to simple bias or standard operating conditions, which may include an RF bias. The use of the standard operating conditions is not recommended at temperatures in excess of the maximum rating of the device, as failures would not be representative of normal operation.

Dynamic accelerated life tests range from 168h (1 week) to 5000h (7 months) depending on the conditions of stress, the sample size, and the failure rates expected from the failure mechanisms under study. Of course, if a new structure is under test, the failure mechanisms are likely to be unknown, or have different activation energies from those experienced with previous devices. If this is the case, the lifetest must be designed to allow for the failure mechanisms with the lowest activation energy to be dominant.

Accelerated testing normally uses temperature as the acceleration mechanism. Other methods of acceleration include the use of humidity as an accelerating factor. This method usually is normally used in conjunction with temperature acceleration is usually carried out at temperatures between 85°C and 150°C with the relative humidity varying between 50% and 90%.

Current state of the art accelerated lifetesting can be achieved using an autoclave tester or "pressure cooker". The autoclave tester, working up to five atmospheres, 135°C, and 95% humidity allows the activation of failure mechanisms to be enhanced to a much greater extent than could be achieved using normal acceleration techniques.

### 3.3.4.2 Evaluating Accelerated Lifetest Data

The rate at which many chemical processes progress is governed by the Arrhenius equation below:

\[
r = A_r \exp\left(-\frac{E_a}{kT}\right)
\]  

(3.5)
where \( r \) is the rate of the reaction, \( A_r \) is a coefficient which maybe dependant on temperature, i.e \( A_r = A_r(T) \), \( E_a \) is a constant for a given reaction and is known as the activation energy and is usually quoted in electron volts (eV), \( k \) is Boltzmann's constant, and \( T \) is the temperature in Kelvin.

Equation (3.1) has been widely adopted by the electronic component industry as the guide line by which the operation of device under varying temperature conditions can be monitored. Experimental data obtained from accelerated life tests can be processed via the Arrhenius equation to obtain an estimate of the activation energy of a given process within a device. In semiconductor devices this process is the degradation of a device due to a particular failure mechanism.

Rearranging equation (3.1) gives:

\[
\ln(r) = \ln(A_r) - \frac{(E_a/k)(1/T)}
\]  

(3.6)

Using the assumption that chemical reaction processes are analogous to component failure rates, i.e, \( r = \) Failure rate, then equation (3.2) can be used in a graphical form to give the activation energy of a particular failure mechanism. The failure data at several temperatures is plotted as a failure rate against the inverse temperature. The best straight line is fitted to the data, \( E_a/k \) is obtained from the gradient of this line, and \( A_r \) from the intercept. Fig (3.9) shows how this data is displayed and has been taken from Ref. [88]. Clearly the power GaAs MESFET devices lifetested under bias, have a higher activation energy associated with the failure mechanism.

In the presence of more than one failure mechanism, as so often is the case, the data must be plotted for each failure mechanism and two lines of best fit must be used. Care must be taken therefore to eliminate all possible errors in temperature, and detailed failure analysis must be carried out on each device to ascertain which failure mechanism caused device failure. If one failure mechanism is dominating the failure data it maybe impossible to identify the activation energy of other mechanisms.

For the most part, it appears that, while discrepancies exist, valid estimates of activation energies can be made using this technique.
Fig. (3.9) Arrhenius Plot for Reliability Evaluation
(from Ref. 88)

Accelerated Lifetest
GaAs Power MESFETs

\[ E_a = 1.04 \text{eV} \]

\[ E_a = 1.85 \text{eV} \]

Log Mean Time To Failure (hrs)

Device Temperature (°C)
3.3.5 Failure Analysis

Failure analysis of devices from laboratory tests or from the field is of paramount importance within a reliability testing program. If the failure mechanism can be identified by failure analysis techniques, measures can be taken to eliminate it from future device structures. Failure analysis thus plays an important part in a laboratory reliability analysis.

3.3.5.1 Decapsulation

Ceramic packages are easily decapsulated by means of a cutting edge breaking the top off the device. Although this is a common method it has the disadvantage of introducing loose particles into the package and so possibly disguising any particles which may have induced the device to fail. To overcome this, an x-ray analysis should be carried out prior to decapsulation.

3.3.5.2 Surface Analysis Techniques

There are many surface analysis techniques available to the failure analyst[54], some of which are outlined below.

a) Secondary Ion Mass Spectroscopy(SIMS).

This technique uses ion bombardment to detect the presence of atoms at different depths into a semiconductor sample by sputtering. This technique can thus be used to give depth profiles of a given semiconductor specimen.

b) Laser Induced Mass Analysis(LIMA).

This technique uses a laser to produce a plasma at the surface of the material which can be used to analyse the atomic concentration within the sample. This technique can be used for rapid depth profiling and because of its high lateral resolution provides a means of examining impurity levels and their spacial distribution. The major disadvantage of this technique is the laser beam penetrates deep into the sample (>1μm) and is somewhat destructive.
c) X-ray Photoelectron Spectroscopy (XPS or ESCA).

Core electrons have characteristic energies which can identify a material. These electrons can be displaced using an x-ray source, and identified using an electron spectrometer.

d) Auger Electron Spectroscopy (AUGER or AES).

A sample is bombarded with low energy electrons and this releases, by ionisation, electrons with energies which are characteristic of the atoms near the surface. Detection of these electrons is similar to the XPS technique. The surface can be continuously removed by the sputtering facility available in the equipment.

e) Scanning Electron Microscope (SEM)

Scanning the surface of a material with an electron source causes secondary electrons to be emitted. These electrons are detected using an electron detector and photomultiplier which amplifies these signals so they can be output to a CRT. This instrument is ideal for identification of surface failure modes in semiconductor components.

3.4 Reliability of GaAs Devices

3.4.1 Introduction

Present results of the most extensive, published, reliability programmes to date, indicate that properly designed and fabricated GaAs MESFETs can indeed have low failure rates.

The following sections will describe the various failure modes/mechanisms reported in historical order, for low noise and power MESFETs subject to accelerated lifetest stress, electrical over-stress, and environmental stress. Radiation induced failure has been considered in section 3.2.2.4.
3.4.2 Low Noise and Digital MESFET Reliability

3.4.2.1 Accelerated Lifetesting

A number of papers have reported the results of accelerated lifetests. Several failure mechanisms have been described with their activation depending on the structure of the MESFET under stress.

One of the earliest studies on the failure of low-noise devices was reported by Abbott et al[55] in 1975. They reported on the DC accelerated lifetesting of several X-Band MESFETs with AuGe, InGeAu, NiAuGe and PtAuGe ohmic contacts. The dominant failure mode associated with these devices was metal migration of the ohmic contact in the direction of electron flow. This degradation of the ohmics caused the saturated drain current and transconductance to decrease due to the increase in ohmic contact resistance. The InGeAu ohmic contacts were concluded to give the best performance giving a MTTF of $> 10^7$ hrs.

In 1976, Kohzu et al[56] reported similar degradation effects in the $I_{ds}$ vs $V_{ds}$ characteristics but this was attributed to the creation of interface traps between the active layer and the Semi-insulating substrate.

Also in 1976, Irie et al[57] reported on an extensive programme to determine the degradation effects of lifetesting of epitaxially grown devices with Al gates and Ae-Ge/Pt ohmic contacts. High temperature storage tests between 227°C and 295°C for 1500 hrs, gate reverse bias at 150°C for 500 hrs and a high power burn-in test carried out for 500 hrs were all reported. Similar results to those found by Abbott[55] for the degradation of the drain current with time, as well as reversible drifting of the gain and noise figure were found. It was concluded that the ohmic contacts were degrading with time at a rate which was dependant on the storage temperature. An activation energy for this failure mechanism was calculated as 1.8eV which gave an expected MTTF of $3 \times 10^8$ hrs. at 100°C.

In 1978, another major investigative program was reported by Lundgren et al[58]. This program followed a approach similar to the previous studies for several combinations of gate and ohmic metals. These consisted of AuGeNi and AuGePt ohmics and Al, TiPtAu/PtAu, MoPtAu/PtAu and Cr/PtAu gates.
clear advantage was found when the AuGePt ohmic was initially tested, and because of the existing reliability literature available for the AuGeNi ohmics this combination was used in the main set of experiments. Neither of the TiPtAu or MoPtAu gates degraded significantly following 80hr. anneals at 350°C, but the Cr/PtAu gates showed considerable degradation after only 85 hrs. at 350°C. Because the TiPtAu and MoPtAu gates had a higher contact resistance than the Al gates the Al structure was retained for the main set of experiments. DC and unbiased lifetest results at 230°C and 255°C showed a degradation in the saturated drain current, and the results at 270°C showed an increase of the saturated drain current. No explanation was offered for this phenomena. The study also showed a greater degradation rate for the biased lifetest. A MTTF of 2x10^8 hrs at 100°C was calculated from only two temperatures, and an activation energy of 1.52eV was predicted for biased ohmic degradation. This value can be compared to that of Irie et al[57] who predicted a value of 1.8eV for unbiased ohmic degradation. If this was indeed the same failure mechanism, the presence of bias whilst under accelerated conditions increases the rate of ohmic degradation. A comparison of the DC and RF parameters which indicate degradation was also carried out and a good correlation was found between the change in I_{ds} and the noise figure, F_{min}.

In 1978, a further study by Lundgren[59] reported on the unbiased lifetest of in-house and commercial MESFETs. The active/buffer layers had been fabricated by LPE, VPE and ion implantation techniques. The gate contacts consisted of Al and TiCrPtAu and the ohmic contacts consisted of AuGeNi and AuGePtAu. Each device structure had a different thickness of SiO_{2} passivation. The study was very comprehensive and the overall conclusions were:

a) Several failure modes were evident. These were gold migration from source to drain, gate-source/drain short circuit, degraded gate characteristics and the formation of intermetallics at the higher temperatures.

b) The ion-implanted devices showed a lower failure rate than the epitaxially grown devices.
Degradation in the gate or channel characteristics may result from a reduction of the channel thickness or mobility caused by contact migration or interdiffusion.

This study was the also first to show that failure mechanisms other than just ohmic degradation are present in low-noise GaAs MESFETs.

Also in 1978 a major study by Irvin[60] was reported. This study used Al gates with AuPtTi bonding pads and AuPtTiAu/AuGe source and drain contacts. Aging up to 284°C was performed and two failure mechanisms were observed. These were:

a) Electromigration and intermetallic phase formation in the gate structure.
b) Gradual degradation of the channel properties.

The calculated activation energy of the electromigration and gradual degradation were 1eV. The final conclusions were that hermetically sealed devices would have a median life of 10 yrs. at 60°C yielding a failure rate of 40 FITs after 20 yrs. operation.

In 1979, Behmann[61] reported on biased lifetest results with Al gates and Al or AuTiPt gate pads. The predominate failure mechanisms for the Al MESFETs was the formation of intermetallics and voids. An activation energy of 0.56eV was calculated yielding a MTTF of 3x10⁶ hrs at 40°C. The devices with the Au gate pads showed much lower failure rates and with an activation energy of 1.5eV. This led to the conclusion that the Au devices had a MTTF 2x10⁸ hrs at 100°C.

In 1979, FrossDr[62] published the first paper in which the reliability of GaAs MESFETs was investigated using accelerated lifetesting. The devices were made with CrPtAu gates, AuGe ohmics and CrPtAu interconnect metals. Lifetesting was carried out between 150°C and 250°C. Degradation was characterised by a change in the frequency of operation and/or changes in the bias current. The results showed that the MTTF of the IC was comparable to that of a single FET and would have a MTTF of 1x10⁶ hrs at the worst case operating temperature.

In 1980, Omori et al[63] reported on the lifetest of Avantek MESFETs
with TiW/Au gates and AuGeNi ohmics. The predominant failure mode was
the annihilation and redistribution of shallow impurities in the channel area.
This was accompanied by the degradation of the series resistance between source
and drain. This failure mode is similar to that previously reported by Irvin[60]
and Lundgren[59]. The activation energy of this failure mode was calculated to
be 1.5eV yielding a MTTF of 9x10^5 hrs at 150°C. This activation energy for
channel degradation can be compared to the 1eV for Al gated MESFETs[60]
and shows the possible variation of the activation energy which is characterising
the same failure mechanism.

In 1980, Bowman[64] reported on the degradation of 9 types of MESFET
with two gate lengths and DC/RF bias applied during the lifetest. The formation
of nodules and intermetallics were the two observed failure modes. The
activation energy for the formation of the nodules was calculated to be 1.5-1.9eV
and an expected median lifetime of >9x10^5 at 150°C.

Also in 1980, Yin[65] compared the degradation properties of Al and
TiAu gated MESFETs stressed with a high DC forward bias on the gate in an
attempt to accelerate any inherent failure mechanisms. The observed failure
modes were the formation of hillocks and degradation of the channel properties.
No estimation of the activation energy or MTTF was given.

In 1983 Brydon[66] reported on the degradation properties of 2 types of
MESFETs manufactured in the U.K. The devices had Al and TiAl gates with
InGeAu ohmic contacts. Degradation of the devices was measured by the
changes in the gain or noise figure. The failure mechanisms were attributed to
electromigration and the formation of intermetallics at the higher temperatures.
The activation energy of 0.8eV for burnout was found. The TiAl gated devices
showed a MTTF of 1x10^8 hrs while the Al devices had a MTTF of 3x10^7 hrs.

Also in 1983 a paper was published by Namordi[67] reporting the
degradation of GaAs IC logic circuits. Accelerated lifetesting up to 200°C was
performed and Ag solder creep was identified as the failure mechanism. The
activation energy was estimated to be 1.6eV yielding a median life of > 10^10 hrs.

In 1985, Bresse[68], reported on the accelerated lifetesting of AuCrAl
gated devices with AuGeNi ohmic contacts. The devices were analysed using
AES to establish any diffusion related failure mechanisms in greater detail. The
observed failure mechanisms were the interdiffusion of AuCr, causing the
formation of a Au-Al₂ alloy, Ga and As outdiffusion, causing an increase in contact resistance, nickel and germanium diffusion also causing an increase in contact resistance. The activation energies associated with the four failure mechanisms, with no applied bias, were 0.64eV, 0.92eV, 0.76eV and 0.5eV. The MTTF for each of the four mechanisms were 3x10⁶ hrs, 6x10⁹ hrs, 3x10⁸ hrs and 3x10⁶ hrs respectively. The values reported in this paper are lower than previously reported for similar structures but the failure criteria adopted in this paper was far from catastrophic. After comparison with the biased lifetest results it was concluded that biased lifetesting accelerated any inherent failure mechanisms, except for the diffusion of Ge which appeared to be inhibited by the drain/source bias.

Another paper published in 1985 by Sethi et al [69] reported on the differences in the degradation properties of Al and CrAl gated structures concentrating on current induced electromigration. The activation energy was calculated to be 0.61eV for the Al structure and 0.16eV for the CrAl structure. The difference in the measured activation energies between the two structures was attributed to the smaller grain size and number of grain boundaries in the CrAl metallisation.

Other papers related to the failure mechanisms in low noise MESFETs can be found in refs. [70-74].
3.4.2.2 Electrical Overstress

Electrical overstress in low-noise MESFET devices comprises of constant voltage, RF or electrostatic discharge pulse damage to the gate, source or drain. The main papers reporting the various conditions for damage to occur, and the various parameters which characterise failure, are discussed below in historical order. Where no details of the device structures are given they have already been discussed in section 3.4.2.1.

The first paper to describe the effects of pulse degradation on GaAs MESFETs was published in 1975 by Bellier et al[75]. They used a technique based on the "human body model" reported in section 3.2.2.4.1. but omitted the 1.5Kn "body resistance". The devices had suffered sequentially increasing positive or negative pulses applied to the 2μm Al gate. Beginning at 5x10⁻⁹ Joules, the input energy was doubled with each sequential step. In many cases the observable damage was on the surface of the devices with no increase in leakage current. Two effects were recorded for positive polarity pulses. These were:

a) A transient increase in drain-source current as a result from a decreased depletion layer width.

b) A transient current of 1A for 1ns from gate to ground at 200V charging voltage.

Failures were found to occur at the lowest resistance paths between the gate and source contacts and at high resistance points on the gate. For negative polarity voltages, failures were found to occur at points of lowest breakdown voltage. It was found that a device could be subject to sub-threshold pulses and still operate within specification.

Abbott et al[55], in 1976 described the degradation of the Al gate diode when subjected to a set of sequentially increasing voltage spikes from a T-R cell. Two sets of experiments were carried out on devices: unbiased and with high reverse bias on the gate. When the biased devices were subjected to the spike test the noise figure showed no change until the device failed altogether. The mean energy for failure was found to be 0.3 erg/spike. A correlation was found
between failure sites and manufacturing defects such as irregularities in the gate metallisation. It was found that the burnout energy could be increased by almost a decade using a refractory gate metal.

In 1976, Irie et al[57] reported on similar experiments related to burnout induced by rectangular pulses on the gate and drain of a device. In both cases the drain electrode was subject to a +2V bias. The gate-source diode received negative polarity pulses from 1us to 100us duration. The critical voltage was seen to rise gradually with decreasing pulse width. However the drain-source channel received pulses of a similar duration little change in threshold voltage occurred over the time domain under investigation. Breakdown was characterised by burnout between the electrodes and the failure site was again correlated to edge non-uniformity of the electrodes.

Lundgren[58] in 1978 used the "human body model" without the 1.5Kn "body resistance" to assess the pulse susceptibility of MESFETs with Al and Au refractory gates. For positive polarity voltages the Al devices required 70-78V with the corresponding energies of 2.5 to 3 ergs. The refractory gates required only 42-65V for failure, and showed changes in the electrical characteristics prior to failure. For negative polarity pulses the Al devices failed at -40V at 0.8 ergs. The failure point in all the devices occurred between the gate and ohmic contacts based at the high field points.

In 1979 Whalen et al[76] reported on the RF pulse degradation characteristics of MESFETs with Al, TiPtCrAu and TiPtAu gates with AuGeNi, InGeNi and AuGePt ohmics. The stressing consisted of pulsing the devices with RF pulses at 9.3GHZ of various durations. Two failure modes were observed. They were a short circuit path (5-25n) characteristic of 10ns pulses and massive channel damage/reduction in Idss which was characteristic of 1.5ns pulses. All devices were found to have similar burnout energies (between 0.2 to 0.6 ergs).

In 1979, Huang et al[77] reported on the pulse sensitivity of low noise devices using the modified form of the human body model as used by Bellier[57] and Lundgren[58]. The human body capacitance was varied between 100pF and 1µF and the changes in the positive and negative threshold energies were calculated. Negative polarity pulses tended to require lower energies to initiate burnout than positive polarity pulses (0.25µJ at 90V to 0.6µJ at -70V). The gate leakage current was found to be the most sensitive parameter indicating
In 1982, Whalen et al [78] published a further paper on the effects of a single RF pulse on the degradation of low-noise MESFETs. The structures were similar to those reported in his earlier 1979 paper [76]. Devices were subject to bursts of RF power of durations between 1μs and ≈100ms. The incident and absorbed power were measured at burnout and the results showed that the incident failure power was essentially constant over the examined time domain. He plotted his previous results on the same graph and the results showed that the incident failure power increased at pulse lengths less than 10ns. The roughly linear increase in absorbed failure power at burnout, after 10ns indicates that the failure threshold has already been reached at 10ns and the excess energy is probably contributing to the size of the failure site. The results presented in this paper are similar to the EOS results reported in this thesis.

In 1985 Bresse [68] reported on the sensitivity of low-noise structures to rectangular pulses on the drain. Failure was caused with a pulse of 16V and 170μs duration. The device showed degradation in $I_{ds}$ which was correlated to an outdiffusion of the Ga and As into the Cr layer.

In 1986 Rubalcava et al [79] reported on the degradation effects of ESD pulses based on the MIL STD model [48,50] described in section 3.2.2.4.1. on GaAs MESFETs. The pulse was applied to the gate, source or drain with the other contacts earthed. Several important effects are described in this paper. The MESFETs, which had TiPtAu gates and AuGeNi ohmics, proved to be the most sensitive element studied, with the gate width being the most important parameter relating to ESD sensitivity. Another interesting observation from this study is that sub-threshold pulses showed improvements in some DC characteristics, a result also reported in this thesis. The threshold levels for the MESFETs of similar structure to those used in this present study were +1100V and -300V to cause a 10% change in reverse breakdown voltage. MESFETs with the gate in the centre of the channel between the ohmics, showed symmetric ESD sensitivity. A final result, which is considered important related to the results reported in this thesis, is the fact that the ESD sensitivity was related to process maturity. They reported that MESFETs fabricated only a year before had half the ESD sensitivity as the recently fabricated devices.

In 1987 the present author published a paper relating to the degradation
effects of ESD pulses on the MESFET structures[80]. It was shown that a number of near threshold pulses, would eventually cause burnout and will degrade the transconductance of a MESFET whilst keeping the saturated drain current constant. This effect is probably related to the creation of a short circuit path between the gate and source electrodes. The effects of burnout between each electrode were examined and the subsequent changes in the $I_{ds}$ vs $V_{ds}$ characteristics were linked to the magnitude of the gate-ohmic resistive path subsequent to each pulse. Pulse polarity effects on ESD sensitivity were also reported and linked to the action of the schottky depletion region under ESD stress.

In 1977, Buot et al[81] published a paper on an experimental and theoretical study into the subsurface burnout and ESD effects in GaAs MESFETs and HEMTs using the human body model[48,50] and the charged device model[49]. Three types of MESFET were used in the experiments. The gate metals were TiPtAu and TiW Au with gate lengths of between 0.7μm to 1.1μm. Burnout was postulated to follow the following pattern:

The first event is when a deep-level traps-enriched(DLTE) region which has a high temperature coefficient region(PTCR) within the device is heated to a high enough temperature(\( \approx 550^\circ C \)) for thermal runaway to take place in the presence of an electric field. This happens when this region is at or in the vicinity of the hot-electron distribution, with local electron temperature roughly \( 2000^\circ C \) and the local electron density is roughly \( 10^{17} \) cm\(^{-3} \). The PTCR is usually the buffer/substrate region of the device and possibly the AlGaAs region of a HEMT.

The second supplementary event is when the heated PTCR bridges two regions of high electrical conductivity with different potentials. For GaAs FETs, this can happen when metallic filaments of high current density extend deep into the substrate. The filamentary extension is an accumulative process arising from hot-electron induced (and/or strong gate current surges driven) metal GaAs interdiffusion starting at the weak spots of the ohmic metallisations.

The initial action of the thermal runaway process is a current discharge and constant localisation within the PTCR bridge leading to a situation of exponential charge build-up. Current and temperature will build up locally with
the PTCR bridge until they are limited by resistive drops in other parts of the transistor or the heating causes a drain-gate or gate-source short circuit. Melting is therefore postulated to be mainly below the surface with the upper active layer acting as a cap.

In 1988, Rubalcava et al[82] reported a further study on the effects of "human body model" ESD pulses on digital MESFETs in IC's. The MESFET structures were similar to those reported in his 1986 paper[79]. The study concentrated on the effects of sub-threshold pulses on the final threshold voltage. No particular sensitivity to ESD pulses was observed for GaAs IC's pulses under the threshold. The prior history of a structure's ESD exposure had no effect on the final threshold. GaAs IC structures were concluded not to be susceptible to latent failure degradation from ESD pulses. These conclusions tend to contradict to his previously reported results in which he stated that "MESFETs that failed after many pulses tended to have the highest thresholds. This would indicate that short term cumulative effects tend to harden devices". The possible reasons for this may be that the IC structure as a whole must be dissipating the power through many devices, hence any single device would not receive enough energy to cause degradation or the devices contained within the structure contain a low number of defects allowing a sub-threshold pulse to be easily dissipated within the structure because no localised regions of high current density would be present.
3.4.2.3 Environmental Stress

The number of reported studies of the effect of the environment on MESFET failure rates has is limited. The reported failure modes for most the papers are similar and require precise conditions for the associated failure mechanisms to operate.

The first paper to investigate the effect of temperature and humidity of the degradation of MESFET devices was published by Irvin[49] in 1978. An 85°C/85% relative humidity atmosphere was used in conjunction with a -6V gate bias on uncapped devices with Al gates and AuPtTi bonding pads. After two hours electrolytic corrosion was evident on the gate. This corrosion was only present when the device was under bias. This paper also reported on the corrosion of similar hermetically sealed devices under the same conditions. This was attributed to unremoved photoresist harbouring the impurities necessary for corrosion.

In 1978 Anderson Jr.[83] reported on degradation rates in the presence of high relative humidity and ionic contamination. Temperature cycling was used to accelerate the failure mechanisms for both passivated and unpassivated devices with Al and Au gates. The devices were cycled between -10°C and +100°C, at 95% RH, in the presence of Na and Cl ions. Several sets of device were used with various gate and drain bias. Al gate corrosion was evident in the hermetic and non-hermetic biased devices after only 80 hrs. of cycling. The non biased devices showed only a slight increase in gate current for the same number of cycles. The Au gate devices were found to be much less susceptible to the same cycling conditions.

In 1980, Bowman[64] reported on the environmental testing of 8 types of MESFET with two gate lengths. The tests included temperature cycling, random vibration and mechanical shock. No failures were observed from hermetically sealed devices. The only failure was found during the random vibration test, where a drain/source short circuit occurred. This was found to be due to the fracture of the GaAs chip.

In 1983 Brydon[66] reported on the effects of temperature cycling on the degradation properties of two types of hermetically sealed MESFETs manufactured in the U.K. The devices had Al and TiAl gates with InGeAu
ohmic contacts respectively. Each of the devices were subjected to 10 cycles of -65°C to 125°C with the extremes maintained for 10 minutes. No failures or degradation were observed.

In 1985, Bresse[68] reported on the environmental effects on unpackaged devices with AuCrAl gates and with AuGeNi ohmic contacts. The conditions of 95% humidity and 50°C stress and -1V bias on the gate caused catastrophic failure of the gate within 2 hours. This was preceded by a rapid increase in gate current which was also reported by Anderson Jr.[83]. Lowering of the stress conditions to 27°C and 65% RH had little effect on the device characteristics measured over 100hrs.

3.4.3 Power MESFET Reliability

3.4.3.1 Accelerated Lifetesting

The first paper relating to the accelerated degradation properties of GaAs power MESFETs was published by White et al[84]. The devices had Al gates and InGeAu drain and source contacts. Lifetesting was performed at temperatures between 160°C and 220°C, with DC bias applied to the drain of the devices. Al and Au bond wires were used to test the effectiveness of each material under the high power operation. Degradation of the transconductance, $g_m$, was observed with a failure criterion defined as 10% change in that parameter. Failure, in the Al-Au bonds, was characterised by the formation of voids along the gate and it has since been suggested that electromigration was the cause even though the current density was two orders below that previously associated with this failure mechanism.

Further work on the effect of the bonding material was reported by White in a paper in 1979[85]. In this study both Al and Au bond wires were again used, and electromigration induced void formation was found to be the cause of failure. The activation energies of this failure mechanism were 0.6eV and 0.67eV for the Al and Au bond wires respectively.

In 1978, Macpherson et al[86] reported on the first study using full RF drive whilst under an accelerated lifetest. The devices had multiple Al gates and AuGeNi ohmic contacts. Au bonding wires were used in preference to Al.
During the lifetest, the devices were subject to input power variations from 150mW to 500mW and the channel temperatures were estimated to be between 120°C and 130°C. A large number of the devices exhibited sudden drops in output power during the tests and EBIC examination of the surface revealed that voids had been created. The gate current during the tests was estimated to be in the order of $10^7$ A/cm². This led to the conclusion that electromigration was the cause of failure.

A further paper in 1979 by Cohen et al[87] examined the effects of multiple TiWAu gates on the degradation characteristics of X-Band power MESFETs. The tests were carried out between 180°C and 225°C and various DC parameters, and the C-V characteristics were measured at different times during the test. Roughly half of the devices failed catastrophically during the test and the rest degraded gradually. Failure analysis revealed that no voids were present in any of the structures and little change in the majority of the DC parameters and C-V data was evident. The only real evidence of degradation was an increase in the gate leakage current. The degradation of the metal-semiconductor interface was ruled out but no explanation for this failure mechanism was proposed. The activation energy was calculated to be 2.3eV yielding a MTTF at 100°C of 2x10⁸ hrs.

Also in 1979, Drunkier et al[88] reported on a study on hermetically sealed TiPtAu gate, and AuGeNi ohmic devices. Two studies were carried out to ascertain the MTTF and failure mechanisms characteristic of production devices. The two tests were carried out between 140°C and 250°C with zero bias, and drain current bias applied. In the zero bias tests, the failure mode was identified to be gate pad interdiffusion. For the DC bias tests void formation at points of high current density and electromigration of the drain fingers was identified. The activation energy of the unbiased failure mechanism was 1.04eV, yielding a MTTF of $>10^7$ hrs at 150°C. The activation energy for the biased test was 1.85eV, yielding a MTTF of 5x10⁶ hrs at 125°C. This study was the first to report void formation using refractory gate systems.

In 1980 and 1982, Fukui et al[89,90] presented the results for a major study into the degradation characteristics of multiple, recessed, Al gate structures, with AuGeAgAu ohmics and Si₃N₄ passivation. Two lifetest studies were carried out at 150°C, 120°C and 250°C, one with 14V DC bias applied to the drain and
the other at 210°C and 250°C with RF gate drive and DC bias. No catastrophic failures were found in over a million hours of testing. Gradual degradation in $I_{ds}$ and the output power, $P_o$, were observed and the rate of degradation was dependent on temperature and appeared to be independent of RF drive. No changes were found to the metal-semiconductor interface properties and the failure mechanism was postulated to be degradation of the channel saturation velocity. The activation energy associated with this was estimated to be 1.9eV yielding a MTTF of $7 \times 10^8$ hrs at 110°C.

Also in 1980, Jordan et al[91] reported on a large scale study into burnout failure in GaAs MESFETs. The devices had 12 Al gates and AuGe-Ag-Au-Ti-Pt-Au ohmic contacts with SiO$_2$ passivation. The tests were conducted between 150°C and 250°C unbiased, DC bias(+14V-drain) and DC(+14V-drain) and RF bias. Failure was defined as a sudden change in one of the DC characteristics and devices with soft gate characteristics were categorised as degradation failures. A comprehensive statistical analysis was carried out using the lognormal distribution function which found the burnout statistics had confidence limits up to 90%. An Arrhenius analysis revealed that two mechanisms were operating in the temperature range under consideration. The first mechanism had an activation energy of 0.85eV in the temperature range $160°C < T < 208°C$ and 1.65eV in the temperature range $208°C < T < 265°C$.

In 1983, Katsukawa et al[92] reported on a study using devices with Al gates. The study was carried out between 250°C and 337°C with zero, DC bias and RF bias. Three failure modes were evident. One was described as a "non pinch-off phenomenon", the second was $I_{ds}$ degradation and the third was burnout. The first failure mode which was present during both bias tests was attributed to electromigration. The second failure mode which was present during the zero bias test was attributed to degradation of the ohmic contacts. The final failure mode was considered to be the final stages of the previous two failure mechanisms. The activation energies of the two degradation mechanisms were calculated to be 1eV and 1.8eV yielding MTTFs of $1 \times 10^6$ hrs and $3 \times 10^7$ hrs at 130°C. Bases on the results from this study several improvements were adopted to the basic MESFET structure. These were:

a) A TiAl gate metallisation which would suppress electromigration
b) A deeply recessed gate structure which has been previously shown to increase the gate/drain DC breakdown voltage.

c) A new lift-off technique which does not use photoresist can be used to give a better quality Schottky barrier.

This structure was fabricated and was assessed to have a MTTF of $1 \times 10^7$ hrs., a decade better than conventional power MESFETs.

In 1983, Slusark et al[93] presented a paper on the degradation effects of Fujitsu FLC-30MA Al gated power MESFETs. The lifetests were carried out at 190°C and 215°C under DC and RF bias. The failure mechanisms were found to be source-drain and some gate electromigration. Electrical degradation was found to be gradual, and the devices showed a decline in output power with time. The gate resistance was used as a screening parameter, and high initial values of resistance had a lower MTTF during the DC bias lifetests. This effect was shown to be wafer dependent, and directly related to the average gate resistance for a given wafer. The activation energy of this the primary source-drain electromigration was calculated to be 0.6eV, yielding a MTTF of $9.5 \times 10^5$ hrs.

In 1983, White et al[94] published a paper describing the degradation effects on submicron Al gate MESFETS subject to severe RF and DC overdrive. Two failure modes were observed depending on the channel temperature and appeared to be unrelated to the RF drive. At 228°C a gradual degradation in gain was observed, accompanied by a drop in $I_{ds}$ and no gate degradation was observed. This failure mechanism, attributed to channel degradation, had a MTTF of 2100 hrs. At 280°C all the failures were catastrophic in nature with a calculated MTTF of 120 hrs. It was postulated that the high temperature failures were caused by a different failure mechanism than the lower temperature degradation.

A study of the effects of 0.5μm Al, TiAl and TiAlTi gate metallisations on the reliability of power MESFETs was reported by Katsukawa et al[95] in 1984. The tests were carried out between 240°C to 300°C channel temperature and under DC bias only. The dominant failure mechanism for the Al devices was gate metal disconnection, for the TiAl devices catastrophic burnout, and for the TiAlAu devices degradation in the gate breakdown voltage was observed. The
gate metal disconnection was attributed to be due to Al electromigration and the
decrease in gate breakdown voltage was due to the interaction of the Ti and Al
with the GaAs. The catastrophic failures in the TiAl devices occurred after much
longer times than observed for the other devices and it was concluded that this
structure was the most reliable.

In 1986, Canali et al[96] reported on the degradation of TiWAu gated
devices subject to DC, RF bias, and high temperature storage. The common
electrical failure mode, in all tests, was a decrease in \( I_{dss} \) and \( V_p \) and an increase
in \( R_{on} \), the channel resistance. Auger analysis of the devices showed that the
degradation was due to the "sinking" of the Au gate metal into the channel. This
failure mechanism maybe the advanced stages of net-donor compensation,
because Au is known to be a deep acceptor in GaAs.

Also in 1986, Russell et al[97] reported on lifetesting results using multiple
TiWAu gates with AuGeNi ohmic metallisation. These devices were subjected to
RF drive at levels associated with normal operation, and high temperature
storage to identify the temperature dependent mechanisms. The majority of the
population failed due to voids in the gate metal. The major conclusion from this
study was that devices that were RF biased during lifetesting, had a higher failure
rate than DC biased devices in a similar test. This is contradictory to the earlier
results by Fukui[77,78] and White[82]. The difference may be attributed to
inaccuracies introduced by the unknown real channel temperature.

In 1987, Canali et al[98] presented a further study on the accelerated
diffusion characteristics of Al gate MESFETs subject to high temperature
storage, DC drain bias and DC gate bias. Several electrical failure modes were
evident. A decrease in \( I_{dss} \) was evident at temperatures higher than 150°C in all
the tests. A "non pinch-off condition" and an increase in the gate series resistance
were also evident in the forward bias gate test. The "non pinch-off condition"
effect is similar to that reported by Katsukawa[80] in 1980. The decrease in \( I_{dss} \)
was attributed to the increase in barrier height at the junction due to the
formation of a \( \text{Al}_x\text{Ga}_{1-x}\text{As} \) \((0 < x < 1)\) layer under the gate contact. The increase
in gate resistance and the "non pinch-off condition" effect was attributed to
electromigration in the gate fingers causing them to become open circuit and
leaving a portion of the channel open to current regardless of the voltage applied

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to the gate.

Other papers related to the failure mechanisms in power MESFETs can be found in refs. [99-103].

3.4.3.2 Electrical Overstress

The first paper describing the pulse degradation characteristics in power MESFETs was published in 1978 by Yamamoto et al[104]. In this paper they described the effects of the structure on DC bias light emission and pulse breakdown characteristics. The results can be summarised as follows:

a) When a positive drain bias and a zero gate bias was applied to the structure, white-yellow light emission was observed at the drain edge at the edge of the active region. The light intensity was greater for the unrecessed devices.

b) When the gate bias increases the light emission decreases to near zero and again increases when the gate begins to breakdown.

c) When the gate breaks down light emission occurs at the gate edge for all types of device.

d) Near the pinch-off condition burnout is initiated inside the active or buffer epitaxial layer.

e) Positive polarity pulse stressing at the drain initiates burnout at the drain edge for zero gate bias.

It was suggested that under pulse and DC stress source/drain burnout begins at the drain edge of the active region when the gate bias is 0V and inside the active/buffer layer when the gate was near pinch-off.

In 1981, Frensley[105] published a paper which described an analytical model to assess the depletion layer configuration under bias. The model correctly predicted that source/drain breakdown begins at the drain side edge of the gate and the breakdown voltage is inversely proportional to the product of the doping level and the active layer thickness. The possibility of surface depletion regions between the gate and ohmic contacts controlling the breakdown characteristics
was discussed and a model predicting the effects of a gate recess on the device breakdown characteristics was proposed.

In 1983, Anderson Jr. et al.[106] described the various failure modes present when GaAs power MESFETs are subject to high power RF pulses, to the gate, of various duration and number. This work was similar to that reported by Whalen[60,62] for low noise devices. Three types of device structure were analysed. The gate lengths were 0.8μm to 1.1μm, gate metallisations were Al or TiWAn and the active layers were ion-implanted or VPE material. The gain(G), noise figure(NF), I_d vs V_ds and Igs vs Vgs characteristics were all measured after the pulse event. In general devices with Al gates showed a gradual degradation by an increase in NF accompanied by a decrease in I_ds. The TiW gates degraded by an increase in NF and a very little change in I ds. Failure analysis showed that in the Al device the primary cause of failure was electromigration from the gate to the source contacts, initiated at irregularities along the gate. The TiW devices also showed this failure mode but to a lesser extent. The formation of voids in the channel appeared to be the cause of failures in these devices. It was concluded that the devices with TiW gates were less sensitive to pulse burnout than devices with Al gates.

In 1985, Immorlica et al.[107] described the modes of catastrophic failure for GaAs power MESFETs subject to DC bias stress between the drain and source, while the device was pinched-off. They used a number of structures including a FET which was passivated with polyimide. This passivation has been used on the devices reported in this thesis. An ultra fast circuit breaker, operating in less than a 1μs was used to prevent massive damage and to localise the failure site. The primary failure mode was a transverse trench between the gate and drain contacts that grew deeper and wider as the short circuit current continued to flow. A secondary failure mode was observed in ~20% of the polyimide coated devices which took the form of a symmetrical source-drain crater. This failure mode was not catastrophic since the gate could still control the drain current after failure, but the device could not be fully pinched-off. The primary failure mechanism was postulated to be a result of gate-drain avalanche initiated on or near the surface. The secondary failure mode was attributed to defects or contamination in the dielectric or at the semiconductor surface.
3.4.3.3 Environmental Stress

No papers relating directly to environmental stress related to GaAs power MESFETs have been found.

3.5 Summary

This chapter has outlined the various failure mechanisms associated with many semiconductor devices. A detailed literature survey has also been presented with reference to the reliability of GaAs MESFET structures. The reported failure mechanisms associated with these devices are summarised as follows:

a) Ohmic contact degradation has been reported in many structures with various gate and ohmic metallisations. This failure mechanism would cause the average drain current and transconductance to decrease.

b) Channel degradation caused by donor compensation and the indiffusion of the contact metals. This again would tend to decrease the average drain current and transconductance.

c) Electromigration of the contact metals, tending to cause the gate to go open circuit. This mechanism would eventually cause loss of gate control, thus not allowing the device to pinch-off.

d) The formation of intermetallics, most commonly found in devices with Al gates. This mechanism would be identified by the formation of voids in the contact metals tending to decrease the channel current.

e) Electrolytic corrosion can be a cause of failure provided moisture, DC bias, and a catalyst are present

f) Accelerated stressing under DC bias has been found to increase the degradation rate of many failure mechanisms. Stressing under RF bias
does not increase the degradation rate further than with DC bias stressing alone, though this is not conclusive.

g) Multilayer refractory metal gates tend to have lower degradation rates than simple metal gates such as Al.

h) Pulse\ESD burnout has been postulated to occur at points of high electric field/current density and also related to manufacturing defects in the metallisation. Failure is normally exhibited by degradation in the I\V characteristics. Pulse failure thresholds are related to gate geometry, contact metallisation, process maturity, and pulse polarity.

The literature to date on the reliability of GaAs MESFET devices is quite substantial and has tended to concentrate on the degradation of a device due to the activation of long-term failure mechanisms. In a limited number of papers square pulse\ESD burnout has been studied and a number of qualitative models proposed. Experimental verification of these models are generally based on the changes in the device electrical or physical properties subsequent to a pulse, which is normally catastrophic and regarded as thermal in nature. No literature is available of the changes in device electrical properties during a pulse event. Hence, the measurement of the current, voltage and power waveforms during a pulse event will allow a better understanding of the breakdown mechanisms and will also yield accurate times-to-failure. Using this information the data can then be analysed using semiconductor thermal breakdown models.

### 3.6 References


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CHAPTER 4

EXPERIMENTAL STUDY

4.1 Introduction

It has been established in the literature survey that little work has been published assessing the parameters which affect the sensitivity of GaAs MESFET structures to ESD type pulses. The only physical model for breakdown has been presented by Buot[1] et al who postulated that burnout due to EOS and ESD pulses probably initiated near the active layer-substrate interface and was dependant on the interface reaching \( \approx 550^\circ \text{C} \), at which point substrate conduction caused localised current filaments to form and burnout to occur. Hence, in order to gain a greater understanding of the parameters which characterise breakdown in MES structures, the experimental study presented in this thesis focuses on the degradation and burnout characteristics of GaAs MESFET and MES diodes subject to exponentially decaying ESD pulses. Particular emphasis has been placed on the physical mechanisms underlying breakdown. The experimental work specifically addressed the following areas:

a) A study of the effects of the pulsing system on the magnitude and shape of the current and voltage waveforms to which a device is subjected during ESD stress.

b) A study of the standard DC characteristics of the GaAs MESFET and MES diode structures.

c) A study of the degradation effects on MESFET and MES diode I/V characteristics due to ESD pulse(s).

d) A study of the effects of ambient temperature and AutoZap(discharge) capacitance on the ESD breakdown threshold of MES diodes.
e) A study of the visible burnout/degradation modes associated with ESD pulses.

f) A study of the sub-threshold/failure voltage and current waveforms associated with MES diode ESD breakdown.

4.2 The GaAs MESFET Structures

4.2.1 Introduction

The devices used in the experimental study were resident on 3 wafers supplied by the original project sponsors Standard Telecommunication Labs, Harlow, Essex. These wafers were part of a process characterisation contract and the detailed fabrication details were not available. The study on MESFET degradation was carried out on the E552 wafer and the later studies were carried out on the I69X and I69W wafers. The I69X and I69W wafers were fabricated with the same mask set and were regarded as identical except for the variations in n-type layer depth. The E552 wafer used a similar mask but had larger dimensions.

4.2.2 Wafer Details

The devices were present on two 2" <100> DOWA LEC wafers with substrate resistivities of ~1500 ohm per square. Each wafer had 1500 FET structures with AuGeNi source/drain contacts and CrAu gates. Figs. (4.1) and (4.2) show schematic cross-sectional and plan views of the I69X and I69W structures. The I69X and I69W devices had gate-source and gate-drain distances of 1µm and 2µm respectively. The gate length and width were 1µm and 150µm respectively. They had been ion implanted with Si atoms at an energy of 80keV at 2.5x10¹² cm⁻² and received a thermal pulse anneal with a silicon nitride cap(300-400Å) at 1000°C for 8 seconds. The devices were proton isolated at an energy of 50keV at 2x10¹³ cm⁻². All devices were passivated with polyimide and annealed at 100°C for 30 minutes. The E552 wafer had gate-source and gate-drain distances of 1.5µm, though many devices had the gate contact shifted toward the source contact.
Fig. (4.1) GaAs MESFET Cross-sectional View

Fig. (4.2) MESFET Plan View
This was traced to mask misalignment. The gate length and width were 1\(\mu\)m and 150\(\mu\)m respectively. A typical 2" GaAs MESFET wafer is shown in fig. (4.3). Also present on the wafers were ohmic contact test patterns which could be used for the measurement of contact resistance, \(R_c\) and ohmic transfer length, \(L_t\).

### 4.2.3 Wafer Homogeneity

In order to accurately measure the statistical breakdown thresholds of any device structure, the sample of devices must be identical. Due to the immaturity of the technology, variations in many of the DC characteristics were evident. The wafers had been fabricated in 1982 as part of an MOD characterisation programme[2] and had variations in the DC properties across each wafer. These variations were manifested in the changes of the MESFET pinch-off voltage \(V_{p}\), saturated drain current \(I_{ds}\) and transconductance \(g_m\). Hence, in the experimental work, devices were selected with pinch-off voltages within \(\pm0.2V\) of the mean value for the wafer. Where possible these devices were selected in a similar areas of the wafer for a given experiment. In order to eliminate any contamination effects the wafers were stressed with a 100°C temperature screen for 15 minutes before any experiments were carried out.

### 4.3 Stress and Measurement Apparatus

#### 4.3.1 Introduction

An experimental system consisting of probing equipment, pulsing apparatus and characterisation equipment was set up for ESD stressing of the MESFET/MES structures.

#### 4.3.2 The Wafer Microprober

The manual wafer microprober is shown in fig. (4.4). The wafer is placed on a smooth metal chuck and held in place by vacuum suction.
Fig. (4.3) GaAs MESFET Wafer

Fig. (4.4) The Wafer Microprober
The chuck could be electrically heated to an accuracy of ±5°C using an RS 348-144 thermostat, a Ni/Cr Ni/Al thermocouple and four 1 ohm resistors embedded in the chuck. The complete chuck assembly could be left floating or grounded as required.

A stereo optical microscope incorporated in the microprober allowed detailed visual analysis to be carried out with the magnification range from 50 to 1500 times. Illumination was available using a through-the-lens system and could be turned-off if required. The complete assembly could also be covered to allow the experiments to be carried out in the dark.

The devices were probed using 12.5μm Wentworth probes which were held in place by a magnets attached to the base of the probe assemblies.

4.3.3 ESD Pulsing Apparatus

4.3.3.1 Manual ESD Apparatus

The initial study on MESFET degradation used a simple ESD "zapper" designed at LUT. This consisted of the basic "human body" circuit elements outlined in section 3.2.2.4 with two mercury wetted relays to switch between the charge and discharge circuits. This was connected to the probes using low resistance flying leads. This apparatus could not be used to stress devices above ±1000V, because this exceeded the breakdown specification of the relays.

4.3.3.2 AutoZap ESD Apparatus

The later experiments on MES diodes used a commercial instrument called the AutoZap. This instrument was originally designed by British Telecom Research Labs, U.K for a study into the ESD threshold variations in MOS structures[3]. This instrument is capable of delivering very reproducible ESD waveforms up to 4kV with less than 10ns rise time into a 1500Ω load. Such apparatus is necessary to provide reproducible pulses for ESD sensitivity analysis[4-6]. The instrument can be programmed, using a Commodore computer to provide a single pulse, or provide sequentially increasing pulses, until a preprogrammed change in the I/V characteristics, between -10V and +1V, has
been attained. This change could be as little as 2µA, or as large as 20µA. The original instrument had been designed for packaged devices, and had a number of "testboards" available. These testboards could allow devices with 60 pins, or more, to be pulsed with a identical ESD waveform. The AutoZap was connected to the probes via either an earthed coaxial system or flying leads.

4.3.4 Parametric Analysis

4.3.4.1 Analogue Curve Tracer

The initial study on MESFET degradation used a Telequipment Ct1 curve tracer to analyse the changes in the MESFET $I_{ds}$ vs $V_{ds}$ characteristics. Drain-source current, $I_{ds}$ measurements could be made down to $10\mu A/cm$ with up to 12 gate-source voltage, $V_{gs}$ steps. The gate-source voltage steps could be in the range ±0.1V to ±2V. Drain-source, $V_{gs}$, voltages were be applied in the range ±0.1V to ±5V. A series limiting resistor of 1kΩ was added to protect sensitive devices from accidentally being overstressed. The curve tracer was connected to the device with earthed 50Ω coaxial leads, connected directly to the probes.

4.3.4.2 Hewlett Packard Parametric Analyser

The later studies used an HP4145B parametric analyser to assess changes to the diode, $I_{gs}$ vs $V_{gs}$ characteristic, or the MESFET $I_{ds}$ vs $V_{ds}$ characteristics. The accuracy of these measurements was limited only by the noise in the system and could easily measure down to 10mV and 10nA. The instrument also had a programmable voltage/current limiting feature which allowed strict controls of the current/voltage present under any conditions of bias. In the initial experiments using the full MESFET structure this limit was set to 1mA, $I_{gs}$. In the later experiments, using MES diodes, this was set to a limit appropriate for each experiment. The analyser was connected to the device using the HP2010 test fixture and earthed 50Ω coaxial leads connected to the probes. Ferrite beads were added near the device to eliminate device oscillation during characterisation[6,7]
4.3.4.3 The Wayne Kerr LCR meter

Capacitance and static resistance measurements were made using the Wayne Kerr 4210 LCR bridge. This instrument could accurately measure capacitance, resistance and inductance values at 1 and 10kHz to 0.01n, 0.1pF and 0.1uH respectively. This instrument could be trimmed to compensate for any voltage drops in the measurement leads. The author adapted this instrument by adding a variable DC voltage source in order to measure the Capacitance-Voltage characteristics of the MES diodes. These measurements used the Wayne Kerr meter in conjunction a BBC microcomputer and a Keithley 230 voltage source. The voltage source provided the DC bias from 0 to -2V, and the Wayne Kerr meter used a 10kHz, 0.25V sinewave superimposed on the DC signal to measure the capacitance. The data was digitised using an IEEE system and could be plotted on a standard printer in graphical form. The complete suite of programmes are listed in Appendix 1. The programmes are flexible and with little adaptation could be used with any IEEE controlled C-V bridge such as the HP 4191A.

Fig. (4.5) C-V Characterisation Plots

This system was limited due to the low frequency of operation and large measurement signal used by the bridge. Characterisation of this set-up is shown in fig. (4.5). This shows the C-V plots for a large area GaAs device using a
commercial C-V bridge at 100kHZ and 1MHz, compared to the Wayne Kerr measurements at 10kHZ. The results show the Wayne Kerr measurements are significantly different to those of the commercial bridge. This highlights the need to measure C-V characteristics at 1MHz in order to get accurate plot of the doping profile. Hence, the Wayne Kerr apparatus was only considered useful for large changes in device capacitance.

4.3.4.4 Waveform Analysis

The author set up a system to measure the current and voltage waveforms present during an ESD event. This system consisted of an HP 54111D 1GHz digital oscilloscope with a HP10440 10MΩ, 3pF voltage probe across the device and a Tektronics CT1 Hall effect current probe connected around the input lead directly next to the device. These probes allow the waveforms to be measured with the minimum load on the pulsing system. The oscilloscope was connected to an IBM desktop computer via an IEEE control card which was used to programme the oscilloscope and transfer data into the computer. The complete stress and characterisation system is pictured in fig. (4.6) and as a block diagram in fig. (4.7).

Fig. (4.6) ESD Stress and Measurement System
Fig. (4.7) Block Diagram of the Stress and Measurement System
The HP54111D oscilloscope can be programmed to capture the waveforms generated during ESD event. The raw data is stored as 501 bytes, each byte represents a single quantised level between 0 and 255. This data also requires 6 parameters which allow the correct scaling to be applied to each waveform. The digitised data from an ESD pulse and the scaling parameters were downloaded onto a 5.25" floppy disc and/or directly into the MathCad/Lotus 123 software packages. The data is then reconstructed into real currents and voltages and plotted in graphical form. Using this technique the current, voltage, and power waveforms could be plotted as a function of time, or mathematical operations, such as the reconstruction of the $I_{gs}$ vs $V_{gs}$ characteristic, performed on the data. The data capture/transfer programmes are shown in Appendix 1.

### 4.4 System Characterisation

It is likely that the characteristics of the pulse transmission system(s) will effect the shape and magnitude of the pulse a device would receive during an ESD event. Therefore a series of experiments were carried out to assess the effect of the two transmission mediums on the pulse waveforms derived from the AutoZap pulsing system. This consisted of pulsing purely resistive loads through both an earthed coaxial system and a flying lead system and analysing the voltage and current waveforms present during the pulse in each case.

The load resistance was varied between $50\Omega$ and $1.5k\Omega$ and the corresponding device voltage and current waveforms measured for a $+100V$ ESD pulse. These experiments are expected to show the effects of the transmission medium, and the effective resistance of the device, on the waveforms present during an ESD event.
4.5 Experimental Procedures

4.5.1 Introduction

The experimental investigation concentrated on the effects of voltage, temperature, and charge on the degradation\burnout threshold of GaAs MES device subject to ESD stress. The results will be shown in chapter 5 and discussed in chapter 6.

In all cases the pulse was applied to the gate of a device because an analysis of the previous literature on this subject, discussed in section 3.4.2.2, had shown this to be the most sensitive contact[8,9]. In the MESFET degradation experiments both the ohmic contacts were earthed, and in the MES diode experiments the source contact was earthed and the drain left floating. The chuck was left floating in all of the experiments.

4.5.2 Preliminary Experiments

A series of preliminary experiments was carried out to assess the electrical properties of the devices to be used in the study. The typical \( I_{ds} \) vs \( V_{ds} \) and \( I_{gs} \) vs \( V_{gs} \) characteristics as a function of temperature will be compared to existing data on similar structures.

4.5.3 MESFET ESD Degradation

4.5.3.1 \( I_{ds} \) vs \( V_{ds} \) Characteristics

A total of 517 devices from the E552 wafer were subject to a single positive polarity ESD pulse in the range +350V to +900V, and with negative polarity ESD pulses in the range -50V to -250V. The drain characteristics were analysed subsequent to a pulse, and depending on the changes of the saturated drain current, \( I_{ds} \), and transconductance, \( g_m \), the device was assigned to a particular failure category. These definitions of these failure categories will be
discussed in chapter 5.

Twenty devices from the I69W wafer were used to test the effects of multiple ESD pulses (10 in this case) at +300, +500V, -50V and -75V. In this set of experiments the changes in the $I_{ds}$ vs $V_{ds}$ characteristics were recorded subsequent to the 1st, 2nd and 10th pulse.

In addition, a study was carried out to assess the damage site(s) associated with single pulse ESD breakdown at -250V and +900V. The devices were stripped of the polyimide using a plasma etch, and analysed using a scanning electron microscope.

4.5.3.2 Parametric Degradation

Using the autoprobing facilities at STL, a series of experiments was carried out to assess the changes in several DC parameters subsequent to single ESD pulses. A total of 96 devices from the I69X wafer was used. The DC parameters measured were:

1) The saturated drain current, $I_{ds}$, measured at $V_{ds} = 2V$.
2) The transconductance $g_m$, measured at $V_{ds} = 2V$.
3) The pinch-off voltage $V_{p}$, defined as $\leq 5\%$ of $I_{ds}$.
4) The channel resistance $R_{on}$, measured as the gradient of the $I_{ds}$ vs $V_{ds}$ plot between $0V < V_{ds} < 0.2V$.
5) The diode ideality factor $n_r$, measured as the gradient in the exponential region of the log $I_{gs}$ vs $V_{gs}$ plot.
6) The diode built in voltage $V_{bi}$, measured as the intercept on the $V_{gs}$ axis of the log $I_{gs}$ vs $V_{gs}$ plot.
7) The source resistance $R_s$, measured as the gradient of the $I_{gs}$ vs $V_{gs}$ between $0.7V < V_{gs} < 1V$.

The experiments were carried out with positive and negative polarity pulses at 25°C and 100°C.
4.5.4 MES Diode ESD Degradation

4.5.4.1 Introduction

The MESFET structure consists of two MES diodes, one between the gate and source, and the other between the gate and drain. If both the ohmic contacts are earthed and a pulse applied to the gate, any current flow will be between the gate and both the ohmic contacts. In order to study the breakdown properties within a single well defined region of a device, a further study has been carried out into the breakdown characteristics of the gate-source MES diode alone. The gate-source diode within the MESFET structure was considered to be more appropriate for a detailed degradation analysis because only one current path is present and is more likely to breakdown than the gate-drain diode, because a greater field exists in this region during overstress.

4.5.4.2 \( I_{gs} \) vs \( V_{gs} \) Characteristics

In order to assess the changes in the basic electrical properties of a device a series of experiments were carried out, using 20 devices from the I69W wafer, to test the effect of ESD pulses on the \( I_{gs} \) vs \( V_{gs} \) characteristics. Electrically identical devices to within 5% were pulsed with single ESD pulses ranging from +500V to +1.5kV and -50V to -400V. The subsequent \( I_{gs} \) vs \( V_{gs} \) characteristics were compared to the pre-pulse characteristics. These experiments were carried out at 25°C.

4.5.4.3 Barrier height and Ideality Factor Degradation

In order to assess the changes due to an ESD pulse of the region between the metal and GaAs surface, further experiments were carried out. This consisted of pulsing 435 devices from the I69X wafer, with single ESD pulses ranging from +50V to +900V, and -50V to -200V. The ideality factor and barrier height magnitudes were then compared to their pre-pulse values. These experiments were also carried out at 25°C.
4.5.4.4 Capacitance-Voltage Characteristics

In order to assess whether any changes in the net donor concentration occur subsequent to ESD stress, a series of experiments were performed to measure the changes in the diode C-V characteristics subsequent to an ESD pulse. This will give an indirect indication of any changes in the net donor concentration beneath the gate, subsequent to an ESD pulse. The experiments used 10 devices from the I69X and I69W wafers. However, it was found that the capacitance of these devices was too small to measure accurately using the present set-up because noise within the system tended to dominate the C-V characteristics which limited the accuracy of this experiment.

4.5.4.5 Temperature Effects

The ambient temperature is well known to effect the electrical characteristics of a semiconductor device. In order to test whether an increased ambient temperature changes the sensitivity of a GaAs MES device to ESD stress, a series of experiments were carried out to measure the changes in the positive and negative degradation thresholds at elevated temperatures between 25°C and 150°C. This experiment used 168 devices from the I69W wafer. The AutoZap was programmed to sequentially pulse a device until a 2μA change was recorded in the $I_{gs}$ vs $V_{gs}$ characteristics.

4.5.4.6 AutoZap Capacitance Effects

Increasing the capacitance in the "human body" circuit increases the available charge in an ESD pulse. Therefore, experiments were carried out to assess the effect of the AutoZap capacitance on the positive and negative polarity ESD threshold's using 100 devices from the I69W wafer. The AutoZap was programmed to sequentially pulse a device, using the threshold method, until a 20μA change was recorded in the $I_{gs}$ vs $V_{gs}$ characteristics.
4.5.4.7 MES Diode ESD Threshold

A series of experiments were carried out to assess the differences in the ESD voltage threshold between the I69W and I69X wafers, as a function of the pulse increment. These experiments used 170 devices from the I69W and I69X wafers. The devices were pulsed, using the thresholding technique, with positive increments of +20V to +800V and negative increments of -4V to -20V. The threshold point was defined as a 2µA change in the $I_{gs}$ vs $V_{gs}$ characteristics.

4.5.4.9 ESD Waveform Analysis

Using the high frequency oscilloscope the current and voltage waveforms present during an ESD event were investigated. A number of experiments was carried out using 120 devices from the I69W and I69X wafers. These experiments assess the sub-threshold failure waveform patterns, and the DC $I_{gs}$ vs $V_{gs}$ characteristics. Specifically, these experiments were:

a) An assessment of the effects on the ESD voltage and current waveforms when increasing the ESD voltage from +300V to +900V and -25V to -100V.

b) An assessment of the effects on the ESD voltage and current waveforms when increasing the AutoZap capacitance from 100pF to 1000pF, at fixed ESD voltages of +100V and -50V.

c) An assessment of the effects on the ESD voltage and current waveforms when increasing the ambient temperature from 25°C to 150°C, at fixed ESD voltages of +500V and -50V.

d) An assessment of the voltage and current failure waveforms which characterise an ESD event. The devices were pulsed with +1.5kV, +2.5kV, -100V, -125V and -150V pulses.

e) A comparison of the ESD voltage and current failure waveforms between
the I69W and I69X wafers, at ESD voltages of +1.5kV, +2.5kV, -100V, -125V and -150V.

4.6 Summary

The experimental apparatus and procedures described in this chapter have been used to determine the sensitivity of GaAs MESFET\MES diode structures when subject to ESD stress. The investigation has included the assessment of effects of voltage, charge and temperature on the ESD failure threshold of GaAs MES devices.

4.7 References

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 Introduction

Chapter 4 has described the experimental apparatus and procedures which have been used to investigate the ESD degradation effects in GaAs MES devices. The results contained in this chapter are the culmination of a 5 year study sponsored initially by STC Ltd and over the past 3 years by the MOD (CVD). The results describe the characterisation of the ESD pulsing system and the assessment the ESD threshold levels in low noise GaAs MESFETs and MES diodes. Device degradation has been measured as a function of extrinsic parameters such as ESD voltage, charge, and ambient temperature.

5.2 System Characterisation

The voltage and current characterisation waveforms for the both the earthed coaxial system and flying lead system are shown in figs. (5.1) and (5.2). These results show the effects of the pulse transmission system on the waveforms subject to a device during an ESD event. The measured peak voltage $V_{\text{peak}}$ and current $I_{\text{peak}}$ for the two transmission systems are shown in tables (5.1) and (5.2). Also shown in Tables (5.1) and (5.2) are the predicted values of peak voltage and current for a simple resistive divider between the AutoZap and device. The results show that the peak voltage and current are less than would be expected for a system with only resistive elements present. These lower values are due to capacitive elements present between the AutoZap and the device and will be discussed in chapter 6. The coaxial system was adopted for the study on MES structures because this allows reproducible pulses to be applied to a device[1].

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Fig. (5.1) Voltage Characterisation Waveforms

![Voltage Characterisation Waveforms Graph]

Fig. (5.2) Current Characterisation Waveforms

![Current Characterisation Waveforms Graph]
5.3 Preliminary Experiments

5.3.1 MESFET $I_{ds}$ vs $V_{ds}$ Characteristics

Typical device $I_{ds}$ vs $V_{ds}$ characteristics for the E552, I69W and I69X wafers are shown in figs. (5.3) to (5.5).

The three main electrical parameters of the MESFET are the pinch-off voltage($V_p$), saturated drain current($I_{ds}$), and the transconductance($g_m$). These DC parameters have been measured for each wafer and typical values of $V_p$, $I_{ds}$, and $g_m$ are shown in table (5.3). These values of have been calculated from figs. (5.3) to (5.5) and represent the characteristics measured on the usable portion of each wafer. The centre, and the edges of each wafer showed the greatest deviation (>25%) from the average values shown in table (5.3) and were not used in any experiments. The greatest overall spread was evident on the I69X wafer.
Fig. (5.3) $I_{ds}$ vs $V_{ds}$ Characteristics for the E552 Wafer

Fig. (5.4) $I_{ds}$ vs $V_{ds}$ Characteristics for the I69X Wafer

Fig. (5.5) $I_{ds}$ vs $V_{ds}$ Characteristics for the I69W Wafer
Table (5.3) Experimental DC Parameters

<table>
<thead>
<tr>
<th></th>
<th>E552</th>
<th>I69X</th>
<th>I69W</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_p$</td>
<td>-1.25V</td>
<td>-1.4V</td>
<td>-1.2V</td>
</tr>
<tr>
<td>$I_{dss}$</td>
<td>10.2mA</td>
<td>8mA</td>
<td>7.2mA</td>
</tr>
<tr>
<td>$g_m$</td>
<td>9mS</td>
<td>5.3mS</td>
<td>6.75mS</td>
</tr>
</tbody>
</table>

These characteristics are similar to those reported in the literature for this type of device\[2\]. The drain($I_d$) current increases with drain voltage($V_d$) until velocity saturation limits the current. The gate can modulate the channel current by the application of a negative voltage from 0V to $-V_p$. The upper curves in figs. (5.3) and (5.5) represent the drain characteristics at $V_{gs} = 0$ and the lower curves represent the drain current at values of $V_{gs}$ between -0.1 and -1V. The current saturation effect is expected for MESFET devices with gate lengths less than 2\(\mu\)m\[2,3\]. Using the average pinch-off voltage for each wafer the n-type layer depths can be also be estimated from eqn. (2.17). These values are:

E552, $d = 0.157\mu$m  
I69X, $d = 0.166\mu$m  
I69W, $d = 0.158\mu$m

From eqn. (2.15) the theoretical saturation current can also be predicted. These values are shown below, assuming the initial depletion depth is $\approx 0.1\mu$m and a saturation velocity of $\approx 1.2 \times 10^5$ m/s.

E552, $I_{dss} = 16.4$mA  
I69X, $I_{dss} = 19.8$mA  
I69W, $I_{dss} = 16.7$mA

The experimental values in table (5.3) are lower than the predicted values probably because either:

a) Equation (2.15) is only valid for constant doping in the n-type layer. The gaussian doping profile present within these devices will lower the
average" level used in the calculation of the saturated drain current.

b) Large values of the source and drain resistances, $R_s$ and $R_d$, will add to the effective channel resistance.

c) Variations in the estimated gate depletion depth, and/or the presence of surface depletion regions[4], may effect the overall channel current by increasing the effective resistance of the channel.

5.3.2 MESFET $I_p$ vs $V_p$ Characteristics

Figs. (5.6) to (5.11) show the typical forward and reverse bias $I_p$ vs $V_p$ characteristics for a sample of gate/source MES diodes on the E552, I69X and I69W wafers. The devices were selected from several different points on the wafer.

The forward bias current increases exponentially above 0.7V, followed by a linear region until $\approx 2V$ and finally begins to saturate until the device breaks down at voltages $> 4.5V$. The current limiting region probably arises as a result of velocity saturation, followed by space charge limited conduction between the gate and source contacts. The initial forward bias velocity saturation value can be estimated using equation (2.15) by setting $h = 0$. The predicted and measured values for the E552, I69W and I69X wafers are shown in table (5.4).

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Predicted</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>E552</td>
<td>$I_s = 37.5mA$</td>
<td>$I_s = \approx 30-40mA$</td>
</tr>
<tr>
<td>I69X</td>
<td>$I_s = 39.8mA$</td>
<td>$I_s = \approx 18-30mA$</td>
</tr>
<tr>
<td>I69W</td>
<td>$I_s = 37.9mA$</td>
<td>$I_s = \approx 32-40mA$</td>
</tr>
</tbody>
</table>

The predicted values for the E552 and I69W wafer compare favourably with the higher measured values, but the experimental results for the I69X wafer show a much lower value of saturation current than predicted by eqn. (2.15).
Fig. (5.6)  Forward $I_F$ vs $V_F$ Characteristics for the E552 Wafer

Fig. (5.7)  Forward $I_F$ vs $V_F$ Characteristics for the I69X Wafer

Fig. (5.8)  Forward $I_F$ vs $V_F$ Characteristics for the I69W Wafer
Fig. (5.9) Reverse $I_g$ vs $V_g$ Characteristics for the E552 Wafer

Fig. (5.10) Reverse $I_g$ vs $V_g$ Characteristics for the I69X Wafer

Fig. (5.11) Reverse $I_g$ vs $V_g$ Characteristics for the I69W Wafer
Similar considerations to those outlined in section 5.3.1 with regard to the accuracy of the predictions probably apply to these results. The reverse characteristics for each wafer are shown in fig. (5.9) to (5.11). A small reverse current flows until the device enters the avalanche region, as evidenced by "white" light emission from the edge of the gate. The device will finally exhibit irreversible breakdown at a reverse current of \( \approx 1\text{mA} \) (high values of \(-V_{br}\)) to \( \approx 5\text{mA} \) (low values of \(-V_{br}\)). The reverse avalanche voltage range for \(-V_{br}\) measured on each wafer is shown in table (5.5). The greatest spread in the value of \(-V_{br}\) was found on the 169X wafer.

**Table (5.5) Reverse Bias Avalanche Voltages**

<table>
<thead>
<tr>
<th>Wafer</th>
<th>(-V_{br})</th>
</tr>
</thead>
<tbody>
<tr>
<td>552</td>
<td>-10V to -25V</td>
</tr>
<tr>
<td>169X</td>
<td>-8V to -48V</td>
</tr>
<tr>
<td>169W</td>
<td>-2SV to -3SV</td>
</tr>
</tbody>
</table>

The existing literature suggests that the reverse avalanche voltage is inversely proportional to the product of the doping level and n-type layer depth[5,6]. This would imply that the E552 and 169W wafers should, on average, have higher values of reverse breakdown voltage than devices on the 169X wafer. This appears to be the case for the majority of the results shown in figs. (5.9) to (5.11), but these are only small samples of the devices present on the wafers. It should be noted, however, that traps on the GaAs surface between the contacts may cause an increase the gate-drain breakdown voltage by a reduction of the peak field in the channel. Many other abnormal effects observed in MESFET devices, including prematurely high reverse breakdown voltages, have been attributed to the presence of these surface traps[5-8].

### 5.3.4 Temperature effects

Fig. (5.12) show the changes in the sub-burnout forward bias \( I_{gs} \) vs \( V_{gs} \) characteristics, with the ambient temperature increasing from 25°C to 150°C. The magnitude of the forward bias current limiting region decreases by \( \approx 10\text{mA} \) at \( V_{ds} = 5V \) over this range of temperature.
Fig. (5.12) Temperature Effects on the Forward $I_{gs}$ vs $V_{gs}$ characteristics

Fig. (5.13) Temperature Effects on the Reverse $I_{gs}$ vs $V_{gs}$ characteristics

Fig. (5.14) Temperature Effects on the Reverse $\log(I_{gs})$ vs $V_{gs}$ characteristics
This decrease is qualitatively consistent with the changes in saturation velocity as a function of temperature[5]. The source resistance also increases with temperature probably caused by the decrease in the electron mobility at the higher temperatures.

Figs. (5.13) and (5.14) show the reverse current, plotted on a linear and log scale respectively as a function of the reverse gate voltage. It is clear that the reverse avalanche voltage $-V_{br}$ increases with temperature and the change is more pronounced at 150°C. The change in avalanche voltage is qualitatively consistent with the decrease in impact ionisation coefficients with increasing temperature[10]. In addition the reverse leakage current increases with temperature. This effect can be predicted by considering the Schottky barrier lowering effects on the leakage current through the depletion layer under reverse bias[11].

5.4 MESFET ESD Degradation

5.4.1 Degradation Categories

ESD pulses ranging from +350V to +900V, and from -50V to -250V were applied to devices on the E552 wafer. Two degradation categories, and two burnout categories were evident from the results. The classification terms used here are based on the changes in the $I_{ds}$ vs $V_{ds}$ characteristic parameters, $I_{dss}$ and $g_m$, after pulsing.

Category (1) failures had no measurable change, i.e. <5%, in the parameters $I_{dss}$ and $g_m$. Category (2) had a greater than -5% change and category (3) had greater than +5% change in the parameters $I_{dss}$ and $g_m$ after pulsing. Category (4) failures showed degradation in $g_m$ with $I_{dss}$ constant to within 5%. Category (5) failures simply showed near resistive characteristics after pulsing. Tables (5.6) and (5.7) summarise these failure categories, and give approximate voltage ranges for failure in each category. Figs (5.15) to (5.19) show the $I_{ds}$ vs $V_{ds}$ characteristics associated with each category.
Fig. (5.18) Category (4) Failure Characteristics

Fig. (5.19) Category (5) Failure Characteristics
Fig. (5.20) Positive Polarity Failure Statistics

Fig. (5.21) Negative Polarity Failure Statistics
The results show that the full MESFET structure can be severely degraded at voltages as low as -50V and +500V. In many cases the device can still operate as a transistor and can be classified as a "walking wounded" failure.

5.4.2 Multiple Pulsing

A series of experiments was carried out to assess the degradation in the $I_{ds}$ vs $V_{ds}$ characteristics after 10 pulses at $+300V$, $+500V$, $-50V$ and $-100V$. Pulsing at $+300V$ caused no significant change in the $I_{ds}$ vs $V_{ds}$ characteristics, i.e. category (1) characteristics, while pulsing at $+500V$ showed a gradual degradation in the $I_{ds}$ vs $V_{ds}$ characteristics, i.e. category (2) characteristics. Visible damage was observed after 8 pulses. Typical results for 0, 1, 2 and 10, $+500V$ pulses are shown in figs. (5.22 a-d).

No significant degradation in the $I_{ds}$ vs $V_{ds}$ characteristics was observed for pulses at $-50V$, i.e. category (1) characteristics. Pulsing at $-100V$ caused degradation effects similar to those observed for positive polarity pulsing at $+500V$. After the first pulse, damage was evident between the gate and source contacts, with $I_{dss}$ and $g_m$ severely degraded, i.e. category (2) characteristics. Subsequent pulses caused further degradation in $g_m$ alone eventually leading to a super-position of all the $I_{ds}$ vs $V_{gs}$ curves indicating no gate modulation is taking place, i.e. severe category (4) characteristics. $I_{ds}$ vs $V_{ds}$ characteristics similar to those in fig. (5.22d) were observed after 5 pulses.

The cumulative degradation rate for positive polarity pulses is lower than observed for negative polarity pulses at a given pulse voltage. Degradation in both $I_{dss}$ and $g_m$, i.e. category (2) failure characteristics, is normally observed until visible damage is evident. Subsequent pulsing tends to decrease $g_m$ alone until no gate modulation is possible.
Fig. (5.22a) Cumulative Degradation Characteristics - Zero Pulses

Fig. (5.22b) Cumulative Degradation Characteristics - 1 Pulse
Fig. (5.22c) Cumulative Degradation Characteristics - 2 Pulses

Fig. (5.22d) Cumulative Degradation Characteristics - 10 Pulses
Fig. (5.23) Positive Polarity Burnout

Fig. (5.24) Negative Polarity Burnout
5.4.3 Visible Failure Modes

No visible evidence was observed for the degraded devices (categories 2-3). Category (4) failures resulted in damage between the gate and source contacts. Category (5) failures were similar in appearance to the category (4) failures but occurred between the gate and drain contacts. Category (4) and (5) failures showed marked differences in the amount of damage between the contacts depending on the polarity of the applied pulse. SEM micrographs of the damage associated with a +900V ESD pulse and a -250V ESD pulse are shown in figs. (S.23) and (S.24) respectively. Negative polarity pulses caused severe damage in the channel region, which melted part of the ohmic contact. Positive polarity pulses only caused minor damage near the edge of the gate.

5.4.4 Parametric Degradation

Initially the results from this experiment, which was carried out at STL, were analysed using a difference graph, with any unchanged values on a 45°, "no change", line and any values which increased or decreased were plotted above or below respectively. The results plotted in this form showed no discernable trends. This inconsistency in the results was initially attributed to the automatic probing system, since the control groups changed beyond acceptable limits. Two sets of parametric tests were performed on a second set of devices and the probe system was shown to be sufficiently accurate by STL personnel[12]. The original results were therefore tabulated which showed the difference value for each parameter relative to the pre-pulse value. In order to qualify the results, the device must have had all the parameters measurable subsequent to the test pulse. Any device grossly out of specification before, or after, pulsing were regarded as failed and not included in the analysis. This tended to be the case with the negative polarity results. The tabulated results for parametric degradation are shown in tables (5.8) to (5.18). At the lower positive voltages at 25°C, small changes are evident in many of the parameters, but at the higher voltages a definite decrease in the source resistance $R_s$ is observed (see tables 5.10 and 5.11). At 100°C a very large increase in the channel resistance $R_{on}$ is evident, much greater than observed at
25°C. This decreases $I_{ds}$ and $g_m$ significantly (see tables 5.14 to 5.16). Some of the devices which exhibit the large changes in $R_{on}$ are also accompanied by a decrease in $R_s$ (see table 5.16 - devices 5 & 7). Negative polarity pulses at -100V degraded the majority of device out of specification, but the devices which remained measurable had much lower values of $R_s$. At 100°C more devices remained in specification after a negative polarity pulse of -100V. In general, these results show that an increase in the ambient temperature increases the likelihood of degradation during a positive polarity pulse and decreases the burnout probability during a negative polarity pulse.

**Table (5.8) - 169X 1μm MESFETs, Control Group, 25°C**

<table>
<thead>
<tr>
<th>Voltage(V)</th>
<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bd}$(V)</th>
<th>$I_{ds}$(mA)</th>
<th>$g_m$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
<td>1.</td>
<td>+0.49</td>
<td>-0.01</td>
<td>+0.008</td>
<td>-0.34</td>
<td>-1.04</td>
<td>+136</td>
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</tr>
<tr>
<td>2.</td>
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<td>+0.013</td>
<td>+0.42</td>
<td>+0.08</td>
<td>+5.9</td>
<td>-0.005</td>
</tr>
<tr>
<td>3.</td>
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<td>+0.01</td>
<td>+0.36</td>
<td>+0.3</td>
<td>+16.5</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
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<td>-0.03</td>
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<td>+0.21</td>
<td>-0.37</td>
<td>+28</td>
<td>+0.025</td>
</tr>
<tr>
<td>5.</td>
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<td>-0.02</td>
<td>+0.008</td>
<td>-0.164</td>
<td>-0.5</td>
<td>+20.5</td>
<td>-0.005</td>
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<tr>
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<td>+0.008</td>
<td>+0.33</td>
<td>+0.18</td>
<td>+9.6</td>
<td>-0.005</td>
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<td>+1.01</td>
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<td>+11.9</td>
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</tr>
<tr>
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<td>+0.008</td>
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<td>+10.7</td>
<td>-0.005</td>
</tr>
<tr>
<td>12.</td>
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<td>+0.19</td>
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<td>+38</td>
<td>-0.005</td>
</tr>
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**Table (5.9) - 169X 1μm MESFETs, +100V, 25°C**

<table>
<thead>
<tr>
<th>Voltage(V)</th>
<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bd}$(V)</th>
<th>$I_{ds}$(mA)</th>
<th>$g_m$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
<td>1.</td>
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<td>+0.02</td>
<td>+0.34</td>
<td>+8.3</td>
<td>-0.015</td>
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<td>-0.04</td>
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<td>+13.9</td>
<td>-0.05</td>
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<tr>
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<td>-0.005</td>
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<tr>
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<td>+0.013</td>
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<td>-0.05</td>
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<td>+19.9</td>
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<tr>
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Table (5.10) - 169X 1μm MESFETs, +300V, 25°C

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<tr>
<th>Voltage (V)</th>
<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bi}$(V)</th>
<th>$I_{ds}$(mA)</th>
<th>$g_{m}$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
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<td>+0.11</td>
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</tr>
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<td>-0.015</td>
</tr>
<tr>
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<td>-0.06</td>
<td>+0.07</td>
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<td>+4.9</td>
<td>-0.015</td>
</tr>
<tr>
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</tr>
<tr>
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<td>+0.18</td>
<td>-0.05</td>
<td>-0.13</td>
<td>+0.03</td>
<td>+24.1</td>
<td>-0.005</td>
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<tr>
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<td>-0.062</td>
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<td>+0.28</td>
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Table (5.11) - 169X 1μm MESFETs, +500V, 25°C

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<th>Voltage (V)</th>
<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bi}$(V)</th>
<th>$I_{ds}$(mA)</th>
<th>$g_{m}$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
<td>1.</td>
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<td>-0.005</td>
</tr>
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<td>-0.015</td>
</tr>
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<td>+0.5</td>
<td>+23.5</td>
<td>-0.02</td>
</tr>
<tr>
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<td>+0.24</td>
<td>-0.07</td>
<td>-0.36</td>
<td>-0.08</td>
<td>+4.5</td>
<td>-0.009</td>
</tr>
<tr>
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<td>-13.7</td>
<td>+0.21</td>
<td>-0.06</td>
<td>-0.164</td>
<td>+1.38</td>
<td>+14.3</td>
<td>-0.015</td>
</tr>
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<td>+0.6</td>
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<td>-0.01</td>
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<tr>
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<td>0</td>
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Table (5.12) - 169X 1μm MESFETs, -100/-150V, 25°C

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<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bi}$(V)</th>
<th>$I_{ds}$(mA)</th>
<th>$g_{m}$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
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<td>-150V</td>
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<td>+0.71</td>
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### Table (5.13) - I69X 1µm MESFETs, Control Group, 100°C

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<th>$V_{bh}$ (V)</th>
<th>$I_{ds}$ (mA)</th>
<th>$g_m$ (mS)</th>
<th>$R_{on}$ (Ω)</th>
<th>$V_p$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
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<td>-0.4</td>
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<td>-0.005</td>
</tr>
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<td>-0.005</td>
</tr>
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### Table (5.14) - I69X 1µm MESFETs, +100V, 100°C

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<th>$R_s$ (Ω)</th>
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<th>$V_{bh}$ (V)</th>
<th>$I_{ds}$ (mA)</th>
<th>$g_m$ (mS)</th>
<th>$R_{on}$ (Ω)</th>
<th>$V_p$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
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<td>+0.08</td>
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<td>+0.005</td>
<td>-0.6</td>
<td>-1.23</td>
<td>+12</td>
<td>-0.01</td>
</tr>
<tr>
<td>7.</td>
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<td>+0.005</td>
<td>-3.4</td>
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<td>+0.006</td>
<td>-8.2</td>
<td>-10.9</td>
<td>+&gt;10⁵</td>
<td>-0.98</td>
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### Table (5.15) - I69X 1µm MESFETs, +200V, 100°C

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<tr>
<th>Voltage (V)</th>
<th>$R_s$ (Ω)</th>
<th>$n_f$</th>
<th>$V_{bh}$ (V)</th>
<th>$I_{ds}$ (mA)</th>
<th>$g_m$ (mS)</th>
<th>$R_{on}$ (Ω)</th>
<th>$V_p$ (V)</th>
</tr>
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<tr>
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<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
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<td>+0.006</td>
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<td>+27</td>
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<td>2.</td>
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<td>+0.004</td>
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<td>-0.52</td>
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<tr>
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<td>+0.004</td>
<td>-4.02</td>
<td>-2.55</td>
<td>+40</td>
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<td>+0.09</td>
<td>-0.023</td>
<td>-4.62</td>
<td>-3.42</td>
<td>+35</td>
<td>-0.01</td>
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<td>6.</td>
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</table>
Table (5.16) - 169X 1μm MESFETs, +500V, 100°C

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<th>Voltage (V)</th>
<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bi}$(V)</th>
<th>$I_{ds}(mA)$</th>
<th>$g_m$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
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</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
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<td>-5.11</td>
<td>-7.3</td>
<td>+272</td>
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<td>-0.9</td>
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<td>+12</td>
<td>+499</td>
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<td>-5.3</td>
<td>+79</td>
<td>+0.04</td>
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<td>-9.47</td>
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<td>-0.05</td>
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Table (5.17) - 169X 1μm MESFETs, +900V, 100°C

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<th>$R_s$(Ω)</th>
<th>$n_f$</th>
<th>$V_{bi}$(V)</th>
<th>$I_{ds}(mA)$</th>
<th>$g_m$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
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<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
</tr>
<tr>
<td>1.</td>
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<td>+726</td>
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<td>-6.54</td>
<td>-9.7</td>
<td>+6.5K</td>
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<tr>
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Table (5.18) - 169X 1μm MESFETs, -100V, 100°C

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<th>$V_{bi}$(V)</th>
<th>$I_{ds}(mA)$</th>
<th>$g_m$(mS)</th>
<th>$R_{on}$(Ω)</th>
<th>$V_p$(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(average value)</td>
<td>15</td>
<td>1.22</td>
<td>0.7</td>
<td>8</td>
<td>5.3</td>
<td>120</td>
<td>-1.4</td>
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<td>-0.005</td>
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<td>-7.7</td>
<td>-10.1</td>
<td>+10^5</td>
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</table>
5.5 MES Diode Degradation

5.5.1 Introduction

These experiments used the transmission line system between the AutoZap and the device. This allows the ESD pulses to be more consistent, but was found to significantly increase the damage threshold in these devices. This was traced to the increased capacitance between the AutoZap and the device as indicated in the characterisation experiments outlined in section 5.2.

5.5.2 $I_{gs}$ vs $V_{gs}$ Degradation

Figs. (5.25) to (5.27) show a sample of changes in the forward and reverse $I_{gs}$ vs $V_{gs}$ characteristics after the application of a +500V and +1kV pulse using the AutoZap. The forward bias characteristics indicate that the source resistance increases, as the pulse voltage is increased from +500V to +1kV and the current saturation decreases with applied voltage. An optically visible "white" region at a single point between the gate and source contacts was evident after the +1kV pulse. The reverse bias characteristics show an increase in the leakage current and a decrease in the reverse breakdown voltage. Pulsing in excess of +1.5kV also caused total failure, and had linear $I_{gs}$ vs $V_{gs}$ characteristics under both forward and reverse bias. A optically "black" region, at a single point between the gate and source contacts, was evidence of this failure mode.

Figs. (5.28) to (5.30) show typical changes in the forward and reverse $I_{gs}$ vs $V_{gs}$ characteristics after the application of a -50V, and -75V pulse using the AutoZap. The forward bias characteristics show a decrease in the source resistance as a function of the applied voltage. The current saturation region remains virtually constant at all pulse voltages. The reverse bias characteristics show no change in the reverse breakdown voltage but an slight increase in the reverse leakage current is evident. In the majority of cases "white" failures were observed for negative polarity pulsing above -100V and had similar post-pulse $I_{gs}$ vs $V_{gs}$ characteristics to the +1kV positive polarity results. Pulsing in excess of -200V caused total failure and the associated linear $I_{gs}$ vs $V_{gs}$ characteristics.

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5.5.3 Interface Effects

The degradation of the metal-semiconductor interface barrier height and ideality factor are plotted in figs. (5.31) and (5.32) respectively. The graphs show the mean average change of the parameter at each stress voltage. Pulsing at voltages less than +300V appears to increase the barrier height and decrease the ideality factor, therefore improving the diode characteristics. Pulsing at higher voltages severely degrades both the barrier height and ideality factor. Negative polarity pulses tended to degrade both parameters, though a slight improvement in the ideality factor is evident at voltages less than -100V.

5.5.4 Temperature Effects

Using the thermal chuck arrangement, the temperature effects on the sequential pulsing voltage threshold of devices from the I69W wafer were assessed. The results both for positive and negative polarity pulses are shown in figs. (5.33) and (5.34). The positive voltage threshold decreases approximately linearly from +500V to +250V for a 100°C increase in ambient temperature above room temperature. The negative voltage threshold shows a non-linear increase in magnitude from -75V to -90V, for the same temperature change.

5.5.5 AutoZap Capacitance Effects

The variation in positive and negative polarity voltage thresholds are shown in figs. (5.35) and (5.36). An increase in AutoZap capacitance, and hence the charge available during an ESD event, causes an 1/V type decrease in both the positive and negative voltage thresholds from +1650V to +250V, and from -93V to -50V respectively over a ten fold increase in capacitance. The positive polarity threshold at 100pF is much greater than that observed for the previous set of results in section 5.5.3 at 25°C. This is attributed to the failure leakage current being a decade greater in this set of experiments, thus a higher ESD voltage is required for given damage causing an increase in leakage current.

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Fig. (5.25) Positive Polarity Forward Bias $I_F$ vs $V_F$ Degradation

Fig. (5.26) Positive Polarity Reverse Bias $I_F$ vs $V_F$ Degradation

Fig. (5.27) Positive Polarity Reverse Bias Log $I_F$ vs $V_F$ Degradation
Fig. (5.28) Negative Polarity Forward Bias $I_{p}$ vs $V_{p}$ Degradation

Fig. (5.29) Negative Polarity Reverse bias $I_{p}$ vs $V_{p}$ Degradation

Fig. (5.30) Negative Polarity Reverse bias Log $I_{p}$ vs $V_{p}$ Degradation
Fig. (5.31) Ideality Factor Degradation

Fig. (5.32) Barrier Height Degradation
Fig. (5.33) Temperature Effects on the Positive Polarity ESD Threshold

![Graph showing the relationship between temperature and positive voltage threshold for I69W MES Diodes. The graph includes a regression line with a correlation coefficient of r = -0.947.]

Fig. (5.34) Temperature Effects on the Negative Polarity ESD Threshold

![Graph showing the relationship between temperature and negative voltage threshold for I69W MES Diodes. The graph includes a regression line with a correlation coefficient of r = -0.947.]

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Fig. (5.35) AutoZap Capacitance Effect on Positive Polarity Threshold

Fig. (5.36) AutoZap Capacitance Effect on Negative Polarity Threshold
Fig. (5.37) Positive Polarity Wafer Threshold Comparison

![Graph showing positive polarity wafer threshold comparison]

Fig. (5.38) Negative Polarity Wafer Threshold Comparison

![Graph showing negative polarity wafer threshold comparison]
5.5.6 ESD Wafer Threshold Comparison

Fig. (5.37) to (5.38) show the variations in the ESD voltage threshold as a function of pulse increment. The 169X positive polarity results consistently show a larger threshold compared to the 169W wafer. The voltage threshold appears to be a function of the pulse increment. The negative polarity thresholds are approximately -115V, and appear relatively independent of pulse increment. The 169W devices have a slightly lower overall threshold.

5.5.7 Stress Waveform Analysis

5.5.7.1 ESD Voltage Effects

Using the high frequency oscilloscope the voltage and current waveforms which are delivered to a device during a single sub-threshold ESD event were analysed. The voltage and current waveforms from +300V to +900V and from -25V to -100V, are shown in figs. (5.39) to (5.42). These are typical of the waveforms recorded for devices on 169W wafer. The post-pulse forward and reverse $I_{gs}$ vs $V_{gs}$ plots for these devices are shown in figs. (5.43) and (5.44).

5.5.7.1.1 Positive Polarity - Figs. (5.39), (5.40) and (5.43)

After an initial period of voltage ringing, which appears to be a function of voltage magnitude, the voltage decays and enters a voltage "plateau" region at $\approx +5V$. The duration of this region is related to the applied voltage magnitude. Another feature of the voltage waveforms is the rise in voltage to $\approx 6V$, towards the end of the plateau region, which occurred in many of the results. There is a definite change in the decay time constant at characteristic times related to the applied ESD voltage. These changes all occur in the voltage range 2-3V. The characteristic times are $\approx 350$ns, 700ns and 1.1$\mu$s for $+300V$, $+600V$, and $+900V$ respectively. The peak values and characteristic decay times of the current waveforms appear to be related to the applied voltage. An increase in the applied voltage causes the magnitude of the peak current to increase. Ringing occurs in all the waveforms, especially at the higher voltages, unfortunately this
Fig. (5.39) Device Voltage Waveform vs Positive ESD Voltage

Fig. (5.40) Device Current Waveform vs Positive ESD Voltage
Fig. (5.41) Device Voltage Waveform vs Negative ESD Voltage

Fig. (5.42) Device Current Waveform vs Negative ESD Voltage
Fig. (5.43) Positive Polarity $I_p$ vs $V_p$ Characteristic

Fig. (5.44) Negative Polarity $I_p$ vs $V_p$ Characteristic
is characteristic of all AutoZap pulse systems[13]. The profile of the current waveforms do not have a true exponential decay profile, as expected, due to the transmission line capacitance effects described in section 5.2. There appear to be no major changes in the current waveforms at the characteristic times defined by the voltage waveforms, although the points at which the voltage waveforms begin to rise to $\approx 6V$ all occur when the device current had reached $\approx 40mA$. The forward bias $I_{gs}$ vs $V_{gs}$ plot for this device shows a change in the effective resistance of the device at $+0.7V$ and $+2-3V$. The device finally breaks down at $\approx +7V$ and the current saturation region occurs between 24-40mA.

5.5.7.1.2 Negative Polarity - Figs. (5.41), (5.42) and (5.44)

The voltage waveform increases in magnitude to peak values of -15V, -30V, -40V and -55V, for applied ESD voltages of -25V, -50V, -75V and -100V respectively. The decay time constant at -25V, -50V, and -75V is very large and hence little decay in the voltage occurred in the first 2$\mu$s. Increasing the oscilloscope time-base showed the waveforms decay to 63% of their peak value in $\approx 1ms$. A current spike appears at the onset of the pulse and decays to near zero when the voltage saturates at its peak value. A similar spike also occurred when the pulse was discharged into the voltage probe. This implies that the pulse generation system/transmission medium may be causing this effect. Therefore, any subtle changes in the current waveforms early in the pulse may be masked by this effect. It was established, however, that the rate of decay after $\approx 100ns$ for the -25V to -75V results, depend on the applied ESD voltage. The -100V pulse shows a -2mA current saturation region for a duration of 600ns and then a decay toward zero. The reverse bias, $I_{gs}$ vs $V_{gs}$ characteristic shows virtually zero current flow, until -30V when the device enters the avalanche breakdown region.

5.5.7.2 AutoZap Capacitance Variations

The current and voltage waveforms for sub-threshold ESD voltage stress of +100V and -50V, were compared for variations in the AutoZap capacitance between 100pF and 1000pF. These results are shown in figs. (5.45) to (5.48). The post-pulse forward bias and reverse bias, $I_{gs}$ vs $V_{gs}$ characteristic for these devices
are shown in figs. (5.49) and (5.50).

5.5.7.2.1 Positive Polarity - Figs. (5.45), (5.46) and (5.49)

The waveforms show the voltage plateau region at \( \approx +5V \), as noted in section 5.5.6.1.1. The duration of the this plateau region increases linearly with the capacitance. The initial peak voltage and the voltage peak at the end of the plateau region are similar in magnitude and rises to between 5V and 6V. At the higher values of capacitance, and there is a increase in the voltage decay time constant at characteristic times also related to the AutoZap capacitance. These characteristic times are \( \approx 150\text{ns} \), 600\text{ns} and 1.05\mu s for \( C = 100\text{pF} \), 500\text{pF} and 1000\text{pF} respectively, and again all occur at +2-3V. The initial peak current increases between the 100pF and 500pF results, and then remains essentially constant. The current decay time constant increases in direct relation to the AutoZap capacitance. In all cases the waveforms experience a small step when the current decays to \( \approx 35\text{mA} \), these points occur at the same point in the voltage waveform when the voltage rises to \( \approx +6V \) at the end of the plateau region. Only slight changes in the current waveform occur at the characteristic times recorded for the voltage waveform. The forward bias \( I_{gs} \) vs \( V_{gs} \) characteristics show changes in the effective resistance of the device at +0.7V and +2-3V. The current saturation region occurs between +3V and +5.3V. The magnitude of the saturation current is between 30-35mA.

5.5.7.2.2 Negative Polarity - Figs. (5.47), (5.48) and (5.50)

The voltage across the device rises to its peak value in all cases within 500\text{ns}. The peak values are -25V, -45V and -50V for the 100pF, 500pF and 1000pF results, respectively. The highest capacitance, i.e 1000pF, within the "human body" circuit allows the device voltage to rise to the full applied ESD voltage during the pulse. The decay time constant for each waveform was measured to be \( \approx 1\text{ms} \). The current waveform for the 100pF capacitance decays to near zero in \( \approx 400\text{ns} \), while the higher capacitance values show longer decay times of \( \approx 800\text{ns} \). The reverse bias, \( I_{gs} \) vs \( V_{gs} \) characteristic shows virtually zero current flow, until -30V, when the device enters the avalanche breakdown region.
Fig. (5.45) Capacitance Effect on Positive ESD Voltage Waveform

![Capacitance Effect on Positive ESD Voltage Waveform](Image)

Fig. (5.46) Capacitance Effect on Positive ESD Current Waveform

![Capacitance Effect on Positive ESD Current Waveform](Image)
Fig. (5.47) Capacitance Effect on Negative ESD Voltage Waveform

Fig. (5.48) Capacitance Effect on Negative ESD Current Waveform
Fig. (5.49) Positive Polarity $I_{gs}$ vs $V_{gs}$ Characteristic

Fig. (5.50) Negative Polarity $I_{gs}$ vs $V_{gs}$ Characteristic
5.5.7.3 Temperature Effects

The voltage and current waveforms recorded for pulses at +500V and -50V, at 25°C, 75°C and 175°C, are shown in figs. (5.51) to (5.54).

5.5.7.3.1 Positive Polarity - Figs. (5.51) and (5.52)

In the early part of the waveforms the voltage and current waveforms appear relatively independent of temperature. The duration of the voltage plateau region increases from 500ns to 600ns for the 150°C increase in temperature. The characteristic times at which the decay time constant experiences a rapid rise, also increases with temperature. The greatest change in the waveforms clearly occurs between 75°C and 175°C. The current waveforms appear independent of temperature over the temperature range used in this study.

5.5.7.3.2 Negative Polarity - Figs. (5.53) and (5.54)

The voltage waveforms at each temperature are similar and reach the a peak of -25V whereas the decay time constant appears to decrease slightly as the temperature is increased. The decay time constant of the current waveforms appears to increase slightly with temperature.

5.5.7.4 Failure Waveforms

Typical voltage and current failure waveforms for positive and negative polarity pulses of +1.5kV and +2.5kV, at 25°C and -200V, -300V and -400V, at both 25°C and 150°C are shown in figs. (5.55) to (5.58).

5.5.7.4.1 Positive Polarity - Figs. (5.55) and (5.56)

The +1.5kV and +2.5kV voltage waveforms at 25°C show a premature collapse in the voltage plateau region at 200ns and 250ns respectively. The +1.5kV shows a further rise to \( \approx +5V \) at \( \approx 900ns \) and then decays in a similar manner to that observed for subthreshold pulses.
Fig. (5.51) Temperature Effect on the Positive ESD Voltage Waveform

![Graph showing the effect of temperature on the positive ESD voltage waveform for I69W MES Diodes. The graph displays different voltage responses at 25°C, 75°C, and 175°C.](image)

Fig. (5.52) Temperature Effect on the Positive ESD Current Waveform

![Graph showing the effect of temperature on the positive ESD current waveform for I69W MES Diodes. The graph displays different current responses at 25°C, 75°C, and 175°C.](image)
Fig. (5.53) Temperature Effect on the Negative ESD Voltage Waveform

![Graph showing the effect of temperature on the negative ESD voltage waveform for I69W MES Diodes. The graph plots device voltage (V) against time (us) with temperatures at 150°C, 75°C, and 25°C. A -50V pulse is applied.]

Fig. (5.54) Temperature Effect on the Negative ESD Current Waveform

![Graph showing the effect of temperature on the negative ESD current waveform for I69W MES Diodes. The graph plots device current (A) against time (us) with temperatures at 150°C, 75°C, and 25°C. A -50V pulse is applied.]

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Fig. (5.55) Positive Polarity Voltage Failure Waveforms

Fig. (5.56) Positive Polarity Current Failure Waveforms
Fig. (5.57) Negative Polarity Voltage Failure Waveforms

![Graph showing voltage waveforms for I69W MES Diodes with negative polarity voltages of -200V, -125V, and -100V. The x-axis represents time in microseconds from 0.2 to 1.8, and the y-axis represents device voltage in volts from -70 to 20.]

Fig. (5.58) Negative Polarity Current Failure Waveforms

![Graph showing current waveforms for I69W MES Diodes with negative polarity voltages of -200V, -125V, and -100V. The x-axis represents time in microseconds from 0.2 to 1.8, and the y-axis represents device current in amperes from -0.6 to 0.2.]
The +2.5kV waveform shows no such recovery in the voltage, and gradually decays to near zero. The +1.5kV pulse caused a visible "white" failure site between the gate and source contacts, as described in section 5.5.1, which resulted in a decrease in the forward bias DC current saturation region. The 2.5kV pulse resulted in a visible "black" failure site between the gate and source contacts with the associated $I_{gs}$ vs $V_{gs}$ characteristics. The current waveforms show an increase in peak current as a function of the applied voltage. No changes in the current waveform are evident at the failure time(s) observed in the voltage waveform.

5.5.7.4.2 Negative Polarity - Figs. (5.57) and (5.58)

During a pulse of -100V the device voltage increases to near -60V and then begins to decay very slowly. After 750ns the voltage rapidly collapses to near zero and then exhibits a recovery to around -20V. The current remains very small until the voltage collapses, then a rapid spike occurs for $\approx 20$ns. At the higher ESD voltages the voltage collapse occurs during the rising portion of the pulse and the higher the ESD voltage, the earlier the voltage collapse occurs. Each of these devices show a slight decrease in the reverse breakdown voltage, increase in reverse leakage current and a decrease in the forward bias current saturation region. A single "white" failure site was observed for all the devices pulsed between -100V and -200V. In general, at ESD voltages above -200V the devices showed no voltage recovery and had visible "black" failure sites subsequent to the pulse. No measurable changes in the current waveforms are evident at the characteristic recovery times observed in the voltage waveforms.

5.5.7.5 Wafer ESD Failure Waveform Comparison

The positive polarity failure waveforms for four devices from the I69X and I69W wafers are shown in figs. (5.59) and (5.60). The negative polarity failure waveforms are not shown.
Fig. (5.59) I69X/W Positive Polarity Voltage Failure Waveforms

![Graph showing voltage waveforms with labels I69W/2, I69X/1, I69X/2, and I69W/1 with time in microseconds on the x-axis and voltage on the y-axis.]

Fig. (5.60) I69X/W Positive Polarity Current Failure Waveforms

![Graph showing current waveforms with labels I69X/1, I69X/2, I69W/1, and I69W/2 with time in microseconds on the x-axis and current on the y-axis.]

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5.5.7.5.1 Positive Polarity - Figs. (5.59) and (5.60)

The I69X +1.5kV failure waveforms show the expected collapse in the voltage plateau region at times between 200ns and 300ns, each waveform shows a recovery in the voltage to \(\approx +5\text{V} \) at \(\approx 1\mu\text{s}\). The I69W waveforms show the collapse in the voltage at \(\approx 120\text{ns}\) and show no recovery in the voltage. The I69X devices had a reduction in the DC current saturation region and a visible "white" region between the gate and source contacts. The I69W devices had linear DC characteristics and visible "black" failure sites between the gate and source contacts.

5.5.7.5.2 Negative Polarity - Not Shown

The profile of the voltage waveforms for both the I69X and I69W devices are similar to those observed in section 5.5.6.4.2. The peak voltage attained by the I69X devices is slightly less than observed for the I69W devices. The point in time at which the voltage begins to recover is similar for both sets of devices, at each stress voltage. The current waveforms are virtually identical for each set of devices as found with the positive polarity results.

5.6 Summary

The characteristics of the ESD pulsing system and the sensitivity of GaAs MESFET and MES diode structures has been investigated. The results show the following major effects:

a) The transmission medium between the AutoZap and a device under test, i.e., the coaxial or flying leads, will effect the shape and magnitude of an ESD pulse.

b) Single ESD pulses of less than -100V and +300V can degrade the \(I\backslash V\) characteristics of GaAs MESFET/MES structures. Four categories of degradation and burnout have been found.
c) GaAs MESFET structures show gradual degradation in I/V characteristics after a number of subthreshold ESD pulses. The degradation rate is dependant on the polarity of the applied pulse.

d) GaAs MES diode structures show slight improvement in Schottky interface characteristics after single subthreshold positive polarity ESD pulses.

d) An increase in ambient temperature decreases the positive polarity ESD threshold voltage, while increasing the negative polarity ESD threshold.

e) Increasing the amount of charge available in the ESD pulse decreases both the positive and negative ESD threshold voltage.

f) The positive polarity ESD threshold voltage measured using the thresholding technique is dependant on the pulse increment. The negative polarity ESD threshold was found to be independent of the pulse increment.

g) Analysis of the subthreshold/threshold waveforms reveal:

i) Under subthreshold positive polarity ESD stress the device voltage enters a plateau region around +5V which is independent of pulse voltage (below threshold). The duration of this plateau region is dependant on the applied ESD voltage, the external capacitance and the ambient temperature. The current waveform appears relatively independent of the device and the profile is related to both the applied ESD voltage and external capacitance.

ii) Under subthreshold negative polarity ESD stress the device simply acts as a high resistance. Little current flows until the device voltage passes the DC avalanche voltage.

iii) Analysis of the positive polarity threshold/superthreshold pulses show a premature collapse of the voltage plateau region. This voltage collapse
has been observed to occur up to 300ns into the pulse. The current waveforms show no change from the normal exponential decay profile at the point of voltage collapse.

iv) Analysis of near threshold negative polarity pulses show the voltage will increase until \(-60\text{V}\) and begin to decay slowly until the voltage collapses and a large current spike is evident. Superthreshold pulses cause the voltage collapse to occur during the rising portion of the pulse. The breakdown voltage is far higher than the DC breakdown threshold. No failures were recorded below \(-100\text{V}\), visible "white" failures were observed between \(-100\text{V}\) and \(-200\text{V}\) and visible "black" failures were observed at voltages above \(-200\text{V}\).

v) Devices from the I69X wafer have a much larger positive polarity ESD threshold than devices from the I69W wafer. The negative polarity thresholds are similar at around \(-100\text{V}\).

5.7 References


CHAPTER 6

DISCUSSION

6.1 Introduction

In this chapter, the results presented in chapter 5 will be discussed with reference to the parameters governing MESFET/MES diode ESD sensitivity. The possible burnout/degradation failure mechanisms will also be discussed and qualitative physical models for subthreshold/threshold failure will be presented.

6.2 Transmission Medium Effects

The transmission line between the AutoZap and the load has a fixed capacitance to earth, which will have a minimum reactance which depends on the frequency of the rising portion of the pulse. This reactance appears in parallel with the load resistance, reducing the effective resistance external to the AutoZap. The overall effect is to lower the peak voltage and current to approximately 26V and 18mA at the 1.5kΩ load. From table (5.1), it can be seen that, at the lower values of load resistance, the effects of the transmission line will be minimised. The flying lead system shows peak voltage and current values of 33V at 28mA for the 1.5kΩ load. These values are larger than those measured for the coaxial system, but still below the maximum peak values of 50V and 33mA predicted for a simple resistive load. This implies that a large stray capacitance to earth is also present in this system, though it is smaller than the fixed capacitance of the coaxial system. The decay time constant associated with the flying lead system is shorter than that for the coaxial system, but neither system yields true exponential decay profiles. Therefore, care must be taken when considering the profile of any waveforms derived from these systems.
6.3 MESFET Degradation

6.3.1 Voltage and Polarity Effects

Changes in the MESFET $I_{ds}$ vs $V_{ds}$ characteristics indicate damage to the structure has taken place during the ESD pulse. These changes can range from small shifts in the $I_{ds}$ vs $V_{ds}$ curves, to complete catastrophic failure when the device no longer operates as a transistor and has linear $I_{ds}$ vs $V_{ds}$ characteristics. Each failure category, defined in section 5.4, represents a different level of degradation in the transistor. It should be noted that the large voltage ranges shown for each degradation category indicate that the extent of degradation caused by a particular pulse could not be predetermined.

*Category (1)* - The unchanged characteristics indicate that no damage has taken place within the structure which effects the normal operation of the MESFET.

*Category (2)* - The degradation in the $I_{ds}$ vs $V_{ds}$ characteristics indicate that the average channel current has decreased subsequent to an ESD pulse. No visual damage was associated with this type of failure, therefore these changes must be reasonably subtle.

The possible reasons for this type of degradation are:

a) The contact/source resistance has increased, causing an increased voltage drop in this part of the device, and therefore lowering the voltage actually applied to the channel. Regions of high current density within the ohmic contact are likely to increase the temperature, and hence increase the probability of diffusion of the ohmic metal(s), Ga or As during an ESD pulse. This type of failure mode has been previously reported for MESFETs subjected to accelerated lifetest[1-3] and pulse stress[4].

b) The cross-sectional area for current flow has decreased. This effect could be due to the elimination of interface oxides or changes in the interface
trap density which alters the Schottky barrier height, or by indiffusion of
the gate metal into the channel. An advanced stage of indiffusion is the
encroachment of the gate metal in the channel. This has been observed
in GaAs power MESFETs subsequent to lifetesting[5]

c) The net doping level has decreased in the channel thus decreasing the
numbers of free carriers available for conduction. This may be due to the
creation of traps in the active layer[6-9]. Accurate C-V measurements
would verify this effect.

d) The surface trap density in GaAs has been estimated to be in the order
of $10^{14}$ cm$^{-2}$. The presence of these traps may lead to unpredictable
effects on the channel current subsequent to a pulse if charge trapping has
taken place during a pulse.

**Category (3)** - This change in the $I_{ds}$ vs $V_{ds}$ characteristics indicates that the
average channel current has increased subsequent to an ESD pulse. The possible
reasons for this type of degradation are:

a) The contact/source resistance has decreased, causing an increased voltage
drop in this part of the device. This would increase $I_{dss}$ and $g_m$.

b) The cross-sectional area for current flow has increased. This effect could
be due to the elimination of interface oxides or changes in the interface
trap density which decreases the Schottky barrier height.

c) The net doping level has increased, thus increasing the numbers of free
carriers available for conduction. Again, accurate C-V measurements
would verify this effect.

d) Again, the presence of surface traps may lead to unpredictable effects on
the channel current if charge trapping has taken place during a pulse.
Category (4) - This type of failure indicates that the channel current at zero gate bias is similar to the that of an undamaged structure (category 1), but the degradation in the transconductance, and the visual damage between the gate and source contacts, indicates that a parallel gate-source leakage path has been created. At zero gate bias, the normal $I_{ds} \text{vs } V_{ds}$ characteristic occurs because no current is flowing through this parallel resistance. When the gate is biased, a current will flow from the gate circuit into the source contact, and add to the channel current. If the leakage resistance is low enough, as observed in the multiple pulse experiments, the voltage on the gate will tend toward zero. The device will thus exhibit very little gate control. This type of failure has serious implications to circuit designers.

Category (5) - The near linear $I_{ds} \text{vs } V_{ds}$ characteristics, and the visual damage between the gate and the drain, indicate that a parallel leakage path has been created between the gate and the drain. The current in the drain will now be a combination of the gate current, flowing directly into the drain, and the normal channel current. The potential at the gate will be controlled by the series combination of the compliance limit of the curve tracer and the drain leakage resistance. As the drain voltage rises, the gate will gradually be pulled positive and hence the channel current will flow into the drain leakage resistance, via the gate. The resulting current will now only be limited by the source part of the MESFET which has a higher saturation current as observed in section 5.3.3.

The failure statistics shown in figs. (5.20) and (5.21) indicate that major differences in the breakdown thresholds are evident when devices were subject to positive and negative polarity pulses. The positive polarity threshold was far higher than the negative polarity threshold. This has also been reported in other low noise GaAs structures[12,13]. This difference may be attributed to the changes in the Schottky depletion region under the two bias conditions[14].

A positive polarity pulse applied to the gate will forward bias the gate-source and gate drain MES diodes and, as a result there will be no depletion layer and so the device can be regarded as two semiconductor n-type resistors in parallel. In an ideal device Joule heating will heat up the whole of the channel
region uniformly. However, it is likely that "defect" regions, due to dislocations, impurities or localised regions of higher than average carrier density, will have a higher current density and therefore heat up to a far greater temperature and on subsequent cooling cause changes in the conduction properties at these points in the channel. Changes in the conduction properties at localised regions in the channel are unlikely to effect the $I_{ds}$ vs $V_{ds}$ to any significant extent. This is shown in the results where, for a large voltage range, only subtle (category 2 and 3) changes are evident with no damage on the surface of the GaAs or to the contacts. A number of pulses will cause cyclic heating and cooling of the "defect" regions within the channel, each pulse causing greater cumulative damage. This effect is clearly shown in the results in section 5.4.2 in which a gradual degradation in the $I_{ds}$ vs $V_{ds}$ characteristics occurred as a function of the number of pulses. This also shown in section 5.5.6 where the ESD threshold, for a fixed change in $I_{gs}$ vs $V_{gs}$ characteristics, is dependant on the number of applied pulses.

A negative polarity pulse will reverse bias the gate-source and gate-drain MES diodes. The majority of the voltage will build up across the high resistance depletion region until the field reaches $\approx 4 \times 10^5 \text{ Vcm}^{-1}$ when impact ionisation will commence. The current will then increase exponentially and burnout would be virtually instantaneous ($10^{-12}$s) relative on the time scale of an ESD pulse ($10^{-7}$s). Burnout will occur unless the current is limited by an external resistance(s) to the junction. In this case the majority of the voltage will transfer to the 1.5kΩ "body resistance" and so limit the current during the remainder of the pulse. Pulsing at voltages lower than the avalanche voltage will cause little change to the device because no significant power is dissipated during the pulse. It is possible, however, that charge trapping may occur at either the metal-GaAs interface region or at the surface causing small changes in the device $I_{ds}$ vs $V_{ds}$ characteristics.

### 6.3.2 Parametric Degradation

The results shown in tables (5.8) to (5.18) show that many DC characteristics of a MESFET change following an ESD pulse. The main features of these results are:
a) The relatively large variation which occurred within in the control groups were evident indicated the possibility of environmentally related degradation in the devices.

b) Positive polarity pulses tended to degrade a device over a large voltage range of +100V to +900V. Degradation was normally manifested by an increase in the channel resistance $R_{on}$ and decrease in the source resistance $R_s$. Negative polarity pulses at -100V tended to cause severe degradation of $R_s$ at 25°C.

c) Increasing the ambient temperature tended to increase the degradation of a device when subject to a positive polarity pulse, and decrease the burnout probability when subject to a negative polarity pulse.

In some cases, positive ESD voltages of less than +300V caused the source resistance, $R_s$, and channel resistance, $R_{on}$, to increase, and $I_{dss}$ to decrease accordingly. Above this voltage the source resistance, $R_s$, in virtually all cases decreased, indicating the presence of a significant gate-source leakage path. The low voltage effects on $R_s$ and $R_{on}$ indicate how category (2) failure characteristics may be attained. This is likely to be degradation of either the ohmic or channel resistance, which also appears to be enhanced significantly by an increase in the ambient temperature. In a number of cases the source resistance $R_s$ and channel resistance $R_{on}$ decreased, thus increasing the saturated drain current, $I_{dss}$ indicating how category (3) type characteristics may be obtained.

At positive ESD voltages, less than +300V, the interface characteristics improve as indicated by an increase in barrier height $V_{bi}$ and a decrease in the ideality factor, $n_r$. Above this voltage both parameters tend to degrade. In many cases the increase in barrier height was accompanied by a decrease in the pinch-off voltage $V_p$ again yielding category (3) failure characteristics.

In the many of the results, virtually all the parameters changed to some extent, thus making any definite conclusions regarding a dominating electrical failure mode difficult. It is likely that degradation in these devices is due to a combination of several failure mechanisms. If any one failure mechanism
dominates it is likely to be a function of an individual device's electrical and physical properties. If devices from a more mature fabrication process were available, with individually tailored structures to test for one particular failure mechanism, a study such as the above would reveal which failure mechanism is dominating failure at any particular voltage stress or polarity.

6.3.3 ESD Visible Failure Modes

The damage associated with a positive polarity pulse is generally far less, at a given voltage, than that caused under negative polarity stress. This is due to the majority of the positive polarity input power being dissipated in the channel where the increase in temperature is insufficient to cause damage. Therefore, a much larger overall power is required to cause a "defect" in the channel to rise to the critical temperature required for catastrophic damage. The damage, shown in fig. (5.23), appears to be confined to the channel near the edge of the gate. This is likely to be the point where the highest field had been attained during the pulse.

Once the avalanche voltage has been attained during a negative polarity pulse the current will begin to rise due to impact ionisation. It is likely that Joule heating within the depletion layer at the point of avalanche is sufficient to cause a rapid rise in temperature and lead to the formation of a melt channel. The subsequent damage, shown in fig. (5.24), extends across the channel and the ohmic contact also suffers damage.

6.4 MES Diode Degradation

In order to assess the ESD degradation characteristics of a single, well defined, portion of the MESFET, only the gate-source MES diode was used in subsequent experiments. These experiments also investigated the effects on ESD sensitivity of extrinsic parameters, such as ambient temperature and charge.
6.4.1 $I_{gs}$ vs $V_{gs}$ Degradation

6.4.1.1 Positive Polarity

Examination of the forward bias characteristics in fig. (5.25) show the source resistance increasing and the current saturation region decreasing as the positive ESD voltage increases. This indicates that the ohmic resistance and/or channel resistance is increasing subsequent to a pulse. The reverse characteristics in figs. (5.26) and (5.27) show the leakage current is increasing and avalanche voltage decreasing subsequent to a pulse. This indicates the creation of a resistive leakage path between the contacts. Generally pulses above $+1000\text{V}$ caused a localised visible "white" failure site between the gate and source contacts. This also acts as a high resistance path but with a much lower resistance than that observed at the lower pulse voltages as is indicated by the large leakage current in the reverse bias characteristic. This confirms the idea of a resistive path being created during an positive polarity ESD pulse.

It is interesting to note at this point, that using the failure criteria adopted by the AutoZap a failure is not registered, i.e a $2\mu\text{A}$ change in the diode current, until the ESD pulse voltage exceeded $+500\text{V}$ as demonstrated in fig. (5.27). This is due to the limited voltage sweep($+1\text{V}$ to $-10\text{V}$) carried out by the AutoZap curve tracer. In addition to the voltage limitations, the current is also limited to a maximum of $\pm100\mu\text{A}$, which normally limits the forward voltage to only $+0.3\text{V}$. Only if the complete $I_{gs}$ vs $V_{gs}$ characteristics are analysed can the electrical failure mode(s) be discovered. This demonstrates the limitations of using the AutoZap failure criteria as a basis of assessing breakdown.

6.4.1.2 Negative Polarity

Little change is observed in the $I_{gs}$ vs $V_{gs}$ characteristics subsequent to ESD pulses up to $-75\text{V}$. Above this value, the characteristics tended to become more resistive rather than showing gradually degrading properties as observed under positive polarity stress. This indicates that little damage is taking place to the device under $-75\text{V}$ and above this value the damage is sufficient to cause a resistive path to form between the contacts.
6.4.2 Interface Degradation

The changes at the metal-semiconductor interface can be assessed by measuring the barrier height and ideality factor subsequent to an ESD pulse.

Positive polarity pulses below +300V tended to slightly decrease the diode ideality factor and increase the barrier height. This implies that the interface properties are changing so as to improve the diode characteristics. This was also evident in the results in section 5.4.4 at the lower voltages. Pulses greater than +300V tended to degrade both the ideality factor and barrier height, due to the creation of a leakage path between the contacts. Eventually the leakage path would so dominate the electrical characteristics that the device would simply act as a resistor.

Negative polarity pulses degraded both parameters, but a slight decrease in ideality factor is evident at voltages less than -100V. This again indicates the interface properties are improving, but with no increase in barrier height.

These observations confirm the idea that category (2) characteristics may be partially due to an increase in built in voltage $V_{bi}$. This decreases the cross-sectional area for current flow at zero gate bias, thus decreasing $I_{ds}$ and $g_m$.

6.4.3 Temperature Effects

The positive polarity results, shown in fig. (5.33), indicate that the ESD threshold of the diode structure is highly sensitive to ambient temperature. The relationship shows a fairly linear decrease over the temperature range under investigation, as shown by the correlation coefficient of 0.947. Extrapolation of the regression line to the zero threshold voltage indicates the critical temperature to be $\approx 200^\circ$C. This is the temperature at which an infinitely small ESD pulse will fulfil the failure criteria of $2\mu$A. This critical temperature is lower than predicted for DC burnout by Wemple[15] who showed that the DC breakdown power threshold decreased linearly until $\approx 550^\circ$C, when the device entered a region of negative differential resistance. A similar critical temperature was suggested by Buot[16] for MESFET devices subject to ESD stress. The low extrapolated critical temperature in this study is likely to be a combination of the following effects:
a) It has been previously observed that the failure criteria adopted in this study may be fulfilled by a sub-burnout ESD pulse due to changes in the active layer or interface region. It is therefore likely that the observed temperature relationship is partially dependant on the susceptibility to degradation of the active layer, interface region or surface at increased temperatures. This effect is likely to have a lower critical temperature than for catastrophic failure.

b) The resistivity vs temperature relationship derived in section 2.4.3 shows that current will be impeded within the active layer until the temperature of the region reaches its intrinsic value \( \approx 875^\circ \text{C} \). If the heating of the active layer is extending into the substrate, which has an effective doping of \( 10^{13} \text{ cm}^{-3} \), the intrinsic temperature is closer to \( 300^\circ \text{C} \). Therefore, the lower critical temperature may be linked to the point at which the substrate current becomes significant.

The negative polarity results, shown in fig. (5.34) indicate that the voltage threshold increased as the ambient temperature was increased. The number of devices which degraded out of specification during the parametric degradation experiments also decreased as the ambient temperature was increased. This implies the critical voltage is increasing with temperature. It is likely that the device will not begin to dissipate sufficient power to damage the structure until the DC avalanche voltage has been reached. Baraff[17] has shown that the impact ionisation coefficients, i.e. the current multiplying factors, decrease as the temperature is increased due to a decrease in the mean free path of the avalanche electrons. This implies that the rate of current growth under avalanche conditions will be impeded by an increase in ambient temperature and requires a higher voltage to initialise/sustain impact ionisation. In the DC results shown in fig. (5.13) the avalanche voltage increases by \( \approx 4V \) for a \( 125^\circ \text{C} \) increase in temperature while the increase in ESD threshold voltage increased by \( \approx 20V \) over the same temperature range.
6.4.4 AutoZap Capacitance Effects

Increasing the AutoZap capacitance increases the available charge, and hence the energy contained in an ESD pulse. If the threshold voltage is linked to the total charge, or the total energy a decrease in the voltage threshold should be observed. In both sets of results, shown in fig. (5.35) and (5.36) a roughly inverse relationship between the threshold voltage and capacitance is observed. If the threshold is dependant on the total charge the threshold voltage will be given by:

\[ Q_{th} = CV_{th} \]  

(6.1)

Whereas if the threshold is dependant on the total energy \( V_{th} \) will be determined by:

\[ E_{th} = \frac{1}{2}CV_{th}^2 \]  

(6.2)

Hence, plotting the threshold voltage against AutoZap capacitance on logarithmic scales, a straight line of gradient -1 or -\( \frac{1}{2} \) indicates that the threshold voltage and capacitance is directly related to the total charge or energy in the pulse respectively. Fig. (6.1) shows these relationships. The results show that the positive polarity relationship has a gradient of -0.738 and a correlation coefficient of 0.977. Therefore, from these results, it is concluded that the positive polarity threshold relationship is neither solely dependant on the total charge or the total energy. The negative polarity relationship has a gradient of -0.185 and correlation coefficient of 0.792. This implies that the negative polarity threshold is relatively insensitive to the increase in capacitance.

The presence of the transmission line has also been found to effect the device voltage, as the capacitance is increased. This effect changes both the positive and negative polarity relationship shown in the results and is further discussed in section 6.4.5 and modelled in chapter 8.

Similar studies on the dependence of the ESD threshold voltage on the capacitance have been carried out by Huang[12]. In these results the capacitor was directly connected to the device under test and no "human body resistance"
Fig. (6.1) Log ($V_{th}$) vs Log (Capacitance)

- Positive polarity
  - Experimental Data
  - Regression line
- Negative polarity
  - Experimental Data
  - Regression line

$r = 0.792$
$m = -0.185$

$r = 0.977$
$m = -0.738$

Fig. (6.2) Reconstructed $I_{gs}$ vs $V_{gs}$ Characteristics ($C=100\text{pF}$ to $1000\text{pF}$)

- I69W MES Diode
- +100V ESD Pulse

$100\text{pF}$

$500\text{pF}$

$1000\text{pF}$

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was used. The capacitance was varied between 100pF and 1µF and both positive and negative polarity pulse thresholds were analysed. Huang's results show that the positive polarity threshold decreases linearly as the capacitance is increased from 100pF to 1µF when plotted on a log scale. The negative polarity threshold remains virtually constant between 100pF and 1000pF and then reduces by almost a decade at 1µF. These results compare favourably with the results presented in fig. (6.1) between 100pF and 1000pF.

6.4.5 Stress Waveform Analysis

Further information regarding the effects of an ESD pulse on a device can be obtained by measuring the voltage and current waveforms during an ESD event, provided that the measurement probes do not significantly load the discharge circuit. Under positive polarity stress the load resistance offered by the device is small compared to the impedance of the voltage probe, therefore the probe is unlikely to affect the results. However, under negative polarity stress the device impedance is in the same order as the voltage probe until the avalanche voltage is attained. Care must therefore be taken when interpreting the subthreshold negative polarity results.

6.4.5.1 Positive Polarity Subthreshold Effects

The main feature of the subthreshold positive polarity voltage waveforms is that they show a voltage plateau region at ≈5V for a large portion of a pulse. In order to obtain a clearer view of the $I_{gs}$ vs $V_{gs}$ relationship during an ESD pulse, the digitised voltage and current data from the oscilloscope can be analysed using the MathCad software package. This involves eliminating the time dependence from each waveform and reconstructing the current vs voltage relationship. The reconstructed $I_{gs}$ vs $V_{gs}$ characteristics of the results in figs. (5.45) and (5.46), with most of the initial ringing removed, are shown in fig. (6.2). This result can be compared to that in fig. (5.49) and clearly shows the $I_{gs}$ vs $V_{gs}$ relationship is similar to the DC relationship after the current re-enters the current saturation region and is independent of the "human body" capacitance. Thus it appears that even under ESD stress the $I_{gs}$ vs $V_{gs}$ relationship is partially
linked to the DC characteristics. The only major difference between the DC and the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics is that the voltage waveform exhibits a rapid rise of 1-2V just before the current re-enters the current saturation region. This rapid rise may be indicative of the device passing through a region of negative differential resistance (NDR) due to electron transfer from the lower to upper valleys in the conduction band. This is known as the transferred electron effect and is a feature of two valley semiconductors such as GaAs[18-20]. The reconstructed $I_{gs}$ vs $V_{gs}$ characteristics for various ESD pulse voltage are shown in fig. (6.3). These show that at each pulse voltage the current rises to a peak value dependant on the ESD charge voltage, but the $I_{gs}$ vs $V_{gs}$ relationships are similar throughout the decay portions of each pulse. Thus it appears that increasing the ESD charge voltage allows the device to be forced beyond the region of negative differential resistance into another region of positive differential resistance. The dynamic resistance in this region is very low and consequently the voltage waveform becomes largely independent of the device current. This type of behaviour has been observed in large area GaAs p-i-n diodes[21-23] and has been linked to the formation of current filaments under DC bias[24].

During ESD stress the electric field within the device exhibits fast transient changes and thus the electron dynamics under pulse stress cannot simply be linked to the quasi-static velocity-field characteristic shown in fig. (2.5) because the electrons must first acquire a kinetic energy at least equal to the energy separation between the central and the satellite valley(s). This leads to frequency limitations in any devices utilising the negative differential resistance effect. Rees[25] has shown that the dominant speed limitations of hot-electron effects in GaAs is the rate at which electrons can gain or lose energy in the central ($r$) valley of the energy band structure, rather than the intervalley scattering rate which is much faster. Kromer[26] has also discussed these effects and predicted relaxation times in the order of picoseconds. This means a GaAs device can easily respond to the transient field change over the time scale of an typical "human body" ESD pulse and hence the reconstructed current-voltage relationship can be linked to the DC characteristics during the later portion of the pulse.

The current profile during a pulse decays exponentially with a fixed time-
constant, except when the current enters the current saturation region, observed in all the DC $I_{gs}$ vs $V_{gs}$ characteristics, which gives rise to a "kink" in the waveform. The current decay time-constant must therefore be dependant on the $C_B \times R_B$ combination within the AutoZap, thus increasing the "human body" capacitance will allow the device to be sustained longer beyond the NDR region because the current will remain above the critical value for a longer time.

An increase in the ambient temperature increases the duration of the voltage plateau region as observed in fig. (5.51). This is due to the decrease in magnitude of the current saturation region, as observed in fig. (5.12). This allows a device will be sustained longer beyond the NDR region as the temperature increases.

6.4.5.2 Positive Polarity Threshold Effects

It is likely that the probability of failure is linked to the time and dissipated power whilst the device is sustained past the NDR condition in the region of positive differential resistance. Failure has been found to depend on the ESD charge voltage, external capacitance and ambient temperature.

The majority of the power is likely to be dissipated in the first few hundred nanoseconds of a pulse and this is clearly shown in fig. (6.4). This shows the power profiles associated with increasing the ESD charge voltage for a range of values from +300V to +900V. The peak power increases as the ESD charge voltage is increased and the decay time-constant remains fairly constant.

When the charge in an ESD pulse is increased the duration of the voltage plateau region increases as shown in fig. (5.47). The decay time constant(s) of the current waveforms also increase as shown in fig. (5.48). Hence, the overall energy contained within the pulse increases. Fig. (6.5) shows the power profiles associated with increasing the available charge at a constant voltage of +100V. At the higher capacitance values the peak powers are similar, while the decay time constant increases. The peak power attained using the 100pF capacitor is $\approx 15\%$ lower. This effect is due to the presence of the transmission line. Consequently the power dissipated within the device, at a fixed ESD charge voltage increased with capacitance. This effect may partially explain the relationship observed in fig. (5.35).
The majority of the voltage failure waveforms, e.g. fig. (5.55), show a premature collapse in the profile after the peak power point had been attained. This indicates that the peak power is not the crucial parameter which controls the burnout threshold. It is more likely that the power profile is the controlling factor which determines the burnout threshold. The failure waveforms shown in figs. (5.55) and (5.56) have profiles which vary with the applied ESD charge voltage. Both pulses show a premature collapse of the voltage plateau region after only a few hundred nanoseconds, but the 1.5kV pulse shows a recovery in voltage after \( \approx 1\mu s \), while the 2.5kV pulse shows no such recovery. It is likely that in both cases, the critical temperature has been attained and a low resistance melt channel has been created. In the case of the 2.5kV pulse the power is sufficient to create a permanent resistive path between the gate and source contacts possibly by metallic diffusion or dissociation of the GaAs. In contrast the power profile of the 1.5kV pulse is insufficient to sustain the breakdown site at a temperature where metallic diffusion\dissociation has time to take place. It appears in this case that as the temperature decreases the breakdown site becomes effectively open circuit, i.e a resistive path of a few megohms. Hence the voltage can recover and follow a similar decay to that of an undamaged device. The \( I_g \) vs \( V_g \) characteristic subsequent to each pulse, showed a decrease in the current saturation magnitude, which indicates a small portion of the channel has become inoperative due to the creation of a high resistance region in the channel.

### 6.4.5.3 Negative Polarity Subthreshold Effects

Fig. (5.41) shows the effects of subthreshold ESD voltage pulses on a device. It is clear that ESD pulses of -25V and -50V only reach -15V and -30V respectively, at the device. This effect is due to the transmission line and will be discussed further in chapter 8. These lower voltages are therefore insufficient to cause impact ionisation which was observed in the DC results between -35V and -45V, see fig (5.44). Consequently, the decay time-constant for each of the voltage waveforms is in the order of 1\( \mu s \) and is dependant both on the AutoZap capacitance and the parallel combination of the voltage probe and the device. The decay time constant of the -75V pulse is slightly shorter implying the device...
is entering the impact ionisation condition at \( \approx -40V \). This is verified by the examination of the DC characteristics shown in fig. (5.44). Pulsing at -100V yields a peak voltage of -55V and an avalanche current which is sustained at -2mA for greater than 500ns. The dissipated power is now close to the maximum that could be sustained under DC conditions, i.e. 50-100mW.

Pulsing the device at a constant voltage of -50V and varying the AutoZap capacitance changes the device voltage profile. This effect is shown in fig. (5.47). The higher values of capacitance tend to swamp the effect of the transmission line and allow the device to receive the full ESD charge voltage. Thus, increasing the AutoZap capacitance allows a higher power to be dissipated in the device and consequently a lower charge voltage would be required to induce damage. This effect is therefore partially responsible for the trend in the results shown in fig. (5.36) which show the ESD threshold voltage decreases as the capacitance is increased. Increasing the ambient temperature increases the leakage current during a subthreshold pulse as observed in fig. (5.54) and the device voltage remains virtually constant with temperature, as expected.

Fig. (6.3) Reconstructed \( I_{gs} \) vs \( V_{gs} \) Characteristics
Fig. (6.4) Power Profiles as a Function of ESD Charge Voltage

Fig. (6.5) Power Profiles as a Function of AutoZap Capacitance
6.4.5.4 Negative Polarity Threshold Effects

Under negative pulse conditions the current is initially inhibited by the presence of the depletion layer. The voltage rises rapidly until breakdown occurs between -50V and -70V as shown in fig. (5.57). The failure waveform at -100V indicates that failure condition is not totally voltage dependant because the device failed during the decay portion of the pulse. But, it has been established in section 6.4.5.3 that little current flows until the voltage reaches the DC avalanche voltage (-40V to -50V) after which it rises rapidly. The device now begins to dissipate significant power at the avalanche point(s) causing the local temperature to rise. At this stage the depletion layer will remain stable until a critical temperature is reached, when it collapses, allowing the charge built up on the depletion layer capacitance to discharge limited only by the 1.5KΩ body resistance. Superthreshold pulses simply cause the device to fail earlier in the pulse.

The increase in device voltage towards the end of a negative polarity ESD pulse between -100V and -200V implies that the device resistance is increasing. This enables the depletion layer to become re-established and the residual charge on the AutoZap capacitance to build up on the depletion layer capacitance. Once again this is confirmed because all the devices which exhibited a recovery in voltage were observed to have "white" failure sites with degraded $I_{gs}$ vs $V_{gs}$ characteristics subsequent to the pulse. At ESD voltages above -200V no recovery was generally evident indicating a permanent low resistance path between the contacts had been created. This again is confirmed because devices pulsed above -200V generally had "black" failure sites and near linear $I_{gs}$ vs $V_{gs}$ characteristics.

6.4.6 Wafer Threshold Comparison

The only measurable differences between the 169W and 169X wafers were the depth of the n-type layer, the contact resistance and the transfer length. Fig (6.6) shows the $N_d$ vs depth profiles, courtesy of STC Technology Ltd, before fabrication of the MESFET structures. The doping densities show roughly
gaussian profiles with the I69X wafer showing a higher donor density than the I69W wafer at any depth. The n-type layer depth, as estimated in section 5.3.1 was 0.158μm (I69W) and 0.166μm (I69X) based on a constant doping level of 10^{17} cm^{-3}. These values compare favourably with values taken from fig. (6.6). The contact resistance of typical devices on each wafer can be estimated from the characteristics of the ohmic test patterns. These characteristics also provide an estimate of the transfer length and contact resistance (see section 2.7.2.2). Fig. (6.7) and (6.8) show the contact spacing vs measured resistance plot for both the structures. These results show the lower contact spacings have a lower resistance than expected in both sets of results. This was traced to the poor quality of the ohmic edges which had visible metallic bridges between the contacts. The higher contact spacings have therefore been used to estimate the contact resistance and transfer length. These are R_c = 33Ω (I69X), R_c = 24Ω (I69W), L_t = 4.75μm (I69X) and L_t = 2.14μm (I69W). These values are quite high and may be effected by the presence of the surface depletion layer[27].

Fig. (5.37) indicates that for the I69X wafer the positive polarity threshold is higher than for the I69W wafer. In addition the I69X wafer has the larger n-type layer depth, contact resistance and transfer length. The difference in the positive polarity threshold is also demonstrated in fig. (5.61), in which "white", high resistance, failures were observed subsequent to a +1500V ESD pulse for the I69X devices, while the I69W devices showed "black", short circuit, failures at the same voltage. It will be shown in chapter 7 that the positive polarity EOS threshold may be linked to the depth of the n-type layer and transfer length. If the threshold is again dependant on these variables under ESD conditions, then a device with a larger n-type layer depth and transfer length will have a higher positive polarity ESD threshold. However, the differences in the n-type layer depth, transfer length and even the n-type carrier density are fairly small and unlikely to give rise to the large difference in threshold observed. It is therefore likely that a more fundamental reason, related to the fabrication process, is responsible for the observed results. Without further detailed information on the fabrication of these particular wafers it is difficult to draw any definite conclusions for the difference in positive polarity threshold between the wafers.

Little difference in the negative polarity threshold is observed between the wafers. It has been established earlier in this chapter that the negative polarity
threshold is linked to the DC avalanche voltage. Figs. (5.10) and (5.11) show that the I69X devices have a larger overall spread in the reverse breakdown voltage. From fig. (5.10) the average reverse breakdown voltage $-V_{br}$ is between -20V and -30V. This would imply that the I69X wafer should, on average, have a lower negative polarity ESD threshold voltage. Fig. (5.38) shows this not to be the case. However, it is possible that the results shown in fig. (5.38) have been taken from a section of the I69X wafer which had a higher than average DC breakdown voltage. This cannot be confirmed since this portion of the wafer has since been damaged.

**Fig. (6.6) $N_d$ vs Depth Profiles for the I69W and I69X wafers**
Fig. (6.7) Ohmic Transfer Length Measurement for the I69W wafer

\[ R_C = 23\Omega \]
\[ L_t = 2.14\mu m \]

I69W Test Structure

Fig. (6.8) Ohmic Transfer Length Measurement for the I69X wafer

\[ R_C = 33\Omega \]
\[ L_t = 4.75\mu m \]

I69X Test Structure
6.5 Summary

It has been established that GaAs MES devices are sensitive to ESD pulses. Two qualitative breakdown models have been proposed which depend on the polarity of the applied ESD pulse.

In general, at the lower ESD voltages, degradation in the device I/V curves indicates that subtle changes are occurring to the device during an ESD pulse. These changes are likely to be a result of changes in the channel or metal-semiconductor interface properties. The presence of surface depletion layers may also be influencing sensitivity. In many cases, subsequent to a pulse, a device still operates as a transistor and would therefore not fail simple screening tests. These devices may fail later in life when operating under normal conditions in the field and these are known as latent failures. Failures of this kind have also been observed in Bipolar devices subject to subthreshold ESD pulses [28]. At the higher ESD voltages, visible "white/black" failure sites are characteristic of high/low resistance short circuits between the closest two contacts. "White" type failures can be detected during an ESD pulse as a collapse in the device voltage with a subsequent recovery later in the pulse. In contrast, "black" type failures show no such recovery.

Examination of the device waveforms during an ESD pulse has shown that under positive polarity ESD stress the device exhibits characteristics similar to those reported for current-controlled negative differential resistance due to inter-valley electron transfer [18-20]. This type of effect has been utilised in the generation of microwave radiation as exhibited in Gunn devices [29]. Thermal breakdown under forward bias stress is linked to the dissipated power profile when the device is operating in the region of positive differential resistance and failure will occur at specific points in the channel due to the formation of current filaments [21,24].

Under negative polarity stress the device current is inhibited by the depletion region until the DC avalanche voltage is attained. The current then increases until sufficient power has been dissipated within the device to induce thermal failure, at which point the voltage collapses.
6.6 References


CHAPTER 7

THERMAL MODELLING

7.1 Introduction

It has been established in chapter 6 that thermal runaway within localised regions of a device is the final destructive ESD failure mechanism in GaAs MES devices. During positive polarity overstress, it is the dissipated power profile, whilst the device is operating in the region of positive differential resistance, which determines if a device will reach the critical temperature for thermal failure. During negative polarity overstress, the DC avalanche voltage must be attained in order for sufficient current to flow in the device to initialise joule heating and eventual thermal failure. It has also been established in chapter 3 that no literature exists on the application of semiconductor thermal breakdown models, such as the 1-dimensional Wunsch & Bell[1] and symmetric 3 dimensional Tasca[2] model, to predict the thermal failure threshold in GaAs devices. It is therefore the purpose of this chapter to study existing thermal breakdown models and to apply these to GaAs MES devices. As part of this study a more versatile three dimensional thermal model is presented which can be used to predict the EOS\ESD thermal breakdown threshold in many semiconductor devices.

7.2 EOS Thermal Breakdown Modelling

In the past, thermal runaway in semiconductor devices has been modelled by a localised heat source, \( P(t) = V(t)I(t) \), throughout a defect region \( \Delta \). The heat generated inside \( \Delta \) raises the temperature at its "centre" (the hottest point) to some critical value \( T_c \) at which point breakdown occurs. \( T_c \) may be a melt,
dissociation or other critical temperature. These are the essential features of thermal breakdown. For the thermal analysis described in this study, it is convenient to define a "defect" in terms of three lengths $a$, $b$ and $c$. These are defined as the lengths of the principle axes of the "defect" and are taken in the order $c \leq b \leq a$.

The earliest analytical models reported for thermal breakdown in semiconductor devices are those of Wunsch and Bell[1] and Tasca[2]. Wunsch and Bell described junction breakdown in Si p-n diodes and transistors under constant power stress by a simple one-dimensional heat flow analysis. In this model the pulse power $P_f$ and time to failure $t_f$ are related by

$$P_f = \left( \pi K \rho C_p A_j \right)^{\frac{1}{2}} \left( T_C - T_o \right) \frac{1}{t_f}$$  \hspace{1cm} (7.1)

where $K$ is the thermal conductivity, $\rho$ is the density, $C_p$ is the specific heat capacity, $A_j$ is the junction area and $T_a$ is the temperature of the surrounding ambient. Two values for the critical temperature ($T_c$) were considered, i.e., 1415°C, the melt temperature of Si, and 675°C.

In the Wunsch and Bell model, for a p-n junction under reverse bias, the "defect" was postulated to be the full junction area, or 10% of the junction area. In this case $c$, the width of the depletion region, is zero and the effective junction area, $A_j = a \times b$, is infinite. Despite these rather stringent conditions the Wunsch and Bell model seems to fit existing experimental data for a wide range of microelectronic components[3,4].

Part of the reason for the success of the Wunsch and Bell model was demonstrated by Tasca[2]. Tasca derived a thermal model in which the defect may be regarded as a sphere immersed in an infinite medium at the ambient temperature. Again, when the temperature of the defect reaches the critical temperature, $T_c$, breakdown occurs. In this case, the $P_f$ vs $t_f$ relationship are given by:

$$P_f = \left( \frac{\rho C_p \Delta}{t_f} + \left( \frac{K \rho C_p A_j}{t_f} \right)^{\frac{1}{2}} + \frac{8nKr}{3} \right) \left( T_C - T_o \right)$$  \hspace{1cm} (7.2)

Here $\Delta$ is the defect volume, $S$ is the defect surface area and $r$ is the defect "radius". It is customary to divide time into three domains. For small failure
times, typically below 10 ns, little heat is lost from the surface so that the (adiabatic) $t_f^{-1}$ term dominates. For very large failure times, typically above 100 $\mu$s and after thermal equilibrium has been established, the constant or steady state term dominates. During the intermediate time domain the middle term in eqn. (7.2) dominates. This is the Wunsch and Bell term. The overall pulse power vs time to failure relationship is shown schematically in fig. (7.1).

It is clear from eqns. (7.1) and (7.2) that the relationship between pulse power and time to failure depends quite strongly on defect geometry. This is confirmed by the more recent work of Arkhipov et al[3] who considered thermal failure induced by a defect in the form of a long cylinder, i.e. $c = b$, with $a >> b$. In this case, for sufficiently large failure times (but before the steady state is reached), and under a constant power stress, the $P_f$ vs $t_f$ relationship becomes

$$P_f = \frac{4\pi a (T_c - T_o)}{\left[ \log_e \left( \frac{t_f}{b^2/4\pi D} \right) + \log_e \left( \frac{4}{\pi} \right) \right]}$$

(7.3)

This logarithmic regime has seldom been reported in the literature. Most experimental data seems to fit a curve of the type depicted in fig. (7.1) quite well, even though the defects are unlikely to have the geometry required by eqns. (7.1) - (7.3).

For a general defect a problem arises in this treatment. While the volume and the surface area of any shape are well defined, the radius, $r$, is not. This ambiguity leads to difficulties in the application of eqn. (7.2) to large failure times. The uncertainty in $r$ leads to an uncertainty in the constant power or steady state term which then must be considered separately.

Existing thermal models are normally based on constant power pulses. An extension to arbitrary power profiles, such as those observed in ESD thermal breakdown, may be achieved by use of the Duhamel formula[5], which arises here as a natural consequence of the Green's function formalism. An additional complexity arises since the material parameters $K$ and $C_p$ are sometimes quite strongly temperature dependent. Ash[6] has shown that, in certain cases, the variations in $K$ and $C_p$ with temperature do not alter the overall pulse power $P_f$ vs $t_f$ relationship. In most previous thermal models, as here, this dependence has
therefore been neglected.

7.2.1 Theory

The channelling of the current by the defect causes a Joule heating source $P(t) = V(t) I(t)$ throughout a defect, $\Delta$. The temperature distribution $T(r,t)$ in the vicinity of the defect is given by the solution to the heat transfer equation[9]:

$$\frac{\partial T}{\partial t} - D \nabla^2 T = \frac{q(t)}{\rho c_p}$$

(7.4)

where $D = K/\rho c_p$ is the thermal diffusivity and $q(t)$ is the rate of heating per unit volume ($= P(t)/\Delta$ inside $\Delta$ and 0 outside $\Delta$). This is the general starting point for thermal runaway models in semiconductors. It has been assumed that the heat is generated uniformly throughout $\Delta$. No serious difficulties arise in the theory if this assumption were dropped.

In the case of constant input power, $P_o$, the steady state term $T_{ss}$ may be calculated separately from the steady state heat equation:

$$- D \nabla^2 T_{ss} = \frac{P_o}{\rho c_p \Delta}$$

(7.5)

Eqn. (7.5) is Poisson's equation and consequently has the solution:

$$T_{ss}(r) = T_o + \frac{P_o}{k \Delta} \int_\Delta \frac{dr'}{4 \pi |r - r'|}$$

(7.6)

In order to use Tasca's expression, eqn. (7.2), for a general defect the correct steady state term must first be calculated from eqn. (7.6) by defining the appropriate geometry $\Delta$.

The Green's function for the heat equation, i.e. the solution to the equation:

$$\frac{\partial G}{\partial t} - D \nabla^2 G = \delta(r-r') \delta(t-t')$$

(7.7)

is the three dimensional Gaussian:
Thus, the solution to the general time varying problem, eqn. (7.4), may be written as an integral over both time and the defect volume:

\[ T(\mathbf{r}, t) = T_o + \int_0^t \frac{P(\tau)}{\rho C_p \Lambda} \frac{d\mathbf{r}'}{[4\pi D(t-\tau)]^{3/2}} \exp \left\{ \frac{-(\mathbf{r}-\mathbf{r}')^2}{4D(t-\tau)} \right\} \]  

(7.9)

where \( T_o \) is the temperature of the surrounding ambient. We assume that the defect has a well defined "centre", or hot spot, at \( \mathbf{r} = \mathbf{0} \). The temperature at this centre is then given by:

\[ T(\mathbf{r}, t) = T_o + \int_0^t \frac{P(\tau)}{\rho C_p \Lambda} \frac{d\mathbf{r}'}{[4\pi D(t-\tau)]^{3/2}} \exp \left\{ \frac{-(\mathbf{r}-\mathbf{r}')^2}{4D(t-\tau)} \right\} H(\mathbf{r}, t-\tau) \]  

(7.10)

where

\[ H(\mathbf{r}, t) = \frac{1}{4\pi K\Lambda} \int_\Delta \text{erfc} \left( \frac{\mathbf{r}-\mathbf{r}'}{2\sqrt{4tD(t-\tau)}} \right) d\mathbf{r}' \]  

(7.11)

and \( \text{erfc}(x) \) is the complementary error function.

Clearly if \( P(t) \) is independent of time, i.e. \( P = P_o \), then:

\[ T(\mathbf{r}, t) = T_o + P_o H(\mathbf{r}, t) \]  

(7.12)

In the limit of \( t \to \infty \) the steady state term becomes \( T_{ss} = T_o + P_o H(\infty) \) which becomes identical to eqn. (7.6) upon setting \( \mathbf{r} = \mathbf{0} \).

Eqns. (7.10) and (7.12) represent the Duhamel formula which may be used to analyse the heating effects of an arbitrary power profile based on a knowledge of constant power results, e.g. Tasca [5].
The $P_f$ vs $t_f$ time relationship derived from eqn. (7.12) yields:

$$P_o(t_f) = \frac{T_C - T_o}{H(t_f)}$$

(7.13)

i.e. $P_o$ becomes an implicit function of $t_f$. Substituting this expression into eqn. (7.10) gives:

$$\frac{T(t) - T_o}{T_C - T_o} = \int_0^t P(\tau) \frac{d}{d(t-\tau)} \left\{ \frac{1}{P_o(t-\tau)} \right\} d\tau$$

(7.14)

Thus the criterion for thermal breakdown under a time varying pulse is:

$$1 = \int_0^{t_f^o} P(\tau) \frac{d}{d(t_f^o-\tau)} \left\{ \frac{1}{P_o(t_f^o-\tau)} \right\} d\tau$$

(7.15)

where $t_f^o$ is the time to failure for the time varying power pulse[5].

Eqns. (7.13) and (7.15) provide the burnout criteria for constant and time varying power pulses respectively. For constant power pulses the $P_f$ vs $t_f$ relationship has been obtained for defects in the form of an infinite plane[1], a sphere[2] and an infinite cylinder[3], eqns. (7.1) - (7.3) respectively. These expressions follow automatically from eqns. (7.13) and (7.14) by specifying the appropriate defect geometry $\Delta$. The geometry of planar devices is not very well represented by any of these high symmetry geometries. This is especially true for diode structures under forward bias. The defect region in these planar devices is more closely represented by a rectangular parallelepiped with side lengths $a$, $b$ and $c$.

The $P_f$ vs $t_f$ relationship for this geometry may be obtained from eqn. (7.9) at an arbitrary point $r = (x,y,z)$. For constant power pulses, integrating $\mathbf{r}$ over the ranges $-a/2 \leq x \leq a/2$, $-b/2 \leq y \leq b/2$ and $-c/2 \leq z \leq c/2$, yields:
\[
T(\xi, t) = T_0 + \frac{P_o}{\rho C_p \Delta} \int_0^t G(x, a, \tau) G(y, b, \tau) G(z, c, \tau) d\tau
\]  
(7.16)

where
\[
G(x, a, \tau) = \frac{1}{2} \left( \text{erf} \left( \frac{a + x}{2\sqrt{4\tau D\tau}} \right) + \text{erf} \left( \frac{a - x}{2\sqrt{4\tau D\tau}} \right) \right)
\]  
(7.17)

The function \( G(x, a, \tau) \) describes one dimensional heat diffusion in an infinite medium for a constant heat source in the range \(-a/2 \leq x \leq a/2\).

Equation (7.16), for the three dimensional problem, is just the product solution. The temperature at the centre of the defect is obtained by setting \( r = 0 \). Thus:

\[
T(\xi, t) = T_0 + \frac{P_o}{\rho C_p \Delta} \int_0^t \text{erf} \left( \frac{a}{4\sqrt{4\tau D\tau}} \right) \text{erf} \left( \frac{b}{4\sqrt{4\tau D\tau}} \right) \text{erf} \left( \frac{c}{4\sqrt{4\tau D\tau}} \right) d\tau
\]  
(7.18)

At this point it is convenient to define diffusion times related to \( a \), \( b \) and \( c \) as follows:

\[ t_a = a^2/4\pi D, \quad t_b = b^2/4\pi D, \quad t_c = c^2/4\pi D. \]

These represent approximate times for thermal equilibrium to be established in the \( x \), \( y \) and \( z \) directions respectively. Thus, since \( c \leq b \leq a \), the device reaches complete thermal equilibrium after a time of approximately \( t_a \). The three diffusion times divide the time domain into four time domains. A good estimate of the value of the integral in eqn. (7.14) by approximating the error functions in the following way

\[
\text{erf}(x) \approx \begin{cases} 
2x/\sqrt{\pi} & \text{if } x \leq \sqrt{\pi}/2 \\
1 & \text{if } x \geq \sqrt{\pi}/2.
\end{cases}
\]  
(7.19a&b)

The approximation given by eqns. (7.19a&b) is excellent except in the range \( 0.22 < x < 1.82 \) and is within 1% even in this range.
Hence, for example:

\[
\text{erf}(c/4(Dt)^{1/2}) \approx \begin{cases} 
(t_c/t)^{1/2} & \text{if } t \geq t_c \\
1 & \text{if } t \leq t_c
\end{cases}
\]  

(7.20a)  

(7.20b)

**Region I**

During the time interval \(0 \leq t \leq t_c\) all the error functions are approximately equal to one, thus:

\[
T(\varphi, t) = T_0 + \frac{P_o}{\rho C_p abc} \int_0^t dt
\]  

(7.21)

Consequently, if failure occurs in this time interval, one obtains:

\[
P_f = M C_p (T_c - T_0)/t_f
\]  

(7.22)

for the pulse power/time to failure relationship. Here \(M\) is the mass of the defect. It is clear that there exists an adiabatic or \(1/t_f\) time dependence which persists until the characteristic time \(t_c\).

**Region II**

Beyond \(t_c\), in the time range, \(t_c \leq t_f \leq t_b\), the error function which describes heat flow in the z direction departs from its asymptotic value of one and enters the linear region given by eqn. (7.19a). During this time interval:

\[
T(\varphi, t) = T_0 + \frac{P_o}{\rho C_p abc} \left\{ \int_{t_c}^{t} \sqrt{\frac{t}{t_c}} dt + \int_{0}^{t_c} dt \right\}
\]

\[
= T_0 + \frac{P_o}{\rho C_p abc} \left[2 \sqrt{t_c t} - t_c \right]
\]  

(7.23)
Thus, the $P_f$ vs $t_f$ relationship becomes:

$$P_f = \frac{ab \sqrt{nK\rho C_p}}{\sqrt{t_f} - \sqrt{t_c}/2} \left( T_C - T_0 \right)$$  \hfill (7.24)

which reduces to the Wunsch-Bell dependence if $t_r$ is much larger than $t_c/4$; this condition holds if $c$ is small, as is the case for a reversed biased p-n junction.

**Region III**

At still larger times, in the range $t_b \leq t_r \leq t_a$, thermal equilibrium exists in both the y and z directions at which point the corresponding error functions (containing $b$ and $c$) enter the linear region eqn. (7.19a). The temperature in this interval is given by:

$$T(\varnothing, t) = T_0 + \frac{P_0 \sqrt{t_c t_b}}{\rho C_p a b c} \left\{ \log_e \left( \frac{t}{t_b} \right) + 2 - \frac{c}{b} \right\}$$  \hfill (7.25)

which may be compared to the expression given by Arkhipov et al., eqn. (7.3) [5]. The $P_f$ vs $t_f$ relationship for thermal breakdown in this time domain becomes:

$$P_f = \frac{4\pi K a (T_C - T_0)}{\log_e \left( \frac{t}{t_b} \right) + 2 - \frac{c}{b}}$$  \hfill (7.26)

**Region IV**

Finally, for times greater than $t_a$, all of the error functions are in the linear region, eqn. (7.19a), hence:

$$T(\varnothing, t) = T_0 + \frac{P_0 \sqrt{t_c t_b}}{\rho C_p a b c} \left\{ 2\log_e \frac{a}{b} + 4 - \frac{c}{b} - 2 \sqrt{\frac{t_a}{t}} \right\}$$  \hfill (7.27)
In this case, if the critical temperature $T_c$ is reached, the $P_f$ vs $t_r$ relationship is given by:

$$P_f = \frac{2\pi k a}{\log_e \left( \frac{a}{b} \right) + 2 - \frac{c}{2b} - \sqrt{\frac{t_a}{t_f}}} (T_c - T_o)$$  \hspace{1cm} (7.28)$$

Thus, for sufficiently large times $P_f$ becomes constant and we obtain the familiar steady state $P_f$ vs $t_r$ dependence.

It is clear from the above analysis that there are four separate time domains for a device of any shape. This is contrary to the analysis of Arkhipov who concluded that a logarithmic dependence of the form in eqn. (7.25) indicates a needle shaped "defect" while a Wunsch & Bell dependence, such as given by eqn. (7.23), indicates a disc shaped "defect". The analysis presented here shows that the true power vs time relationship, at least within the validity of thermal models, should display all four time dependencies. If one type dominates it is a consequence of the device dimensions, certainly, but also of the power in the pulse and the material parameters $\rho$, $C_p$ and $K$. This can be seen from fig. (7.2) which shows the increase in temperature $T(t) - T_0$ with time in a GaAs planar diode with assumed "defect" dimensions of 0.16 $\mu$m x 1.0 $\mu$m x 10.0 $\mu$m subject to a constant input power of 0.2W[8]. The thermal diffusivity, $D = 3.76 \times 10^{-6} \text{m}^2 \text{s}^{-1}$ [calculated from ref. [11] at the melt temperature of GaAs], the critical times are $t_c = 0.54 \text{ns}$, $t_b = 21.17 \text{ns}$ and $t_a = 2.12 \mu$s.

Fig. (7.2) shows the four regions (I-IV). These are made clearer from the $\log(P_f)$ vs $\log(t_f)$ and $1/P_f$ vs $\log(t_f)$ plots shown in figs. (7.3) and (7.4). All four time regions exist for a defect of any shape, it is the duration for which these regions exist which are dependent on the actual defect geometry. It now becomes easy to understand the results obtained in references [1-3]. In the case of reference [1] $a$ and $b \rightarrow \infty$ and $c = 0$, consequently regions I, III and IV are all missing leaving only the Wunsch and Bell or $t^{3/2}$ dependence. Similarly, if $a = b = c$ (as in ref. [2]), regions II and III are missing thus one is left with the linear region (eqn. (7.19a)) and the steady state region, eqn. (7.25). The $t^{3/2}$region which occurs in ref. [2] arises from the way in which thermal equilibrium is approached in eqn. (7.25). Finally, for the infinite cylinder ($a \rightarrow \infty$ and $b = c$), only regions I and III (the logarithmic region) are obtained, as found by Arkhipov et al [3].
If all four regions are present, then estimates of the values of \(a\), \(b\) and \(c\) can be obtained from the transition times between the regions. Several additional relationships between these parameters may also be obtained from experimental data. First, if region I is fitted to \(P_t = At^{-1}\) and region II is fitted to \(P_t = Bt^{-\frac{1}{2}}\) then \(c\) is given by \(c = (\pi D)^{\frac{1}{2}}(A/B)\). Second, the extrapolated \(1/P_t = 0\) intercept of the logarithmic region, \(t = t_o\), is related to \(b\) by \(b = e(4\pi Dt_o)^{\frac{1}{2}}\). Finally, we may relate \(a\) and \(T_c\) to the steady state power, \(P_{\infty}\), and the slope of the \(1/P_t\) vs \(\log(t_f)\) curve, \(\delta\), by \(a = b \exp(1/(2\delta P_{\infty})-2+c/2b)\) and \(T_c = T_o + (4\pi K\delta)^{-1}\). These extra relationships provide consistency checks for \(a\), \(b\) and \(c\).

The approximation which we have used for the error function is excellent (i.e. within 1%) except in the range \(0.22 \leq x \leq 1.82\). Within this range the errors are more significant and as a consequence there is a finite transition region between each of the four time domains. The times \(t_o\), \(t_b\) and \(t_c\) should therefore be obtained from the intersection of the linear extrapolation from adjacent region. Table (7.1) shows the relationships which arise from the theory.

Table (7.1) - Analytic Relationships between Experimental Data and the 3-dimensional Thermal Model

<table>
<thead>
<tr>
<th>Relationship</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) (c = (4\pi D t_c)^{\frac{1}{2}})</td>
<td>(t_c) is the intersection time between extrapolated regions I and II</td>
</tr>
<tr>
<td>(2) (b = (4\pi D t_b)^{\frac{1}{2}})</td>
<td>(t_b) is the intersection time between extrapolated regions II and III.</td>
</tr>
<tr>
<td>(3) (a = (4\pi D t_a)^{\frac{1}{2}})</td>
<td>(t_a) is the intersection time between extrapolated regions III and IV.</td>
</tr>
<tr>
<td>(4) (c = (\pi D)^{\frac{1}{2}}(A/B))</td>
<td>(A) and (B) are the coefficients of the (t^{-1}) and the (t^{-\frac{1}{2}}) regions.</td>
</tr>
<tr>
<td>(5) (b = e(4\pi Dt_o)^{\frac{1}{2}})</td>
<td>(t_o) is the intercept on the (t_f) axis of the (1/P_t) vs (\log(t_f)) plot.</td>
</tr>
<tr>
<td>(6) (a = b \exp(1/(2\delta P_{\infty})-2+c/2b))</td>
<td>(\delta) is the slope of the (1/P_t) vs (\log(t_f)) plot and (P_{\infty}) is the steady state power.</td>
</tr>
<tr>
<td>(7) ((T_c-T_o) = (4\pi K\delta)^{-1})</td>
<td>(\delta) is the slope of the (1/P_t) vs (\log(t_f)) plot.</td>
</tr>
</tbody>
</table>
Fig. (7.1) Log Input Power vs Failure Time

Fig. (7.2) Temperature Rise vs Log Failure Time for a GaAs Diode
Fig. (7.3) Log Input Power vs Failure Time

![Log Input Power vs Failure Time](image)

Fig. (7.4) 1/Input Power vs Failure Time

![1/Input Power vs Failure Time](image)
7.3 Analysis of Existing Experimental Data

7.3.1 Wunsch & Bell Data on 2N2222 Transistors

Experimental data on the 2N2222 transistor drawn from the ref [1], are shown in figs. (7.8) and (7.9). The only criteria used to select the data was that the data should be taken over as large a time range as possible and that the scatter about any underlying trend be as little as possible.

The device fails as a result of thermal runaway at the junction, during a reverse bias condition between two of the electrodes. The data shows a clear $t_1$ dependence at $t_e < 400\text{ns}$, and a $t_e^{-t_2}$ dependence for failures at $t_e > 400\text{ns}$. The characteristic times $t_2$, $t_b$, and $t_a$ can then be estimated at $400\text{ns}, \approx 100\mu\text{s}$ and $\approx 1\text{ms}$ respectively. Inclusion of these values into expressions (1),(2) and (3), with $D = 0.174 \text{ cm}^2\text{s}^{-1}$ yields $c = 9.35\mu\text{m}$, $b \approx 148\mu\text{m}$ and $a \approx 470\mu\text{m}$. The junction area used in the original Wunsch and Bell results was calculated to be $\approx 7.3 \times 10^4 \text{ cm}^2$, and the maximum area calculated by the new model is $\approx 6.95 \times 10^4 \text{ cm}^2$. The predicted value is quite close to that area originally used by Wunsch and Bell to obtain the best fit to their data.

7.3.2 Enlow data on Si ECL logic Gates

Experimental data taken from ref. [10] is shown in figs. (7.10) and (7.11). This failure data was obtained when the input pins of ECL logic gates were subjected to reverse bias pulses. The data shows the $t_1$ region at $t_e < 8\mu\text{s}$, the logarithmic region in the region $8\mu\text{s} < t_e < 100\mu\text{s}$, and the steady state region at $t_e > 100\mu\text{s}$. The characteristic times $t_b$ and $t_a$ can be then estimated as $8\mu\text{s}$ and $\approx 100\mu\text{s}$. Inclusion of these values into expressions (2) and (3), with $D = 0.174 \text{ cm}^2\text{s}^{-1}$ yields the values $b = 42\mu\text{m}$ and $a \approx 147\mu\text{m}$. This yields an maximum area of $\approx 6.17 \times 10^5 \text{ cm}^2$. This value, as expected, is smaller than the value calculated for the 2N2222 transistor.
Fig. (7.5)  2N2222 Log $P_f$ vs $t_f$ Data Plot

Fig. (7.6)  2N2222 $1/P_f$ vs $t_f$ Data Plot
Fig. (7.7) ECL Logic Gates \( \log P_f \) vs \( t_f \) Data Plot

Data reproduced from Enlow - ECL Logic gates

\[ r = -0.948 \]
\[ m = -0.48 \]

Fig. (7.8) ECL Logic Gates \( 1/P_f \) vs \( t_f \) Data Plot

Data reproduced from Enlow - ECL Logic gates

\[ r = -0.93 \]
\[ m = 0.073 \text{ W}^{-1} \]
7.4 Electrostatic Discharge Thermal modelling

7.4.1 Introduction

Electrical components must survive a wide range of electrical stress from high voltage transients, such as occur in electrostatic discharge (ESD) to the lower voltage constant electrical overstress (EOS). Each of these type of stress subjects a device to different current and voltage profiles, characterised by the peak values of $I_o$ and $V_o$. These waveforms combine to produce an instantaneous power profile $P(t)$ which will tend to heat the device and, under certain circumstances, induce thermal breakdown. For a given device, and a given type of stress environment, the thermal breakdown threshold, i.e. the least value of $I_o$ or $V_o$ which causes thermal breakdown, is a parameter of great importance to device manufacturers. However, despite considerable effort in this area over the past twenty years, there does not exist an expression for the breakdown threshold which is both simple and convincing. Some methods do exist for the determination of thresholds but they are either not simple, e.g. the thermal convolution integral technique[11], or not convincing, e.g. the average power method[12].

The breakdown threshold for an electrical component is determined by two competing processes. Energy is input to the component by the power in the pulse (tending to increase its temperature), and heat is lost to the surroundings by thermal diffusion (tending to decrease the temperature). In the case of subthreshold, constant power EOS stressing the temperature of a component rises continuously, asymptotically reaching a steady state value. Above the breakdown threshold, thermal diffusion is unable to carry the heat away from the component fast enough. Consequently, the temperature rises until it reaches some critical temperature (usually taken to be a melt temperature) at which point the component fails and breakdown is said to have occurred.

In the case of the transient pulses of ESD the temperature behaviour is, qualitatively, quite different. If the surroundings are at an ambient temperature $T_a$, the initial and final temperatures of the device must also be $T_a$. The temperature profiles above ambient, i.e. $T(t)-T_a$, for both EOS and ESD-type
Fig. (7.9) Constant Power Electrical Overstress (EOS) Temperature Profile

![Constant Power EOS Pulse](image)

Fig. (7.10) Electrostatic Discharge (ESD) Temperature Profile

![Exponential ESD Power Pulse](image)
pulses are shown, schematically, in figs. (7.9) and (7.10). The ESD profile, fig. (7.9), is easily understood in the following way. For short times there is sufficient power in the pulse to overcome the cooling effect of thermal diffusion so that the temperature of the component rises. For longer times, however, as the pulse decays, the diffusion losses dominate and the temperature of the component drops towards ambient.

The specific case considered here is for a GaAs MES device subject to an MIL-STD-883C ESD event defined by the Human Body Model[13]. The HBM models the effect of a human operator discharging accumulated static charge through a device to earth. In the equivalent circuit, shown in fig. (7.11), the capacitor $C_B$ (100 pF), which represents the human body capacitance, is charged to a voltage $V_0$ and discharged through the device via the human body resistance $R_B$ (1500Ω).

The main aim of ESD thresholding is to define a maximum peak voltage $V_{th}$ below which it safe to stress a particular class of device. For thermal breakdown, however, it is the power in the ESD pulse, $P(t)$, which does the damage as has been shown in chapter 6. Thus one must obtain, or assume, a relationship between the peak voltage $V_o$ (or current $I_o$) and the power $P(t)$ dissipated in the device.

Speakman[12] considered the case of breakdown of the emitter-base junction in bipolar silicon integrated circuits and obtained this relationship in the following way. Power is dissipated in the device by two mechanisms; firstly, because of the voltage drop $V_j$ across the junction and, secondly, due to the internal resistance $R_o$ of the bulk silicon. In the equivalent circuit, shown in fig. (7.12), it is assumed that both the junction voltage $V_j$ and the internal resistance of the bulk silicon $R_o$ may be taken as constants. This is not the case, and will be discussed further in section 7.7.1. This generic circuit model has now become the standard for thermal breakdown modelling[11,14,15]. With these assumptions simple circuit theory predicts an exponentially decaying current profile:

$$I(t) = I_o \exp \left(-\frac{t}{\tau}\right) \quad (7.29a)$$

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Fig. (7.11) Human Body Circuit Model

![Human Body Circuit Model Diagram]

Fig. (7.12) Device Circuit Model

![Device Circuit Model Diagram]
where

\[
I_o = \frac{V_o - V_j}{R_D + R_B} \tag{7.29b}
\]

\[
\tau = (R_D+R_B)C_B \tag{7.29c}
\]

and \(V_o\) is the voltage on the discharge capacitor. The instantaneous power dissipated in the device, at any time, is given by:

\[
P(t) = V_j I(t) + R_D I^2(t) \tag{7.30}
\]

\[
= V_j I_o \exp(-t/\tau) + R_D I_o^2 \exp(-2t/\tau) \tag{7.31}
\]

The "average power" method of reference [12] assumes that threshold breakdown occurs towards the end of the pulse, after a time 5\(r\). One then effectively replaces the pulse by a constant pulse of length 5\(r\) which contains the same average power as the true pulse over the failure time. If, for example, the device displays a Wunsch-Bell failure threshold[1,16], for constant electrical over stress, of the form:

\[
P_f = B t_f^{-\alpha} \tag{7.32}
\]

one compares the average power dissipated in the ESD pulse up to 5\(r\) with the Wunsch-Bell threshold for the same time. There is no real evidence to suggest that threshold failure occurs after 5\(r\) except that most (99\%) of the power is dissipated by that time. One may equally have chosen a failure time of 10\(r\). The validity of the method rests on an implied insensitivity of the result to the threshold time chosen. However, it is easy to see that the results are sensitive to the chosen time. Consider the average power in the double exponential waveform given by eqn. (7.31) over some time interval 0 \(\leq\) t \(\leq\) t\(_f\) where t\(_f\) > 5\(r\). To less than 1% error, one can write:

\[
P_{AV} = \frac{I_0 V_j}{t_f/\tau} + \frac{I_o^2 R_D}{2t_f/\tau} \tag{7.33}
\]

and the Wunsch-Bell power for the same failure time is:

\[
P_{WB} = B t_f^{-\alpha} \tag{7.34}
\]
According to the method in ref. [12], one equates the expressions for power in eqns. (7.33) and (7.34) and solves the resulting expression for I_o. As each of the powers P_{AV} and P_{WB} display different dependencies on t_f, respectively \( t_f^{-1} \) and \( t_f^{1/2} \), it is clear that the value of I_o obtained by this method will depend upon the value of t_f. It is also not the case that threshold failure occurs at or near the end of the pulse as will be seen later.

The same circuit model as shown in figs. (7.11) and (7.12), was implemented for ESD testing of 256K UVEPROMs by Pierce et al[11] who also extended it by using a combination of the full power profile of equation (7.31), rather than an average, and the Duhamel formula[5] which expresses the failure criterion as:

\[
\int_{0}^{t} P(\lambda) \frac{d}{d(t-\lambda)} \left[ \frac{1}{P_D(t-\lambda)} \right] d\lambda = 1 \quad (7.35)
\]

rather than occurring after some fixed time. Here P_D(t) is the damage threshold power of the device subjected to a rectangular pulse of width t. As in reference [12], Pierce et al[11] used the Wunsch-Bell formula for the constant power damage threshold. In this case the failure time, t_f, satisfies:

\[
\frac{I_o V_j \sqrt{\tau}}{D} \left[ \sqrt{\frac{t_f}{\tau}} \right] + \frac{I_o^2 B_D}{D} \sqrt{\frac{I_2}{2}} D \left[ \sqrt{\frac{2t_f}{\tau}} \right] - 1 \quad (7.36)
\]

where B is the Wunsch-Bell coefficient[13] and D(x) is Dawson's integral, defined by:

\[
D(x) = e^{-x^2} \int_{0}^{x} e^{u^2} du
\]

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The right hand side of eqn. (7.36) represents a normalised temperature so that the left hand side may be thought of as the temperature of the device in units of the critical temperature relative to ambient. The function on the left hand side is qualitatively similar to that shown in fig. (7.10). If eqn. (7.36) has a pair of real roots, the lower one represents the time to failure. The least value of $I_o$ for which a failure time exists represents the threshold current and the threshold voltage is again obtained from eqn. (7.29b).

### 7.4.2 Theory

#### 7.4.2.1 ESD Threshold Values

The analysis by Pierce et al[13] can be used as a starting point to predict the ESD threshold values. Hence, the current profile of eqn. (7.31) and the Wunsch-Bell damage formula, eqn. (7.33), are defined as:

$$f(t) = \frac{I_o}{V_j} \sqrt{\frac{T}{D}} \left[ \sqrt{\frac{t_f}{T}} + \frac{I_{o2}^2}{2^D} \sqrt{\frac{t_f}{T}} \right]$$  \hspace{1cm} (7.37)

the failure criterion i.e, eqn. (7.36), can be restated as:

$$f(t_f) = 1$$  \hspace{1cm} (7.38)

as in ref [13]. A schematic of the normalised temperature function, $f(t)$, for a typical values of $I_o$ is shown in fig. (7.13). The lower of the two times at which the super-threshold curve crosses the line $f = 1$ determines the failure time $t_f$. For the subthreshold value of $I_o$, the $f(t)$ curve does not cross the $f = 1$ line at all. The threshold case occurs when the $f(t)$ curve just touches the $f = 1$ line. Therefore, at threshold:

$$\frac{df}{dt} = 0$$  \hspace{1cm} (7.39)
Thus, there are two criteria for determining the two variables of threshold current and threshold failure time. Equation (7.38) expresses the criterion that failure must occur whereas eqn. (7.39) expresses the criterion that it must only just occur. Substituting eqn. (7.37) in eqn. (7.39) one obtains:

\[
V_j I_o \frac{d}{dt} D \left( \sqrt{\frac{t}{\tau}} \right) + \frac{I_o^2 R_D}{\sqrt{2}} \frac{d}{dt} D \left( \sqrt{\frac{2t}{\tau}} \right) = 0 \quad (7.40)
\]

and, solving for \( I_o \), one obtains for the threshold current:

\[
I_{th} = -\frac{V_j \sqrt{2}}{R_B} \cdot \frac{d}{dt} D \left( \sqrt{\frac{t_{f}}{2t_{f}}} \right) - \frac{V_j}{R_D} \cdot \frac{1-2\sqrt{\frac{t_{f}}{t}}}{1-2\sqrt{\frac{2t_{f}}{t}}} \cdot \frac{D \left( \sqrt{\frac{t_{f}}{2t_{f}}} \right)}{D \left( \sqrt{\frac{2t_{f}}{t}} \right)} \quad (7.41)
\]

Eqn. (7.41) expresses the relationship between the time of maximum temperature and the peak current. This variation is shown as the curved arrow in fig. (7.13). The solution is readily completed by substituting eqn. (7.41) back into eqn. (7.39). However, if the function \( I_{th} \), expressed by eqn. (7.41), is plotted as a function of possible failure times, \( t_f \), it is seen that \( I_{th} \) is only positive in a small time range whose end points we designate \( t_L \) and \( t_U \), fig. (7.14). This occurs in the following way. The behaviour of \( I_{th} \), as expressed by eqn. (7.41), as the possible failure time \( t \) increases from \( t = 0 \), is controlled by the behaviour of the two Dawson integral derivatives. These functions are both positive and equal at \( t = 0 \), decrease with \( t \) to a root and from then remain negative. The term in the denominator clearly is decreasing quicker and zeros first, at this point, \( t = t_L \), \( I_{th} \) must be effectively infinite to cause threshold breakdown. Increasing \( t \) further, the denominator becomes increasingly negative causing \( I_{th} \) to decrease until the numerator zeros at \( t = t_U \). After this point \( I_{th} \) becomes negative and, consequently, physically meaningless in the present context, see fig. (7.14).
Fig. (7.13) Normalised Temperature Profile for Various Values of Peak Current

Fig. (7.14) Normalised Peak Current vs Time of Maximum Temperature
Thus a window of possible failure times exists between $t_L$ and $t_U$ given by:

\[
\frac{d}{dt} D \left[ \sqrt{\frac{2t_L}{\tau}} \right] \quad \text{and} \quad \frac{d}{dt} D \left[ \sqrt{\frac{t_U}{\tau}} \right] = 0
\]

or

\[t_L = x_0^2 r/2 = 0.427r \quad (7.42a)\]

and

\[t_U = x_0^2 r = 0.854r \quad (7.42b)\]

where $x_0 = 0.92413$ is the position of the turning point of the Dawson integral i.e. $D(x_0) = 0[19]$. The window is consistent with the result of Pierce et al[1] who found a failure time of 450ns for a decay constant of $r = 790$ns, this represents a failure time of $t_r = 0.569r$.

The threshold current $I_{th}$ must satisfy eqn. (7.38) with the threshold time to failure $t_r$ restricted to the above window. The point of this analysis is that, within the window specified above, the Dawson integrals in eqn. (7.37) do not vary appreciably. Both Dawson integrals may be approximated by 0.521 to within 5% so that the threshold current is given by:

\[I_{th} V_j + I_{th}^2 \frac{R_D}{\sqrt{2}} = \frac{B/\sqrt{r}}{0.521} \quad (7.43)\]

to a very good approximation. Equation (7.43) has solution:

\[I_{th} = \frac{V_j}{\sqrt{2R_D}} \left[ \sqrt{1 + \frac{2\sqrt{2B}}{\sqrt{r}}} - 1 \right] \quad (7.44)\]

The voltage breakdown threshold may then be obtained from equation (7.29b). The threshold breakdown time is obtained by approximating the Dawson integrals in eqn. (7.37) as before and solving for $t_r$. This yields:
For the case considered by Pierce et al[13], with $R_D = 3.90 \Omega$ and $V_j = 11.1\text{V}$, equations (7.44) and (7.45) give $I_{th} = 7.17\text{A}$ and $t_f = 0.549\tau$. These results compare very favourably with his numerical calculations which gave $I_{th} = 7\text{A}$ and $t_f = 0.569\tau$.

It is interesting to note that eqn. (7.43) has the form of an "average power" method in the manner of Speakman[12]. The right hand side represents the Wunsch-Bell failure power for a square pulse of width $0.72\tau$. The left hand side is not strictly an average over any particular time range (this derives from the fact that the pulse is a double exponential). Its value lies between the peak power $P(0)$ and a related "average" power defined by:

$$P_{AV} = \frac{1}{\tau} \int_0^\infty P(t) \, dt$$

i.e. the total energy divided by the characteristic time.

### 7.4.3 Finite width junctions

If we relax the assumption that the region in which the heat is dissipated is a large two dimensional area at the junction by allowing it a small but finite thickness $c$, the Wunsch-Bell dependence is not valid throughout the entire time range ($0 < t < t_f$), as shown in section 7.4. Strictly, the Wunsch-Bell region only holds in the range:

$$t_c = \frac{c^2}{4\pi D} \leq t \leq t_b = \frac{b^2}{4\pi D}$$

where $D$ is the thermal diffusivity of the junction material and $b$ is the smaller of the two dimensions of the area of the junction dissipating power. Prior to $t_c$ an adiabatic region persists in which:
where $A = 2Bt_c^i[16]$. Beyond, $t_b$, the damage profile becomes first inverse logarithmic and then enters a steady state region as shown in section 7.2.

In general, if $b$ is sufficiently large that $t_b >> t_b$, we may assume that:

\[
0 \leq t \leq t_c \quad \frac{d}{dt} \left[ \frac{1}{P_D(t)} \right] = \frac{1}{2Bv t_c} \quad (7.47a)
\]

\[
t_c \leq t \leq t_f \quad \frac{d}{dt} \left[ \frac{1}{P_D(t)} \right] = \frac{1}{2Bv t} \quad (7.47b)
\]

for the damage threshold for square pulses. With this damage profile the Dawson Integrals in eqn. (7.35) are replaced by the more general function defined by:

\[
D(x; x_c) = \int_{x_c}^{x} e^{-x^2} \left[ e^{x^2} \right] dy + e^{-x^2} \left[ \frac{e^{x^2} - 1}{2x_c} \right] \quad (7.48)
\]

where $x = \sqrt{(t/r)}$ and $x_c = \sqrt{(t_c/r)}$. The edges of the failure window are given by:

\[
\frac{d}{dx} D \left[ \sqrt{2x_L} ; \sqrt{2x_C} \right] = 0 \quad (7.49a)
\]

and

\[
\frac{d}{dx} D(x_u; x_c) = 0 \quad (7.49b)
\]

If $c$ is relatively small, such that $t_c \leq r$, the roots of eqns. (7.49a&b) are:

\[
\sqrt{(t_1/r)} = 0.653 + 0.435\sqrt{(t_1/r)} \quad (7.50)
\]
and \[ \sqrt{\left( t_U / \tau \right)} = 0.924 + 0.405 \sqrt{\left( t_c / \tau \right)} \] (7.51)

(Eqns. (7.50) and (7.51) are accurate to 3% and 1.5% respectively). Thus, the failure window moves to larger times, and closes slightly, as \( c \) increases. Over the range \( t_L \) and \( t_U \) the generalised functions \( D(x;x_c) \) and \( D(\sqrt{2x};\sqrt{2x_c}) \) may be approximated by:

\[ \alpha = 0.521 - 0.152x_c \] (7.52a)

and

\[ \beta = 0.521 - 0.152\sqrt{2x_c} \] (7.52b)

respectively. Repeating the analysis leading up to eqns. (7.44) and (7.45) yields the modified expressions:

\[ I_o = \frac{\alpha \sqrt{\left( \frac{2 \sqrt{2} \beta}{\sqrt{r}} \right)}}{B R_D} \left[ \frac{1 + \frac{2 \sqrt{2} \beta}{\sqrt{r}}}{\frac{\alpha^2}{R_D^2}} \right] - 1 \] (7.53)

and

\[ \sqrt{\frac{t_c}{\tau}} = \frac{1}{2 \alpha} \left[ \frac{V_j + I_o}{V_j + \sqrt{2} \left( \beta / \alpha \right)} R_D \right] \] (7.54)

If the time \( t_b \) associated with the smaller of the two effective junction dimensions, \( c \), is less than the predicted failure time, \( t_f \), the Wunsch-Bell profile is no longer valid and the inverse logarithmic region is entered[16]. The derivative of the square wave damage profile required in eqn. (7.35) now becomes:
The contribution from the region beyond \( t_b \) is numerically less than a Wunsch-Bell contribution. As a consequence the numerator in eqn. (7.37) zeros later, thus the upper limit of the failure window increases and the window opens slightly.

The current pulse may be regarded as exponential to a good approximation but this is not crucial to the argument. It can easily be shown that a failure window exits for any monotonically decaying current profile with characteristic time \( \tau \) and, for most physical pulses \( I(t) \), the equivalents of the Dawson integrals will also not vary considerably over the failure window. Consequently eqns. (7.43) and (7.44) or (7.53) and (7.54) are expected to give good estimates of the threshold current and failure time. A similar approach to ESD thermal breakdown with that are reported here will be reported by Lin[18] at IRPS, 1990. His result can be shown to be identical to eqn. (7.53) for the special case of \( R_B = 0 \).

### 7.5 Experimental EOS Thermal Breakdown

#### 7.5.1 Introduction

In the previous sections, thermal models have been derived for EOS(square pulse) and ESD(electrostatic discharge) breakdown in semiconductor devices. A further experimental program has been carried out to verify the accuracy of the new EOS thermal model and compare the results with existing semiconductor thermal breakdown models.

#### 7.5.2 Adaptation of Existing Thermal Models

The Wunsch and Bell (eqn. 7.1) expression requires little adaptation for analysis of the results presented in this thesis. The cross-sectional area, \( A_p \), is defined with reference to the defect dimensions of the new thermal model as \( a \times b \), the largest area. Thus the adapted expression is:
\[ P_f = ab \sqrt{\frac{4\pi\rho C_p}{T_e - T_a}} t_f^{-3/2} \] (7.56)

In order to use the Tasca model (eqn. 7.2) for the planar structures used in our study the spherical defect region was replaced with an equivalent rectangular parallelepiped geometry of dimensions \( a, b, c \) where, \( c \leq b \leq a \). These definitions are identical to the new thermal model.

The volume and surface area coefficients in the Tasca equation are therefore be replaced by the following expressions relating to the new geometry.

\[
\begin{align*}
\text{a) } & \quad 4\pi r^3/3 = abc \\
\text{b) } & \quad 4\pi r^2 = 2ab + 2ac + 2bc
\end{align*}
\]

The final term was ignored, because the experimental study only used pulses in the microsecond region. The final modified expression is:

\[ P_f = \left[ abc \rho C_p t_f^{-1} + (2ab + 2ac + 2bc) \sqrt{\rho C_p K} t_f^{-3/2} \right] \left[ T_e - T_a \right] \] (7.57)

### 7.5.3 Apparatus

The devices were probed in the dark, on-wafer, using a manual Wentworth probe kit and were subjected to temperature stress using a heated chuck.

The devices were electrically stressed using a E-H research Labs 132-L voltage pulse generator able to deliver constant voltage pulses up to 50V with a duration of between 20ns to 100ms, and a rise time of 25ns. It was connected to the probe kit via a grounded coaxial lead.

The current and voltage pulses were captured on an HP 54111D, 1GHZ digital oscilloscope using a Tektronics CT1 Hall probe placed around the input cable, near to the device and an HP 10440A, 10M\( \Omega \), 3pF probe connected directly across the device. It is reasonable to expect that the voltage probe would not load the circuit significantly due to its high impedance.
The current and voltage (I/V) characteristics of the structures were measured using an HP4145B parametric analyser. Both the parametric analyser and oscilloscope were controlled by a Walters 286 (IBM AT compatible) microcomputer equipped with a National Instruments IEEE card.

### 7.5.4 Thermal Failure Criteria

In order to apply the thermal models to the present study, the following criteria were adopted for thermal failure:

a) The devices were subjected to a constant power pulse to within ±0.1W. The power profile was obtained by multiplication of the current and voltage waveforms measured during the pulse.

b) Evidence of thermal failure was indicated as a rapid rise in current\power at some time during the pulse. This point in the current\power waveform was taken to be the failure time, $t_f$.

c) The failure temperature was taken to be 1511 K, the melt temperature of GaAs.

d) The thermal constants were assumed to be independent of temperature in each of the thermal models, and were calculated at the failure temperature using the approximations given by Chase[9]. It should be noted, however, in reality the thermal conductivity is a function of temperature in GaAs[19]. Therefore, $C_p = 368 \text{ JK}^{-1}\text{K}^{-1}$, $K = 7.123 \text{Wm}^{-1}\text{K}^{-1}$, and $\rho = 5170 \text{Kgm}^{-3}$. The thermal diffusivity is then defined by, $D = \frac{K}{\rho C_p} = 3.744 \times 10^{-6} \text{m}^2\text{s}^{-1}$.

### 7.5.5 Experimental Procedure

The main set of experiments were carried out using the I69W wafer. All the devices were assumed to be identical. In order to eliminate possible variations across the wafer, the devices were taken from those areas of the wafer which displayed a pinch-off voltage close to the average for the whole wafer. Devices were stressed until failure occurred according to the following procedure.
a) The wafer was heated to the required experimental temperature and allowed to settle for 15 minutes.

b) The $I_{gs}$ vs $V_{gs}$ characteristics of the MESFET gate-source diode were measured.

c) A constant voltage pulse of up to $25\mu s$ duration was applied to each device and the corresponding current and voltage vs time waveforms recorded on the oscilloscope.

d) If the pulse conformed to the prescribed thermal failure criteria, the failure time, $t_f$, and power magnitude, $P_f$, were recorded.

e) If the pulse did not conform to the failure criteria it was rejected, and a new device selected.

f) The diode $I_{gs}$ vs $V_{gs}$ characteristics were again recorded.

Repeating the above procedure for different input power magnitudes, a series of results was obtained for the variation of the failure time with the input power to the device. These experiments were carried out at ambient temperatures of $25^\circ C$, $100^\circ C$ and $175^\circ C$. The experimental data is thought to be most accurate in the range $100\text{ns} < t_f < 10\mu s$ because the bandwidth of the current probe limits the accuracy at times greater than $10\mu s$, and below $100\text{ns}$ the rising portion represents a significant part of the pulse.

The E552 wafer was used in a second set of experiments using the same failure criteria, which allowed the burnout failure modes to be examined using an SEM.

7.5.6 Results

7.5.6.1 Visible Failure Modes

Two distinct visible failure modes were evident within the results from both wafers. Examples of these failure modes from the E552 wafer with the polyimide removed were photographed using an SEM. These failure modes were:

(a) A large blackened region between the gate and source contacts which normally appears at the end of the gate nearest the probing/bond pad.
These regions varied in size from $1\mu m$ - $20\mu m \times 5\mu m$ on the surface of the GaAs, as viewed through the microscope. A typical electron micrograph of this failure mode is shown in fig. (7.15). In this case a large amount of damage can be seen extending from the ohmic contact to the gate contact, with a portion of the gate being totally destroyed.

(b) Small "white" region(s) between the gate and source contacts which appear along the gate width. Normally, for a single pulse a single "white" region would occur. These regions were approximately $3\mu m \times 6\mu m$ on the surface of the GaAs. A micrograph of this failure mode is shown in fig. (7.16). It can be seen that some of the source contact may have diffused into the channel, or evaporated, leaving a small crater at the edge of the contact. Little damage to the gate contact can be seen.

7.7.6.2 Failure Waveforms

Figs. (7.17) and (7.18) show two voltage/current and power failure waveforms, each recorded for a positive polarity pulse of $2\mu s$ duration. In fig. (7.18a) the power waveform decreases slightly then gradually increases until a sharp step is evident at the failure point. In this case an average power of 1.2W was recorded. In fig. (7.18b) the power waveform decreases slowly and then begins to increase again at $\approx 0.6\mu s$ until the sharp step occurs at the failure point. In this case the average power was recorded as 0.8W.

In general, if the failure criteria were fulfilled early in the pulse, as shown in fig. (7.17a), mode (a) failure sites were observed. If the failure criteria was fulfilled towards the end of the pulse, as shown in fig. (7.17b), mode (b) failure sites were observed. This effect was purely an observation and no further study into these effects was carried out.
Fig. (7.15) SEM Micrograph of failure mode (a)

Fig. (7.16) SEM Micrograph of failure mode (b)
Fig. (7.17) Diode Voltage\current Failure Waveforms

Fig. (7.18) Diode Power Failure Waveforms
7.7.6.3 Diode Failure Characteristics

After being subjected to a pulse similar to the one in shown fig. (7.17a) the diode $I_{gs}$ vs $V_{gs}$ characteristic generally degraded showing resistive or near resistive properties. These failures tended to be characteristic of failure mode (a). An example of such a degradation is shown in fig. (7.19).

In some cases the failure criteria was fulfilled near the end of the pulse, as shown in fig. (7.17b), yet no major changes were observed in the diode $I_{gs}$ vs $V_{gs}$ characteristics. These failures were generally characteristic of failure mode (b). A closer examination of the forward bias $I_{gs}$ vs $V_{gs}$ characteristic revealed that the current plateau region had decreased in magnitude. The $I_{gs}$ vs $V_{gs}$ characteristics are shown in fig. (7.20).

7.7.6.4 Failure time vs Input Power Results

The experimental results were plotted in two formats to allow the thermal models to be compared. The first format was the normal log ($P_I$) vs log ($t_I$) plot, and the second was the $1/P_I$ vs log ($t_I$) plot. Experimental results at the three temperatures in these formats are shown in figs. (7.21) and (7.22). The results at $t_I \geq 1 \mu s$ contain a significant number of mode (b) failures, especially at the higher temperatures. This may explain the large scatter in the results. No distinction has been made between failure modes (a) and (b) because the defined failure criteria had been fulfilled in each case.
Fig. (7.20) Diode I/V plot, Characteristic of Failure Mode (b)

Fig. (7.19) Diode I/V plot, Characteristic of Failure Mode (c)
Fig. (7.21) Log (P_t) vs log (t_f) plot of Failure Data at 25°C, 75°C and 175°C

Fig. (7.22) 1/P_t vs log (t_f) plot of Failure Data at 25°C, 75°C and 175°C
7.5.7 Discussion

7.5.7.1 Visible Failure Modes

In a perfect forward biased MES diode, the current will be distributed uniformly along the gate width. If the dissipated power is sufficient to cause heating, the whole of the channel region will begin to increase in temperature. The active volume being heated would be related to the full gate width. In a real device, however, defects in the channel will cause localised high current regions, far above the average current density for the rest of the channel. Burnout, in this real device, will occur when one, or several, defect regions reach the critical temperature.

The position of the final burnout region will also depend on the field distribution in the channel. The highest field point for the devices used in this study is likely to be at the origin of the gate, near the bonding/probe pad, due to the voltage drop along the gate stripe.

The two distinct failure modes observed are likely to be related to the power dissipated subsequent to the failure criteria being fulfilled. Energy dissipated, subsequent to a portion of the device reaching the critical temperature, will contribute to the increase in size of the defect, and to the probability of metallic diffusion into the channel. If, as in many mode (b) failures, the failure criteria is fulfilled near the end of the pulse, little time remains for significant metallic diffusion. Hence, when the defect region recrystallises after the pulse, a non-conducting region appears to have been created. If the failure criteria had been fulfilled during the early part of the pulse, a large amount of heat would be dissipated within the defect during the remaining part of the pulse, and metallic diffusion is likely to occur causing a permanent low resistance path to be created.

To summarise, the observed failure geometry is unlikely to be related to the dimensions predicted by the model because of the many current paths in the channel, the final burnout site(s) being related to the defect(s) with the highest current density. Observed visual damage is likely to be related to the overall length of the pulse.
A similar situation is likely to be encountered when the diode is reverse biased, due to the localised current regions which occur when the diode enters avalanche breakdown. Further work by the authors is concentrating in this area.

### 7.5.7.2 Diode Failure Characteristics

Two distinct changes were observed in the diode $I_{gs}$ vs $V_{gs}$ characteristics after pulsing. The first, related to failure mode (a), exhibits resistive/near resistive characteristics after pulsing. In this case the pulse brings a localised region to the critical temperature causing metallic diffusion and hence this region becomes fully conducting on subsequent measurement of the diode $I_{gs}$ vs $V_{gs}$ characteristics. This can be interpreted as a fixed resistance in parallel with the normal diode. The current flowing through the device is then a superposition of the currents flowing through the diode and the parallel resistance. The second $I$-$V$ characteristic change, relating to failure mode (b), is thought to be due to a portion of the channel becoming open circuit subsequent to the application of the pulse. This failure mode only becomes evident when the forward bias current plateau region is examined in detail. The plateau region, initially due to velocity saturation in the channel, is directly dependent on the gate width ($W_g$). If, subsequent to a pulse, a portion of the channel becomes open circuit, the value of the effective gate width ($W_g$) will decrease, causing the magnitude of the saturation current to decrease.

### 7.5.8 EOS Thermal Breakdown Modelling

Using the analysis discussed in section 3.3 the experimental results will be used to predict the "defect" dimensions associated with this structure at 25°C. These dimensions will be used in all the thermal models under investigation to assess the accuracy of each model. The temperature dependence of the $P_r$ vs $t_r$ curves, using the new model, will be calculated using these dimensions and then compared with the experimental results.
7.5.8.1 Estimation of the "Defect" Dimensions

Using the data displayed in figs. (7.21) and (7.22) most of the parameters, for inclusion in expressions (1) to (7), can be extracted with reasonable accuracy. Table (7.2) gives these estimations.

**Table 7.2 - Graphical Estimation of Defect Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Lower</th>
<th>Average</th>
<th>Upper</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_a$ ($\mu$s)</td>
<td>10</td>
<td>20</td>
<td>32</td>
</tr>
<tr>
<td>$t_b$ (ns)</td>
<td>320</td>
<td>562</td>
<td>1000</td>
</tr>
<tr>
<td>$t_e$ (ns)</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$A$ (Ws)</td>
<td>0.95x10^{-6}</td>
<td>1.4x10^{-6}</td>
<td>1.8x10^{-6}</td>
</tr>
<tr>
<td>$B$ (Ws$^2$)</td>
<td>2.2x10^{-3}</td>
<td>3.16x10^{-3}</td>
<td>4.5x10^{-3}</td>
</tr>
<tr>
<td>$t_o$ (ns)</td>
<td>100</td>
<td>216</td>
<td>398</td>
</tr>
</tbody>
</table>

The average values of $t_a$ and $t_b$ have been estimated directly from the $1/P_t$ vs log ($t_t$) plot in fig. (7.23), the value of $t_e$ was unclear from the data. The values of $A$ and $B$ are calculated from the best fit $P_t \propto t_t^{-1}$ and the $P_t \propto t_t^{-1/2}$ lines in the time domain less than $t_b$ from the log ($P_t$ vs log ($t_t$) plot in fig. (7.24). The value of $\delta$ (if required) can be calculated by linear regression from $t = 0.56 \mu$m to 2.5$\mu$m and the interpolate of this line is the average value of $t_o$. The lower and upper values of the parameters have been estimated by hand, thus giving an indication of the variation in $a, b$ and $c$ at the limits of the experimental data. Using the above parameters the average values of $a, b$ and $c$ can be estimated. The value of $b$ can be calculated from expressions (2) and (5) and thus a mean can be used. The limits of $c$ have been calculated from the "worst case" combinations of $A$ and $B$, i.e lower value = $A/B$ minimised, upper value = $A/B$ maximised.

**Table 7.3 - Calculation of the Defect Dimensions**

<table>
<thead>
<tr>
<th>Expression</th>
<th>Dimension</th>
<th>Lower</th>
<th>Average</th>
<th>Upper</th>
</tr>
</thead>
<tbody>
<tr>
<td>(2)</td>
<td>$a$</td>
<td>21.6$\mu$m</td>
<td>30.68$\mu$m</td>
<td>38.8$\mu$m</td>
</tr>
<tr>
<td>(3)</td>
<td>$b$</td>
<td>4.1$\mu$m</td>
<td>5.14$\mu$m</td>
<td>6.86$\mu$m</td>
</tr>
<tr>
<td>(5)</td>
<td>$b$</td>
<td>5.9$\mu$m</td>
<td>8.68$\mu$m</td>
<td>11.7$\mu$m</td>
</tr>
<tr>
<td>(4)</td>
<td>$c$</td>
<td>0.724$\mu$m</td>
<td>1.52$\mu$m</td>
<td>2.81$\mu$m</td>
</tr>
</tbody>
</table>
Hence, the average values of the defect dimensions are taken to be:

\[ a = 30.68 \mu m, \ b = 6.91 \mu m, \ and \ c = 1.52 \mu m. \]

Expression (1) could also have been used for the estimation of the \( a \) dimension, but the value of \( t_c \) was not well defined. Expression (6) may also have been used for the prediction of \( a \), but the result obtained from this expression is likely to be in error due to the multiplication of errors from the 5 variables contained in the expression. Finally expression (7) contains the thermal conductivity, which is a sensitive function of temperature, and hence prone to error since this is not well defined in practice.

Using the predicted defect dimensions, the \( P_r \) vs \( t_r \) relationships were calculated for each model. These relationships are shown in figs. (7.25) and (7.26) and are plotted in the log (\( P_r \)) vs log (\( t_r \)), and \( 1/(P_r) \) vs log (\( t_r \)) formats. Examination of the predicted curves in figs. (7.25) and (7.26) show that the predicted defect dimensions using expressions (1) to (5) provide a good fit to the experimental data in 3 time domains. The steady state domain contains a small amount of data, the majority of which was characteristic of failure mode (b). The modified Tasca, and Wunsch models also give an adequate fit, as expected, in selected time domains. The accuracy of the new model cannot be sufficiently tested using these results because the experimental data set is not complete in the time ranges \( t_r < 100ns \) and \( t_r > 10\mu s \). It is, of course, expected that if a more complete set of data is available, with devices from a more mature technology, the predicted \( P_r \) vs \( t_r \) relationship would be better.

The defect dimensions predicted from the new thermal model can be related to the real device dimensions by considering the active layer dimensions. For a perfect device with no defects, the current density in the active layer is the same at any point. If the device is then overstressed the channel region will therefore heat up uniformly. When a number of "defect" regions are present in the channel, each defect carries a current above the average for the rest of the channel, and consequently the sum of these currents will comprise virtually the total amount of measured current within the device. These "defect" regions are effectively combined in the new thermal model to give dimensions which are
indicative of the true current carrying portion of the channel during overstress. The $a$ dimension is a measure of this effective "defect" dimension along the gate width, the $b$ dimension is a measure of the effective "defect" dimension between the gate and source contacts, and the $c$ dimension is a measure of the effective "defect" dimension into the substrate. Fig. (7.27) shows a schematic view of how these dimensions relate to the real device dimensions. The predicted value of $a$ indicates that over $1/5$th of the channel can be considered to be carrying current along the gate width. If the device were perfect, the current would be evenly distributed, and hence this dimension would tend to the limit of the gate width, in this case, 150$\mu$m. In reality, the damaged region was only a few microns in width, indicating that a small portion of the channel had reached the critical temperature, but a significant portion of the channel had carried the current during the breakdown event.

The predicted $b$ dimension must be linked to the portion of the device in that dimension where the majority of the current is present. Part of this dimension maybe linked to the transfer length, $L_t$, which is a measure of the true current carrying portion of the ohmic contact. Using the test patterns, present on the 169W wafer, the transfer length was measured to be 2.14$\mu$m using the standard method[20]. The "defect" dimension in this direction can be therefore be considered to be composed of three real device dimensions. These are :-

i) The gate length, $L_g \approx 1\mu$m
ii) The gate-source distance, $L_{gs} \approx 1\mu$m
iii) The transfer length, $L_t \approx 2.14\mu$m.

The summation of these dimensions gives a value of $\approx 4.14\mu$m for the true current carrying portion of the device in the gate-source direction. The predicted value of this dimension was 6.91$\mu$m.
Fig. (7.23) Extraction of Model Parameters from the log ($P_f$) vs log ($t_f$) plot

Fig. (7.24) Extraction of Model Parameters from the $1/(P_f)$ vs log ($t_f$) plot
Fig. (7.25) Predicted log ($P_f$) vs log ($t_f$) relationship at 25°C

![Graph of log Input Power (W) vs Log Failure Time (s) for I96W MES Diodes]

Fig. (7.26) Predicted $1/P_f$ vs log ($t_f$) relationship at 25°C

![Graph of $1/\text{Input Power (W)}$ vs Log Failure Time (s) for I96W MES Diodes]

- 25°C Results
- New Thermal Model
- Tasca Model
- Wunsch & Bell Model

- $a = 30.68\mu m$
- $b = 6.91\mu m$
- $c = 1.52\mu m$
The c dimension predicted by the analytic expressions is probably the least accurate because of the lack of data at \( t_r < 100 \text{ns} \). It is estimated that this value could be in error by as much as one decade. The expected value for this dimension is close to the n-type layer depth, 0.16\( \mu \text{m} \). The predicted value of this dimension was in fact 1.52\( \mu \text{m} \), which therefore means that heating is taking place within the semi-insulating substrate, or the dimension is in error. An analysis of the effects on the \( P_t \) vs \( t_r \) relationship by changing the c dimension to the same order as the n-type layer indicate that the curves will show little change in the time domain at \( t_r > 100 \text{ns} \). It should be noted, however, that Buot[21] discussed the possibility of subsurface burnout in GaAs FETs initiated deep within the substrate. This may explain the abnormally large value of the c dimension predicted from the results.

7.5.8.2 Temperature Effects

Using the predicted defect dimensions at 25\(^\circ\text{C}\) the changes in the \( P_t \) vs \( t_r \) relationship for an increase in ambient temperature can be predicted. These changes in the predicted relationship for the new thermal model are shown in fig. (7.28) at 25\(^\circ\text{C}\), 100\(^\circ\text{C}\), and 175\(^\circ\text{C}\), plotted in the log \( P_t \) vs log \( t_r \) format. The predicted results show a downward shift in the 25\(^\circ\text{C}\), \( P_t \) vs \( t_r \) curve as temperature increases. The magnitude of this shift is very small in the temperature range measured. The experimental results also show a downward shift in the \( P_t \) vs \( t_r \) curve but the magnitude of this shift is much greater than predicted. The difference between the experimental and theoretical results at the higher temperatures may be attributed to a smaller defect size, implying temperature enhanced current channelling, or the failure temperature being in fact lower than the assumed melt temperature.

The use of the melt point of GaAs as the critical temperature can only be regarded as a starting point in a thermal breakdown analysis such as has been presented in this thesis. The rapid rise in current which defines the failure point maybe linked to a lower temperature as suggested by Wemple[22].
Fig. (7.27) Defect Structure within a Planar MES Diode

- Lgs = Gate/Source Distance
- Lg = Gate length
- Wg = Gate Width
- a = Defect dimension "a"
- b = Defect dimension "b"
- c = Defect dimension "c"
- d = n-type layer depth
- Lt = Transfer Length

Fig. (7.28) Predicted log (P_f) vs log (t_f) Relationship at 25°C, 75°C and 175°C
7.6 ESD Threshold Analysis

7.6.1 Introduction

In section 7.5, the \( P_f \) vs \( t_f \) relationship for GaAs MES diodes subject to a positive polarity EOS pulses was investigated. These results can be used in conjunction with the ESD thermal breakdown model, derived in section 7.4, to predict the time at which a "defect" region will attain some critical breakdown temperature during an exponentially decaying ESD pulse. In order to apply the ESD thermal breakdown model the following criteria must be fulfilled:

(a) The current profile must monotonically decay with characteristic time \( \tau \) during the breakdown period.

(b) The voltage across a junction region must be pinned at voltage \( V_j \) during the breakdown period.

(c) The bulk resistance \( R_D \) must remain constant during the breakdown period.

In principle, both positive and negative polarity pulses can be analysed using the model presented in section 7.4, but since the forward bias EOS failure data has been obtained in section 7.5, the model shall be used to predict the ESD threshold for positive polarity ESD pulses.

7.6.2 Experimental Assessment of ESD Failure

In order to determine the values of \( I_o \), \( t_f \) and \( V_c \) for devices on the I69W wafer, 40 devices were pulsed at ESD voltages of +1000V, +1250V and +1500V. The voltage and current waveforms were analysed to determine the values of the \( I_o \), \( t_f \) and \( V_c \).

It has been previously shown that failure under positive polarity stress is indicated by a premature collapse in the device voltage at some point during the
Fig. (7.29) ESD Voltage Failure Waveforms

![Graph showing ESD Voltage Failure Waveforms for I69W MES Diodes with +1250V ESD Pulse.]

Fig. (7.30) ESD Current Failure Waveforms

![Graph showing ESD Current Failure Waveforms for I69W MES Diodes with +1250V ESD Pulse.]

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pulse. This point in the voltage waveform shall be taken as the time to failure \( t_f \). The peak current \( I_0 \) can be directly measured from the current waveform.

At +1000V no devices failed. At +1250V, 9 out of 20 devices failed, 6 having a recovery in the voltage later in the pulse, showing visible "white" type failures and 3 having no recovery, showing visible "black" type failures (see section 7.5.7.1). In all cases the peak current was measured to be between 0.75A and 0.85A but the majority had a peak current between 0.82A and 0.85A. Figs. (7.29) and (7.30) show the voltage and current failure waveforms. The devices which did not show a recovery in the voltage tended to fail up to 200ns into the pulse, whilst the devices which did show a recovery failed between 270ns and 430ns. At +1500V, 100% of the devices failed in less than 100ns indicating a superthreshold pulse had been applied to the device.

### 7.6.3 ESD Threshold Prediction

In order to obtain the parameters which allow the ESD threshold voltage to be predicted, an approach similar to that suggested by Pierce[15] has been adopted. This involves the mathematical analysis of real failure waveforms to obtain many of the parameters required in eqns. (7.53) and (7.54). These parameters are:

i) The characteristic decay time \( \tau \) of the current waveform. This is normally calculated from the normal "human body" capacitance x resistance.

ii) The Wunsch and Bell damage coefficient \( B \), the defect dimension \( c \) and characteristic time \( t_e \), all of which can be calculated from the square pulse failure data.

iii) The thermal diffusivity at the melt temperature of GaAs, \( K/\rho C_p = 3.744 \times 10^{-6} \text{m}^2\text{s}^{-1} \).

iv) The junction voltage, \( V_j \).

v) The device bulk resistance, \( R_D \).

It has been established in chapters 5 and 6 that the presence of the transmission line between the AutoZap and the device, effects the profile of the
Fig. (7.31) Normalised Current Profiles

Fig. (7.32) Reconstructed $I_{gs}$ vs $V_{gs}$ Characteristics
device voltage and current waveform. This effect is normally manifested by a decrease in peak current and an increase in decay time constant. At low values of device resistance, as would be the case when a device is undergoing thermal breakdown, the peak current is much closer to the expected value. The time constant, however, remains prematurely high. In order to eliminate this error from this analysis the time constant shall be replaced with a normalised value calculated from the experimental current profiles. This is achieved by plotting the log \((I/I_o)\) against time for a number of subthreshold\threshold waveforms over the breakdown period \((0 < t_f < 500\text{ns})\). The line of best fit is obtained by linear regression and the inverse gradient is the average characteristic decay time. The results of this analysis are shown in fig. (7.31). This shows that the characteristic decay time \(\tau\) is not dependant on the ESD charge voltage and has a value of \(\approx 260\text{ns}\). This is greater than value predicted by multiplication of \(C_B\) and \((R_B + R_D)\) which yields a characteristic decay time of \(\approx 150\text{ns}\).

The Wunsch & Bell damage coefficient, \(B\), the defect dimension \(c\) and the characteristic time \(t_e\) calculated in section 7.7 for the devices on the I69W wafer are \(3.16 \times 10^{-3} \text{Ws}^{1/2}\), \(1.52 \mu\text{m}\) respectively and from eqn. (7.12) the characteristic time \(t_e\) is 49ns.

It is difficult to measure the values of \(R_D\) and \(V_j\) directly because they are both internal to the device. The experimental system can only measure the voltage across the whole of the device \(V(t)\) during the pulse and so the contribution of \(R_D\) and \(V_j\) must be estimated from eqns. (7.57) and (7.58) below:

\[
V(t) = I(t)R_D + V_j
\]  
(7.57)

or

\[
V(t) = I_0R_D\exp(-t/\tau) + V_j
\]  
(7.58)

If the MES device were acting as an "effective resistance" \(R_D\) throughout the pulse, i.e \(V_j = 0\) in eqn. (7.58), the voltage waveforms would decay in an exponential form directly related to the value of \(R_D\). Examination of the results in figs. (7.29) and (7.30) show that the voltage across the device rises rapidly to its peak value at \(\approx 14\text{V}\) and subsequently decays to near \(+5\text{V}\). The voltage then remains at this value up to a \(1\mu\text{s}\) if breakdown does not occur. Clearly the device cannot be considered simply as a "effective resistance", but must include an
"effective junction voltage" $V_J = +5V$ in order to allow the voltage plateau region to be modelled correctly. By rearranging eqn. (7.57) such that:

$$R_D = \frac{(V(t) - V_J)}{I(t)}$$  \hspace{1cm} (7.59)

the value of $R_D$ can be estimated by the line of best fit to the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics over the decay portion of a pulse. This technique is demonstrated in fig. (7.32). The average value of the "effective bulk resistance" calculated from five waveforms is 5Ω.

Substituting the parameters $\tau$, $B$, $t_c$, $c$, $D$, and $R_D$ into equations (7.53) and (7.54) the threshold peak current $I_o$, time to failure $t_f$ and the ESD charge voltage $V_c$ can be predicted. In order to give a fuller picture of the effects of $R_D$ and $V_J$, the predicted values of peak current and failure time are plotted in figs. (7.33) and (7.34) against junction voltage $V_J$ (from 0 to 15V) for a range of values for the effective bulk resistance $R_D$ (5Ω to 30Ω). Using the values of $R_D = 5Ω$ and $V_J = 5V$ the model predicts a minimum threshold value of 1.4A, a ESD charge voltage of +2107V and a failure time of 220ns. The experimental results, however, show failures can result from a +1250V pulse at 0.85A up to 460ns into the pulse. The peak current for the failures at 1250V is very well defined at 0.83A. It can be seen from fig. (7.33) that several combinations of $R_D$ and $V_J$ exist which predict this value of peak current. These combinations are $R_D = 30Ω$ @ $V_J = 0V$, $R_D = 25Ω$ @ $V_J = 2.5V$, $R_D = 20Ω$ @ $V_J = 5V$, $R_D = 15Ω$ @ $V_J = 8V$, $R_D = 10Ω$ @ $V_J = 11V$ and $R_D = 5Ω$ @ $V_J = 13.5V$. However, the majority of these combinations are unrealistic because the device voltage predicted by eqn. (7.57) bears little resemblance to the real experimental waveforms. The combination which best predict the experimental voltage waveform(s) is $R_D = 5Ω$ and $V_J = 5V$, as expected, but the peak current is far higher than observed in practice. If the current waveform is used as the controlling factor, the combination which best predicts the experimental current waveform is $R_D = 20Ω$ and $V_J = 5V$, but the predicted voltage waveform is far higher than observed in practice. The predicted and experimental voltage waveforms are shown in fig. (7.35).

The model can also be used to predict the ESD charge voltage and peak current threshold relationship as a function of the AutoZap capacitance. Using
Fig. (7.33) Predicted Peak Current vs $R_D$ and $V_j$

![Graph showing predicted peak current vs junction voltage for different $R_B$ values.]

Fig. (7.34) Predicted Failure Time vs $R_D$ and $V_j$

![Graph showing predicted failure time vs junction voltage for different $R_B$ values.]
Fig. (7.35) Experimental and Predicted Device Voltage Waveforms

Fig. (7.36) Voltage Threshold Variation vs AutoZap Capacitance
the values of \( R_D = 5\Omega \) and \( V_j = 5\text{V} \) the predicted relationship between the ESD threshold voltage and the AutoZap capacitance is shown in fig. (7.36). Also shown are the experimental results for 169W MES devices from the earlier study. The experimental values have been normalised by the addition of the effective capacitance of the transmission line. This additional capacitance \( \Delta C_l \) is calculated from eqn. (7.60) below:

\[
\Delta C_l = \tau/(R_B + R_D) - C_B
\]

Substitution of \( \tau = 260\text{ns} \), \( R_D = 5\Omega \), \( R_B = 1500\Omega \) and \( C_B = 100\text{pF} \) in eqn. (7.60) predicts \( \Delta C_l \) to be 73pF. The model predicts a higher threshold voltage than observed in practice, as expected, but the relationship of the threshold voltage as a function of capacitance matches the experimental results very well at the higher values of capacitance.

### 7.6.4 Discussion

Using the optimised parameters extracted from experimental data the model predicts that failure should occur at 2107V, 1.4A and 220ns into an ESD pulse. These values differ significantly from those observed experimentally where failures have been found to occur at 1250V, 0.83A and 460ns into the pulse.

The model predicts that a window of failure times exists such that any device subject to a threshold pulse will fail within this window. Examination of eqns. (7.50) and (7.51) show that the two parameters which control the boundary limits of the failure window are dependant only on \( \tau \) and \( t_c \). Substitution of the values of \( \tau = 260\text{ns} \) and \( t_c = 49\text{ns} \) into eqn. (7.51) gives an upper limit of time equal to 314ns. This value is 146ns lower than observed in practice. Hence either \( \tau \) or \( t_c \) must be in error. The value of \( \tau \) has been experimentally determined and this has therefore taken into account the additional capacitance of the transmission line. The value of \( t_c \) has been determined from the defect dimension \( c \) calculated from the EOS model equations. The value of \( c \) is obtained from the EOS burnout data at times in the low nanosecond region. The number of data points within this region was very low (see fig. (7.21-2)), due to the limitations of
the experimental system. Hence the estimated value of $c$ can only be regarded as "ball park" figure. It was initially surmised that the value of $c$ may be a decade smaller and close to the n-type layer depth of 0.16$\mu$m. However, in order to increase the upper limit of the failure window to 460ns the value of $c$ must increase to 3.5$\mu$m. Substituting this value into the model, the failure time increases to 340ns. This far closer to the experimental values, but the predicted peak current at $R_B = 5\Omega$ and $V_i = 5V$ increases to 1.6A, which is double that observed in practice and is therefore unrealistic. Further permutations of $R_B$ and $V_i$ can allow the predicted peak current to decrease to near that observed in practice, but the predicted device voltage bears little resemblance to experimental results.

The only other parameter which maybe in error is the Wunsch & Bell damage coefficient $B$. This was determined from the best fit line to the experimental $P_t$ vs $t_f$ data (see fig. (7.24)). The magnitude of the power was determined from the multiplication of the voltage and current waveforms during constant voltage overstress. As has been established in chapter 6, the device under positive polarity ESD overstress enters a region of negative differential resistance and the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics show a near classical current-controlled NDR response. During current-controlled NDR, current filaments will form between the contacts[23]. However, under voltage-controlled overstress the device will again enter an NDR region, but the physics behind this mode of operation is different from those controlling current-controlled NDR. In this case regions of high electric field will form and travel through the crystal[23]. It is therefore likely that any associated Joule heating of the surrounding crystal will depend on the mode of operation. Thus, the Wunsch & Bell damage coefficient obtained with results from constant voltage overstress is likely to be different to that obtained under constant current overstress. If the Wunsch & Bell damage coefficient decreases to around $1.17 \times 10^{-3}$, the value of $c$ replaced with 3.5$\mu$m (to increase the limit of the failure window), $\tau = 260$ns, $R_B = 5\Omega$, and $V_i = 5V$ the model predicts that failure will occur at 0.835A, 1252V and 410ns into the pulse. These predictions are much closer to those observed in the experimental results.

The predicted ESD threshold voltage as a function of AutoZap capacitance are much higher than those observed experimentally. This is to be
expected for the reasons described above. However, a further error will be introduced because of the difference in the failure criteria. A device will fulfill the AutoZap failure criterion when a 20μA change in the $I_{gs}$ vs $V_{gs}$ characteristics is been recorded subsequent to the previous pulse. This can be compared to the $I_{gs}$ change normally observed under single pulse thermal EOS/ESD failure, which could be in the order of milliamperes. It has also been established in chapter 6 that the device voltage will increase as the AutoZap capacitance is increased, at a fixed ESD charge voltage. As a result, at the lower values of AutoZap capacitance a greater ESD charge voltage would be required to induce failure than would be expected. Hence the threshold voltage at $C_B = 125\text{pF}$ and $175\text{pF}$ in fig. (7.36) will be slightly high. At the higher values of capacitance the predicted trend matches the experimental results very well.

### 7.7 Conclusions

Previous attempts to model the conditions leading up to thermal breakdown have been based on the thermodynamics of simple "defect" geometry's which bear little relation to the geometry of the devices under investigation (planes, spheres and cylinders, etc). The EOS model presented in this chapter represents a major step forward in thermal modelling of semiconductor devices. The model allows the "defect" to take on three independent dimensions which have been shown to correlate better with the expected "defect" dimensions under thermal breakdown in GaAs MES diodes. These in turn can be related to real device dimensions. The model predicts relationships similar to all the previous thermal models when the "defect" dimensions are set to those appropriate for each model. This has not been possible with the previous models which had limited accuracy outside their optimum conditions.

An extension to the above model allows the ESD threshold voltage to be predicted to induce thermal breakdown in semiconductor devices. This model predicts that thermal failure can only occur within a specific time "window" during ESD pulse. The boundaries of this time window are linked to the CR decay constant of the ESD pulse and the smallest defect dimension. The model
predicts a prematurely high peak current and low failure time for GaAs MES diodes under forward bias ESD stress. The low predicted failure time is attributed to the errors in the smallest defect dimension which requires accurate EOS $P_f$ vs $t_f$ data in the time range $<100\text{ns}$ which was not possible with the present experimental set-up. The high predicted value of the peak current may be linked to an error in the Wunsch & Bell damage coefficient.

### 7.8 Summary

A new three dimensional thermal breakdown model has been derived which predicts the full $P_f$ vs $t_f$ relationship for all semiconductor devices. This model has been used to assess forward bias thermal breakdown in GaAs MES diodes. The results indicate that the new model is more versatile than previous models for the prediction of the thermal breakdown conditions in GaAs MES devices.

A further model for thermal breakdown in semiconductor devices under ESD stress has also been derived. This predicts that threshold failure can only occur within a specific time "window" during an ESD pulse. The ESD thermal model has been used to determine the threshold conditions under which an positive polarity ESD pulse will induce thermal failure in GaAs MES diodes.

### 7.9 References


There are many papers on this subject, several of which can be found in the EOS/ESD Symposia Proceedings 1979-1988.


CHAPTER 8

COMPUTER CIRCUIT MODELLING

8.1 Introduction

It is the purpose of this chapter to develop circuit models of the experimental system and an MESFET\MES device to study, using computer circuit modelling techniques, some of effects noted during the ESD experimental study in chapter 5. This study will allow the parasitic effects of the experimental system on the device waveforms to be quantified and lead to a greater understanding of how the experimental system can effect "real world" measurements. This information is vital to allow the comparison of the EOS and ESD failure results reported in this thesis with other studies reported on this subject. Specifically, the following areas will be investigated.

a) The variation of the output characteristics of the EOS pulse generation system with purely resistive loads.
b) The degradation of the MESFET $I_{ds}$ vs $V_{ds}$ characteristics subsequent to an ESD pulse.
c) The variation of the output characteristics of the ESD pulse generation system to purely resistive loads.
c) The MES diode voltage and current waveforms present during a sub-threshold ESD event.

Circuit models will be derived for the ESD pulsing system, the MESFET and the MES diode and these models will be used to address the areas outlined above. The predicted curves from a PSPICE circuit analysis can then be directly compared to the experimental results obtained in chapter 5.
8.2 The PSPICE Modelling Package

The PSPICE modelling package is a set of software algorithms designed to predict, by iteration, the current and voltage values present at a set of nodes in a user defined circuit. The user can define such a circuit from the normal circuit diagram of the electronic system under analysis.

Certain circuit elements have their own models within the software package. The models include parameters such as temperature, activation energy, leakage current, threshold voltage, and series resistance, etc which may be varied by the user in accordance with the conditions under which the device is operating.

8.2.1 Resident MESFET Model

The PSPICE modelling package has a GaAs MESFET in its library of devices. This model has been derived from semi-empirical equations[1,2] which can predict typical FET $I_{ds}$ vs $V_{ds}$ characteristics. The library model is "ideal" in the sense that it does not predict breakdown, because there are no model parameters which allow this stage of electrical activity to be included. It is proposed that the MESFET model be used in conjunction with other circuit elements to allow the correct current/voltage MES diode characteristic, including breakdown, to be modelled.

8.2.2 Input File Structure

In order to derive a circuit for analysis using the PSPICE modelling package, an input file must be created using a standard DOS text editor. Each circuit element is connected to other elements at a point called a node. Each node is assigned with a number and each element must be connected to the correct number of nodes, e.g. a resistor must be connected at 2 nodes. Each element is sequentially placed on a separate line in the input file. Other parameters, which will be described in section 8.3, can also be added where necessary.
8.2.3 Circuit Elements

8.2.3.1 Passive Elements

The passive resistive[3], capacitive[4] and inductive[5] circuit elements used throughout the analysis are assumed ideal. They have the form, either:

a) R(name) (node a) (node b) (value)
b) C(name) (node a) (node b) (value)
c) L(name) (node a) (node b) (value)

8.2.3.2 Diodes

The diodes are modelled as an ideal diode in series with a resistance $R_s$. The (+) node is the anode and the (-) node is the cathode. Conventional current flows from the anode to the cathode. Both the statements below are required if the model parameters are to be changes from the default values. The main model parameters[6] are also shown.

D(name) (node a) (node b) (model name)
.Model (model name) D (Model parameters)

Model Parameters

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_s$</td>
<td>Reverse saturation current</td>
<td>$10^{-6}$A</td>
</tr>
<tr>
<td>$N$</td>
<td>Emission coeff.</td>
<td>1</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Series resistance</td>
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</tr>
<tr>
<td>CTO</td>
<td>Zero bias p-n capacitance</td>
<td>1pF</td>
</tr>
<tr>
<td>$V_J$</td>
<td>p-n potential</td>
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<tr>
<td>$TT$</td>
<td>Transit time</td>
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</tr>
<tr>
<td>$BV$</td>
<td>Reverse bias breakdown voltage</td>
<td>5V to 50V</td>
</tr>
<tr>
<td>$IBV$</td>
<td>Reverse breakdown current</td>
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<td>$EG$</td>
<td>Bandgap voltage</td>
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</tr>
<tr>
<td>XTI</td>
<td>$I_s$ temperature coeff.</td>
<td>3</td>
</tr>
</tbody>
</table>
8.2.3.3 MESFETs

The GaAs MESFET circuit element present in the library of devices can be used in any circuit which requires nominal currents and voltages within the device or external circuitry. If the device is stressed to such a limit that the electrical patterns of current and voltage differ from the normal characteristics, additional circuit elements will be required. As with the diode element, both statements are required if the model parameters are changed from the default values. The MESFET model parameters[7] are set to model the typical electrical characteristics of a MESFET on the E552 wafer. Fig. (8.1) shows the equivalent circuit for this device.

\[
\text{B(name) (drain) (gate) (source) (model name)}
\]

\[
\text{.MODEL (model name) GASFET (model parameters)}
\]

Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTO</td>
<td>Threshold voltage</td>
<td>-1.25V</td>
</tr>
<tr>
<td>ALPHA</td>
<td>Tanh constant(V⁻¹)</td>
<td>2</td>
</tr>
<tr>
<td>BETA</td>
<td>Transconductance coeff(A/V²)</td>
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</tr>
<tr>
<td>LAMBDA</td>
<td>Channel length modulation(V⁻¹)</td>
<td>0.001</td>
</tr>
<tr>
<td>(R_g)</td>
<td>Gate ohmic resistance</td>
<td>0Ω</td>
</tr>
<tr>
<td>(R_d)</td>
<td>Drain ohmic resistance</td>
<td>15Ω</td>
</tr>
<tr>
<td>(R_s)</td>
<td>Source ohmic resistance</td>
<td>15Ω</td>
</tr>
<tr>
<td>IS</td>
<td>Gate p-n saturation current</td>
<td>1µA</td>
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<td>VBI</td>
<td>Gate p-n potential</td>
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<td>Gate/source capacitance(no bias)</td>
<td>2pF</td>
</tr>
<tr>
<td>CDS</td>
<td>Gate/drain capacitance(no bias)</td>
<td>2pF</td>
</tr>
</tbody>
</table>
8.2.3.4 Voltage sources and Current Measurement Elements

In order to measure the current in any branch of the circuit model, DC voltage sources with the voltage set to zero, are used as ammeters. This is the convention used by PSPICE. The model parameters are set as follows[8].

\[ V(\text{name}) \ (\text{node a}) \ (\text{node b}) \ 0 \]

8.2.3.5 Transmission Lines

The inclusion of transmission lines within the system model has allowed the coaxial cables carrying the ESD pulse from the AutoZap to the probe tips to be correctly modelled. The transmission line is a bidirectional, ideal delay line. It has 4 nodes a,b,c and d. The (+) and (-) nodes define the polarity of a positive voltage at a,b and c,d. The model parameters[9] are derived as follows:-

\[ T(\text{name}) \ (+\text{node a}) \ (-\text{node b}) \ (+\text{node c}) \ (-\text{node d}) \ + \ Model \ Parameters. \]
### Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZO</td>
<td>Characteristic impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>F</td>
<td>Operational frequency</td>
<td>-</td>
</tr>
<tr>
<td>TD</td>
<td>Time delay through the line</td>
<td>Z₀*C₁</td>
</tr>
<tr>
<td>NL</td>
<td>Relative wavelength</td>
<td>-</td>
</tr>
</tbody>
</table>

The line will operate with any one of the last three model parameters. The characteristic impedance of the line is set to 50Ω and the capacitance, C₁, of the transmission line is measured using an LCR bridge.

### 8.3 Circuit Operational Commands

This section describes the commands within a circuit definition program, which allow the circuit to be exposed to various stimuli, and also the commands which allow the circuit response to be displayed. The commands relevant to this study are:-

1. `.DC (voltage source) (start V) (end V) (inc. V)`

   The `.DC` command allows the voltage from the defined voltage source to sweep from the start value to the end value in predefined defined increments[10].

2. `.TRAN (start time) (end time) (inc. time)`

   The `.TRAN` command allows a transient analysis of the circuit to be performed[11]. Any component can be set to have initial conditions which are released at t = 0.

3. `.MODEL (model parameters)`

   This statement allows the default values of the model parameters to be changed to suit the user[12]. Thus, different types of the same device may be defined and included in the circuit.
4. **.TEMP (value)**

The .TEMP statement allows the user to change the ambient temperature in which the circuit is operating[13]. This is included because some model parameters are temperature sensitive and hence their characteristics will change when this command is interpreted.

5. **.OPTIONS (option parameters)**

The .OPTIONS statement allows several features of the technique used by PSPICE to solve the circuit equations to be modified[14]. It also can be used to change the data format. Some examples of these options are listed below:

a) ABSTOL - Best accuracy of currents 1\mu A
b) VNTOL - Best accuracy of voltages 1\mu V
c) LIMPTS - Max. no. of points in print table 201

6. **V(x) V(y).....(initial node voltages)**

This statement is used to set the voltage at any nodes before the transient routine is started at t=0.

7. **.PROBE**

The .PROBE statement loads in the display algorithm and displays the data stored in the output file as a graph[15].

8. **.END**

The .END statement indicates completion of the circuit under analysis[16].
8.4 EOS characterisation circuit

A circuit model has been derived to predict an EOS pulse generator voltage output variation with changes in the load resistance. This circuit assumes the pulse generator has a 50Ω resistance in series with the output terminals. The measurement probes, and transmission line are included for completeness. The PSPICE programme has been used to predict the change in load voltage for a range of resistive loads from 5Ω to 500Ω and for a range of pulse generator output voltages from 4V to 40V. Comparison of the PSPICE results of fig. (8.2) with the experimental results of fig. (8.3) shows the curves to be identical to within a small experimental error, proving the EOS circuit model is essentially correct. The important feature of these results is that the EOS pulse generator output voltage at the terminals decreases as a device "effective" resistance decreases. This explains why, in section 7.7.6.2, the measured voltage decreases when a device begins to burnout. The effective resistance decreases dramatically during the formation of a melt channel.

8.5 MESFET ESD Degradation Analysis

The GaAs MESFET model can be used to predict the DC $I_{ds}$ vs $V_{ds}$ characteristics. This circuit model was used in conjunction with voltage sources on the gate and drain of the device. The model parameters Alpha, Beta and Lambda were varied to model typical MESFET $I_{ds}$ vs $V_{gs}$ characteristics similar to those measured in section 5.3.1 for the E552 wafer. All other parameters were set at nominal values for the experimental devices.
Fig. (8.2)  PSPICE EOS Voltage vs Load Prediction

Fig. (8.3)  Voltage Variation as a Function of Load Resistance
The model parameters for the analysis are:

<table>
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</tr>
<tr>
<td>( R_g )</td>
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</tr>
<tr>
<td>( R_d )</td>
<td>Drain ohmic resistance</td>
<td>15 ( \Omega )</td>
</tr>
<tr>
<td>( R_s )</td>
<td>Source ohmic resistance</td>
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<tr>
<td>IS</td>
<td>Gate p-n saturation current</td>
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<tr>
<td>VBI</td>
<td>Gate p-n potential</td>
<td>-0.7V</td>
</tr>
<tr>
<td>CGS</td>
<td>Gate/source capacitance (no bias)</td>
<td>2 ( pF )</td>
</tr>
<tr>
<td>CDS</td>
<td>Gate/drain capacitance (no bias)</td>
<td>2 ( pF )</td>
</tr>
</tbody>
</table>

The PSpice circuit definition program is shown below:

```plaintext
*GASFET DC Characteristic Circuit Model
*A.J. Franklin - 1989

Vd 4 0 0.0
Vg 1 0 0.0
Rg 1 2 1000
BI 5 3 0 GAS
vmd 4 5 0.0
vmg 3 2 0.0

.DC Vd 0 4 0.2 Vg 0 -1 -0.1

.MODEL GAS GASFET (VBI=0.7 RS=15 RD=15 IS=1E-6 CGD=2pF CGS=2pF VTO=-1.25 LAMBDA=0.001 ALPHA=2 BETA=0.00825)

.OPTIONS LIMPTS=5000

.TEMP 25

.PROBE

.END
```

The predicted MESFET \( I_{ds} \) vs \( V_{ds} \) characteristics, as a function of the gate voltage, from 0 to -1V are shown in fig. (8.4). The predicted curves are similar to those in fig. (5.3). The saturated drain current at zero gate bias has been fixed at 10mA and the device has a pinch-off voltage of -1.25V.
8.5.1 Assessment of Degradation Categories

In chapter 6, several possible explanations for the changes in the $I_{ds}$ vs $V_{ds}$ characteristics after the application of an ESD pulse were offered. Category (2) degradation was postulated to be due to one, or more, of:

(a) Increase in the source or drain resistances, $R_s$ and $R_d$.
(b) Increase in the built-in potential of the gate diode.
(c) A reduction in the channel doping level.

or

(d) Changes in the surface trap density.

The increase in source or drain resistance (a) can be modelled within the software because both of these parameters are contained within the MESFET model. Fig. (8.5) shows the predicted curves when the model parameters $R_s$ and $R_d$ are increased to 200. The resulting curves show reductions in the saturated
drain current and transconductance, and an increase in the channel resistance. The effects of decreasing the source and drain resistances to 10\( \Omega \) are shown in fig. (8.6). In this case, the curves show an increase in the saturated drain current and the transconductance, and a corresponding decrease in the channel resistance. The second effect, increasing the Schottky built-in voltage (b), can be achieved by changing the model parameter \( V_{bi} \). Unfortunately this parameter is only used for the calculation of the gate-source/drain capacitance values and is not directly used to calculate the channel conduction properties and hence no change in the MESFET characteristics occurs when this value is varied.

The final two effects (c) and (d) do not have parameters within the MESFET model and hence the effects of varying these parameters could not be tested directly using PSPICE.

Category (4) and (5) degradation curves are likely to be related to the creation of gate-source (category 4) or gate-drain (category 5) leakage paths subsequent to an ESD pulse. These effects can be modelled by the inclusion of parallel resistances between nodes 3,0 (gate-source) and 3,5 (gate-drain). The current limiting feature of the curve tracers can also be approximated by the inclusion of a 1k\( \Omega \) resistor in series with the gate, thus allowing a maximum of 1mA to flow through the gate at the maximum applied gate voltage of -1V. The HP parametric analyser actually had a current limiting circuit, which only limited the current when the compliance of 1mA had been reached. However, the approximation shows the essential features of the changes in the \( I_{ds} \) vs \( V_{ds} \) characteristics. The values of the parallel resistances were set at 500\( \Omega \) to show the main features of these effects. The predicted curves are shown in figs. (8.7) and (8.8). These results can be compared to the curves shown in figs. (5.18) and (5.19). The saturated drain current remains constant for a parallel resistance path between the gate and source, while the transconductance has degraded severely. This feature is not present in fig. (5.18) because the HP parametric analyser does not limit the current until the 1mA compliance limit had been reached. The addition of the parallel resistance path between the gate and drain causes the characteristics to become virtually linear at voltages < 1V, and to saturate at voltages > +2V. The current is far greater than the superposition of the (channel current + the gate current) and hence the voltage at the gate must be going positive, forward biasing the gate-source junction.
Fig. (8.5) Category (2) MESFET Degradation Characteristics

Fig. (8.6) Category (3) MESFET Degradation Characteristics
Fig. (8.7) Category (4) MESFET Degradation Characteristics

Fig. (8.8) Category (5) MESFET Degradation Characteristics

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The current may then flow through the source region and into the drain via the parallel resistance. This effect can be verified using PSPICE by monitoring the voltage at the gate (node 3) as a function of drain and gate bias relative to ground. The results are shown in fig. (8.9). Clearly the gate is becoming forward biased as the drain voltage is increasing, hence allowing the current to be limited by the source resistance alone.

8.6 ESD Measurement Analysis

In order to predict the currents and voltages within the ESD system a model must be derived for the AutoZap pulse generator, and the additional circuit elements which model the effects of the voltage and current probes in a real experimental system. Additional transmission line circuit elements are required to model the effects of the pulse transmission medium.
8.6.1 AutoZap Model

The AutoZap circuit model adopted for this analysis is based on the standard MIL STD. model described in section 3.2.2.4 and has been taken from a paper by Chemelli and DeChiaro[17]. In this paper the authors stressed the importance of adding the system inductance in series with the normal "human body" elements and the parasitic shunt capacitance across the body resistance. Therefore the model adopted in this thesis has included both these parasitic elements. The AutoZap circuit model is shown below in fig. (8.10).

![AutoZap Circuit Model](image)

Fig. (8.10) AutoZap Circuit Model

8.6.2 Voltage Probe

The HP10440A voltage probe was used to measure the voltage across the device as a function of time, and has the following characteristics:

i) Probe input resistance 10M\(\Omega\)
ii) Probe input capacitance 2.5pF
iii) Division ratio 100:1
iv) Cable length 1m
These characteristics are translated into the probe circuit model shown in Fig. (8.11).

![Circuit Model with 3pF, C, R, and 10 MΩ](image)

**Fig. (8.11) HP10440A Voltage Probe Circuit Model**

### 8.6.3 Current Probe

Using the TEK CT1 current probe, the current in the main discharge path can be measured. This probe is not directly connected to the circuit, but simply measures the magnetic field created by the current passing through a wire. Its characteristics are as follows:

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>i) Sensitivity (50Ω load)</td>
<td>5mV/mA</td>
</tr>
<tr>
<td>ii) Insertion impedance (50Ω load)</td>
<td>1Ω</td>
</tr>
<tr>
<td>iii) Inductance (50Ω load)</td>
<td>5μH</td>
</tr>
<tr>
<td>iv) Capacitance loading</td>
<td>1pF</td>
</tr>
<tr>
<td>v) Bandwidth (flat)</td>
<td>100kHz-10MHz</td>
</tr>
</tbody>
</table>

These characteristics are translated into the circuit model in Fig. (8.12).
8.6.4 Pulse Transmission Elements

In order to transfer the ESD pulse to the device the pulse could travel through one of two media. These are:

a) A Coaxial Cable

b) A large cross-section copper wire
   (coaxial cable with the outer floating)

The choice of which medium to use depends on the electrical stability of the layout. The coaxial system has the advantage of keeping the impedance constant regardless of the physical position of the cables, but has a large capacitance to ground. The copper wire system has low inductance and a low capacitance, provided the wire is kept away from any ground planes. In order to preserve the consistency of the pulse shape, the coaxial system was adopted. This model was favoured after consultation with Philips Research in Holland[18].

Fig. (8.12) CT1 Current Probe Circuit Model
8.6.5 ESD Characterisation Circuit

In order to understand the effects of the extrinsic circuit components on the current and voltage waveforms receive by a device during an ESD event, another characterisation circuit model has been built up of all the possible components in the ESD system, using values measured by the Wayne Kerr LCR bridge. The circuit model is shown in fig. (8.13). The model includes the measurement probes and a characterisation resistor instead of the device. The current and voltage waveforms predicted using this circuit are for a +100V initial charge voltage on the AutoZap capacitor, and a range of values for the characterisation resistance between 50Ω and 1500Ω.

The predicted voltage and current waveforms are shown in figs. (8.14) and (8.15). These results can be compared to the experimental results also shown in fig. (8.15). The voltage waveforms compare very favourably with the experimental results except that the measured peak values are larger than those predicted at the higher load resistances. This suggests that additional parasitic elements are present in the system. The peak values are far below those expected for a simple resistive divider indicating that the transmission line is changing the impedance of the circuit external to the AutoZap as suggested in section 6.2.

The peak values of the current waveforms also compare favourably with the experimental results although the PSPICE model predicts a slower rise, and faster decay, than observed in the experimental results. This may be attributed to additional parasitic circuit elements. One may compensate for this effect by increasing the value of the AutoZap capacitance. This will change the time scale of the rise and decay portions of the waveforms, but will not change the peak values greatly leaving them sufficiently accurate for the purposes of this study.
Fig. (8.14) Voltage Characterisation Waveforms

Fig. (8.15) Current Characterisation Waveforms
8.7 MES Diode Circuit Design and Evaluation

8.7.1 Introduction

It has been suggested in chapter 6 that many of the effects observed in the current and voltage waveforms during an ESD event are likely to be a function of either:

a) The external components to the device, i.e. the pulsing and transmission systems.

b) The DC characteristics of the MES diode.

In order to predict the effects the external components, and those of the MES device, during an electrostatic discharge event, a circuit model has been derived using the ESD characterisation circuit described in section 8.6 and a model predicting the DC characteristics of a typical MES diode. This software package can be used to predict the current or voltage at any element within a circuit model as a function of time.

The electrical properties of the device are vastly different for positive and negative polarity pulses. The presence of the current saturation region in the positive polarity case, and the depletion region in the negative polarity case requires the development of separate models. Only the positive polarity case will be considered in this thesis because these results, shown in chapter 5, are considered the most accurate.

The principle is to model typical $I_{gs}$ vs $V_{gs}$ characteristic measured from the 169W\169X wafers and combine this model with the AutoZap and transmission line model to yield a complete circuit model for ESD analysis. The transient analysis predictions can then be compared to the experimental results in chapter 5. This analysis can be used to distinguish between external circuit effects from internal device related effects on the experimental waveforms.
8.7.2 Positive Polarity Circuit Model

Fig.(8.17) shows a typical \( I_{gs} \) vs \( V_{gs} \) plot for a 1\( \mu \)m MES diode on the 169X\( \backslash W \) wafers. The curve can be split into several regions of voltage and current showing the differences in effective resistance as the gate/source voltage is increased.

**Region 1** - The initial portion of the characteristic is controlled by the metal/semiconductor junction which resembles a typical forward biased diode. Initially exponential in nature, it is limited at >1V by the internal source resistance + ohmic resistance.

**Region 2** - Region 1 is followed by a current saturation region due to velocity saturation and then space charge limited conduction between the gate/source contacts. In virtually all cases this region exhibits a finite resistance.

**Region 3** - The final portion of the characteristic is associated with the thermal runaway of the device. The current rise is virtually instantaneous at the DC breakdown voltage \( V_{th} \approx 6V \). Above this region it has been shown in chapter 6 that, under pulse conditions, the voltage drops rapidly by 1-2V due to the device exhibiting negative differential resistance. Subsequent to this voltage drop the device once again exhibits positive differential resistance at \( V_{sb} \approx 5V \) and the current then increases reasonably linearly with voltage having a characteristic resistance of \( \approx 5\Omega \), measured using the reconstructed \( I_{gs} \) vs \( V_{gs} \) characteristics for a subthreshold pulse as discussed in section 6.4.5.1.

The different regions of the curve can be modelled using the circuit elements available in the PSPICE library. How this is achieved is explained below:-

**Region 1** - A diode, with the model parameters derived iteratively, to give the exponential rise, followed by a linear region with a characteristic resistance of 15\( \Omega \), can be used to model this region of the characteristics. The diode model is DIO.
Region 2 - The current saturation region can be predicted using the standard MESFET model by grounding the gate via a $10^{12} \ \Omega$ resistor to render it inoperative. The normal current saturation characteristics can be controlled by changing the model parameters LAMBDA, ALPHA and BETA. The GASFET model is GAS.

Region 3 - The final thermal runaway region can be predicted using a Zener diode programmed to breakdown at the voltage at which the device begins to exhibit positive differential resistance at $V_{sb} = 5V$ thereafter allowing the current to increase linearly with a characteristic resistance of $5\Omega$. The diode model is DIO1.

Fig. (8.16) Positive Polarity Circuit Model

The program which models this circuit is shown below with explanations where necessary:-
Using the circuit in Fig. (8.16) the $I_g$ vs $V_{gs}$ characteristic of the device model can be plotted. The results for a typical MES diode are shown in fig. (8.18). A comparison with the typical characteristic shown in fig. (8.17) shows the PSPICE model accurately predicts the low voltage\current regime of a MES diode except the breakdown point occurs at $V_{bh}$ rather than the normal DC threshold, $V_{th}$. During ESD stress it has been shown in chapter 6, that the device voltage\current will rise far above the region shown in figs. (8.17) and (8.18). The device will consequently enter a region modelled by the $5\Omega$ series resistance, and, if sustained in this region, will eventually breakdown due the creation of a irreversible short circuit path between the electrodes. Figs. (8.19) and (8.20) show the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics for a +1000V and +1500V ESD pulse with the reconstructed PSPICE model superimposed on the results. The results show that the PSPICE model accurately predicts the sub-threshold MES diode current\voltage characteristics, apart from the high initial ringing, under ESD high voltage stress. The PSPICE model becomes inaccurate when the devices
fails, see fig. (8.20). The premature collapse of the voltage at 8V probably indicates the creation of a short circuit path between the contacts.

Using the combination of the circuit models for the AutoZap, transmission medium and device, the final model for the ESD analysis can be derived. This circuit is shown in fig. (8.21). The full program for the analysis of the ESD transient event with the initial AutoZap charge voltage of +100V is shown below with explanations of each line where necessary.

*Positive Polarity Coaxial ESD Circuit Model
*A.J. Franklin - 1989

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>autoZap capacitance</td>
<td>100pF</td>
<td></td>
</tr>
<tr>
<td>autoZap resistance</td>
<td>1500</td>
<td></td>
</tr>
<tr>
<td>shunt capacitance</td>
<td>0.5pF</td>
<td>Measured autoZap shunt capacitance</td>
</tr>
<tr>
<td>inductance</td>
<td>3.10μH</td>
<td></td>
</tr>
<tr>
<td>transmission line</td>
<td>30-40Ω</td>
<td>Outward Transmission Line</td>
</tr>
<tr>
<td>probe resistance</td>
<td>4.5Ω</td>
<td>Current Probe resistance</td>
</tr>
<tr>
<td>inductance</td>
<td>5Ω</td>
<td>&quot; inductance</td>
</tr>
<tr>
<td>capacitance</td>
<td></td>
<td>&quot; capacitance</td>
</tr>
<tr>
<td>measurement</td>
<td></td>
<td>Current measurement element</td>
</tr>
<tr>
<td>D1, D2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1, D10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rhp</td>
<td>8.10E6</td>
<td>Voltage probe resistance</td>
</tr>
<tr>
<td>Chp</td>
<td>8.3pF</td>
<td>&quot; capacitance</td>
</tr>
<tr>
<td>Tout</td>
<td>0.0</td>
<td>Inward Transmission Line</td>
</tr>
<tr>
<td>D = 75Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B = 8GAS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D = 6DIO1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R = 6810E6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C = 83pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tout = 90Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TD = 10ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

.PROBE - Probe Graphics

.end

Using the PSPICE algorithm for a transient analysis, the above circuit model can be analysed and the voltage vs time waveforms can be predicted at any node.
Fig. (8.17) Typical Forward Bias Gate-Source Diode Characteristic

Fig. (8.18) $I_{gs}$ vs $V_{gs}$ plot for a 169X/W MES diode
Fig. (8.19) Current Voltage Characteristics for a +1000V ESD Pulse

Fig. (8.20) Current Voltage Characteristics for a +1500V ESD Pulse
8.7.3 ESD Voltage Analysis

Using the PSPICE transient routine the model derived for the full system can be analysed to assess the effects of changing the initial charge voltage on the AutoZap capacitor. This voltage has been varied between +300V and +900V to allow a direct comparison to be made between with the experimental results of chapter 5. The predicted PSPICE waveforms are shown in figs. (8.22) and (8.23) superimposed with the experimental results for the I69W wafer at +300V, +600V and +900V. Examination of the results shows:

(a) The same general profile of the voltage and current waveforms are observed in both the predicted and experimental results.

(b) The Initial ringing in the waveforms is not accurately predicted.

(c) The duration of the voltage "plateau" region is not accurately predicted.

(d) The decay time constant of the current waveforms is not accurately predicted.

(e) The rise in voltage at the end of the voltage plateau region is not predicted.

(f) The voltage at which the sharp increase in time constant occurs in the predicted results is nearly 2V lower than observed in the experimental results.

The model predicts the correct current and voltage profiles, thus the initial assumption that the experimental waveforms are dependant on the external circuit elements and general profile of the DC characteristics seems justified. The large ringing in all the waveforms must indicate that either the device is not following the true DC current/voltage relationship during the rising portion of the waveforms or the presence of small inductive parasitic elements are
becoming significant due to the large changes of current over a short time. The error in the plateau duration is probably due inaccuracy in the decay time constants of the current waveforms. This effect is also observed in the characterisation waveforms at the low values of load resistance. It is possible, however, that the device is being sustained in the post NDR region for a longer duration, thus distorting the current decay profile. If the decay time constants were much longer, as characterised by a larger capacitance, the voltage plateau region would be sustained for a far longer time and so match the experimental results more accurately. The rise in voltage when the device enters the NDR region toward the end of the waveform is not predicted because this effect was not present in the model of the DC characteristics. The voltage at which the sharp increase in time constant occurs near the end of the pulse is lower than the experimental results, because the voltage at which the saturation region begins is lower than observed in the experimental results used for comparison. If the DC current\voltage characteristic were tailored for individual devices, this would also give rise to far greater correlation between the predicted and experimental waveforms.

8.7.4 AutoZap Capacitance Analysis

Using the PSPICE transient routine the model derived for the full system can analysed to assess the effects of varying the AutoZap capacitance(100pF to 1000pF) on the voltage and current waveforms, at a fixed ESD charge voltage of +100V. The predicted waveforms are shown in figs. (8.24) and (8.25) superimposed on the experimental results for the I69W wafer at 100pF, 500pF and 1000pF. Similar observations to those observed in section 8.7.2.1 can be made. The changes in the duration of the plateau region are more accurately predicted in these results. The experimental results show sharp steps in the current waveforms at ≈35mA which correspond to the point in the voltage waveforms where the voltage begins to drop after the plateau region. This effect is also seen in the PSPICE prediction by a slight flattening in the current waveforms at ≈40mA which corresponds to the point at which the region of negative differential resistance(NDR) ends and the current saturation region begins.
Fig. (8.22) Voltage Waveforms at +300V, +600V and +900V

Fig. (8.23) Current Waveforms at +300V, +600V and +900V
Fig. (8.24) Voltage Waveforms for Capacitance Variations from 100pF-1000pF

Fig. (8.25) Current Waveforms for Capacitance Variations from 100pF-1000pF
8.7.2.3 Pulse Transmission Medium Effects

The results observed in section 5.5.6.2 show that the device voltage increases as the external capacitance was increased from 100pF to 1000pF. This was attributed to the impedance mismatch between the AutoZap and the transmission medium. This assumption can easily be tested using the PSPICE circuit model using the characterisation circuit of fig. (8.13). The load resistance is fixed at 1MΩ in order to mimic the nominal leakage of a reverse bias diode. The transient response of the characterisation circuit at a fixed AutoZap charge voltage of 50V is shown in figs. (8.26) and (8.27) where V(6,0),i(vm), v(13,0),i(vm1) and v(20,0),i(vm2) are the 100pF, 500pF and 1000pF results respectively. These results show that the load voltage and current increases with the external AutoZap capacitance. Figs. (8.26) and (8.27) can be compared to the experimental results in figs. (5.47) and (5.48). These show similar relationships, though the ringing in the current waveforms is much less in the experimental results. The presence of the transmission line also effects the device voltage under positive polarity stress. The positive polarity waveforms shown in fig. (5.45) and (5.46), show the peak voltage and current values for the 100pF capacitance, are lower than that observed for the higher capacitance values. Care must therefore be taken when interpreting any voltage threshold relationships as a function of the external capacitances using this system. Therefore, the results shown in figs. (5.35) and (5.36) will be effected by the presence of this mismatching effect in the system. The positive polarity voltage threshold at 50pF and 100pF are likely to have the greatest error. The gradient of the log threshold vs log capacitance plot predicted in section 6.4.4 is prematurely high because the device did not receive the full voltage at these lower values of capacitance. The negative polarity threshold is likely to be effected to a far greater extent because of the high effective resistance of the device whilst the voltage is rising. The voltage will only reach -25V for a -50V applied pulse with 100pF capacitance, but using the 1000pF capacitance the device would reach the full charge voltage of -50V. Therefore, it would be expected that the negative polarity threshold voltage would be ≈25V lower at the higher value of capacitance. Examination of the results in fig. (5.36) shows this to be true.
Fig. (8.26) Voltage Characterisation Waveform vs AutoZap Capacitance

Fig. (8.27) Current Characterisation Waveform vs AutoZap Capacitance
8.8 Summary

PSPICE computer models have been derived for both the ESD pulse generation system, transmission medium, MESFET and an MES diode. These models have been combined to generate a complete model of the ESD system. Using the transient analysis routine available in the PSPICE software the current and voltage waveforms present during an ESD event have been assessed. These compare very favourably with the results in chapter 5 and show that the waveforms measured during an ESD event can be linked in part to:

a) The device DC characteristics.
b) The pulse generation and transmission system.

The degradation categories of the MESFET $I_{ds}$ vs $V_{ds}$ characteristics subsequent to an ESD pulse have been analysed and have confirmed some of the failure modes suggested in chapter 6. Finally, the effects of the impedance mismatch between the AutoZap and pulse transmission medium have been modelled, thus giving a greater understanding of how the experimental system effects the actual device waveforms and consequently the voltage threshold vs capacitance relationships shown in chapter 5 have been shown, at least in part, to be due to this mismatching effect.

8.9 References

<table>
<thead>
<tr>
<th></th>
<th>Reference</th>
</tr>
</thead>
</table>
CHAPTER 9

CONCLUSIONS and FUTURE STUDY

9.1 Introduction

The study reported in this thesis has identified some of the possible electrical overstress failure mechanisms in GaAs MES structures. Particular emphasis has been placed on identifying the physical mechanisms which lead to complete thermal breakdown in GaAs MES devices. A analytic and experimental study has also been presented that predicts the threshold failure time for a three dimensional defect subject to EOS and exponentially decaying ESD pulses. The analytic models are not, of course, restricted to GaAs MES devices and are expected to predict the thermal failure characteristics in many other semiconductor devices.

9.2 ESD Degradation in GaAs Devices

9.2.1 ESD Failure in GaAs MESFETs

The study has shown that low-noise MESFET/MES structures are highly sensitive to ESD pulses. Subsequent to low voltage ESD stress the device DC characteristics can degrade without showing any visible damage on the surface. At the higher ESD voltages visual damage is evident. This damage, normally occurring between the two closest contacts, acts as a short circuit resistance between the contacts. This resistance can be from a few ohms to several megohms depending on the severity of the damage. The main conclusions from these experiments are that ESD sensitivity is:
a) Voltage Dependant - As the ESD charge voltage is increased the likelihood of degradation/burnout increases.

b) Polarity Dependant - Positive polarity pulses have a far higher degradation threshold than negative polarity pulses.

c) Charge Dependant - The positive polarity degradation threshold decreases as the amount of available charge within an ESD pulse is increased. The negative polarity threshold decreases slightly for the same increase in charge.

d) Temperature Dependant - The degradation rate increases for positive polarity pulses and decreases for negative polarity pulses.

d) Geometry Dependant - The majority of visible failures occur between the two closest contacts, i.e between the gate-source contacts.

It was also observed that sequential pulsing of MESFET structures resulted in cumulative degradation in the $I_{ds}$ vs $V_{ds}$ characteristics and eventually resulted in catastrophic failure, although the extent of degradation after any particular pulse could not be predetermined. Many of the devices which showed degraded characteristics would pass a screening test based on a simple pass-fail system. Such devices, which can be classified as "walking wounded" failures, may enter the market place as useable devices. The degraded $I_{ds}$ vs $V_{ds}$ characteristics may be a result of subtle changes in the ohmic/contact resistance, net donor level, advancement of the depletion layer or changes in the surface properties of the GaAs.

9.2.2 Forward Bias MES Diode Physical Model

The device impedance under forward bias stress is relatively small compared to the 1.5kΩ "body resistance", thus, during ESD stress, the majority of the voltage will appear across the 1.5kΩ resistance and the device voltage will be
controlled by the exponential current profile. Hence, the forward bias ESD breakdown is highly dependant on the external circuit elements of the ESD pulsing apparatus and therefore dependant on the circuit model used for ESD threshold assessment. It has been established that a GaAs MES device under forward bias ESD stress will suffer a period of current controlled negative differential resistance (NDR) which is not observed in the DC $I_{gs}$ vs $V_{gs}$ characteristics. This effect is only observed in the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics of an ESD pulse. Negative differential resistance in GaAs is a result of intervalley scattering at sufficiently high fields\cite{1,2} and the reconstructed $I_{gs}$ vs $V_{gs}$ curves show a near classical current controlled NDR response. After the device has passed through the region of negative differential resistance the device re-enters a region of positive differential resistance (PDR) and it is while the device is operating in this region that current filamentation is likely to occur\cite{2}. It has been shown that it is the power dissipated at these localised current filaments, whilst in this PDR region, which allows joule heating to occur causing the temperature to rise and eventually causes catastrophic failure.

Increasing the amount of charge within an ESD pulse by increasing the "body capacitance" causes the ESD positive polarity degradation threshold to decrease dramatically. This is due to the increase in the decay time-constant of the current waveform which allows the device to be sustained longer in the PDR region and thus increases the probability of breakdown.

An increase in the ambient temperature causes the positive polarity voltage threshold to decrease dramatically for a 150°C rise in temperature. The peak field required for the onset of NDR in GaAs actually increases with temperature\cite{3}, but the temperature difference between the ambient and the critical temperature decreases which would thus decrease the power required for breakdown in this condition. But, this large change over such a small range in temperature is greater than expected, which was also found during the EOS burnout experiments. Thus, it appears that the increase in the ambient temperature may cause enhanced current channelling within the device under both EOS and ESD stress which would allow the device to burnout at a much lower input power.
9.2.3 Reverse Bias MES Diode Physical Model

In contrast to the forward bias case, the negative polarity ESD threshold is highly voltage dependant. It has been shown that the DC avalanche voltage must be attained before there is sufficient current flow within the device. At this point the dynamic resistance of the device drops considerably and the majority of the excess voltage will thus be transferred to the 1.5 kΩ "body resistance". The device current is now sufficient to cause significant joule heating of the structure which forces the temperature rise at points where the current density is greater than the average for the junction. The depletion layer will remain stable until the critical temperature is reached and burnout occurs. At this point the depletion layer voltage collapses and a large current spike is evident. As the ambient temperature is increased the negative polarity threshold increased. This may be linked to the duration of the voltage plateau region increases as a function of the ambient temperature and this is linked to the decrease in the current saturation region evident during DC characterisation. The voltage at which a device enters the avalanche condition under negative polarity stress is dictated by the impact ionisation coefficients which are a sensitive function of temperature[4]. Thus, as the temperature is increased a higher voltage is required to initialise\sustain impact ionisation, but the smaller difference between the ambient and critical temperatures will decrease the power required for catastrophic failure.

9.3 Quantitative Thermal Models

9.3.1 EOS Thermal Breakdown Model

A three dimensional thermal model has been developed which allows the conditions for thermal breakdown in semiconductor devices to be predicted. This model, derived from first principles, defines the $P_t$ vs $t_r$ relationship for a three dimensional "defect" site to reach a critical temperature. The model has been tested for GaAs MES structures under forward bias and the results indicate that, within given failure time domains, GaAs structures of this kind follow the same general patterns, $P_t \propto t_r^q$, as those previously reported for silicon semiconductor
devices. There is one exception. In the time domain roughly between 1 and 20μs, the failure power is given by \( P_f \propto 1/\log_e(t_f) \).

Analytic expressions which predict the three "defect" dimensions from experimental data have also been derived. These "defect" dimensions have been discussed with reference to the device dimensions and the ambient temperature and show that defect dimensions may be related to the gate width, gate-source distance and the n-type layer depth and decrease with temperature. Two distinct visible and electrical failure modes have been observed and these have been linked to the channel conductance changing subsequent to an applied pulse.

### 9.3.2 ESD Thermal Breakdown Model

A further analytic model has been developed which predicts the minimum ESD voltage required for a three dimensional "defect" to attain the critical temperature. This model predicts that thermal failure can only occur within a specific time "window" during ESD pulse. The boundaries of this time window are linked to the CR decay constant of the ESD pulse and the smallest dimension of the defect. The model predicts a slightly higher peak current and lower failure time than measured for GaAs MES diodes under forward bias ESD stress. The low predicted failure time is attributed to the errors in the smallest defect dimension which requires accurate EOS \( P_f \) vs \( t_f \) data in the time range <100ns which was not possible with the present experimental set-up. Under positive polarity ESD stress the device is subject to an exponentially decaying current, the characteristics of which are controlled mainly by the components external to the device. The physics of operation in the region of negative differential resistance under current stress are different from those under voltage stress[2]. Thus, the high predicted value of the peak current may be due to an error in the Wunsch & Bell damage coefficient which was calculated from the burnout data under **constant voltage** stress.
9.4 PSPICE ESD Model

The complete ESD pulsing and measurement system has been modelled using the software package PSPICE. The model has been used to test the characteristics of the pulsing system into standard loads and has shown that the transmission lines/flying leads between the "human body" circuit and a device will change the breakdown threshold of a device. This makes the comparison of voltage threshold values, with previous studies using packaged devices, difficult.

A device model has also been derived which models a GaAs device under high forward bias stress. This has been achieved by modelling the DC\reconstructed $I_{gs}$ vs $V_{gs}$ characteristic using standard circuit elements and tailoring the characteristic to model the PDR region with an "effective resistance" which has been taken to be the inverse gradient of the reconstructed $I_{gs}$ vs $V_{gs}$ characteristics above the normal DC current saturation region. This model has been used to test the effects on the device waveforms of variations in ESD voltage and the "human body" capacitance. The predicted waveforms associated with increasing the ESD voltage show a shorter voltage plateau region than observed in practice either indicating the presence of further parasitic circuit elements or the non-linear properties of a device operating in the NDR region. The predicted waveforms associated with an increase in capacitance show a good correlation with the experimental results.

9.5 Future Study

One of the major problems associated with the study reported in this thesis was the unavailability of consistent devices, with detailed processing information, with which a more precise experimental study of the degradation effects of ESD and EOS pulses could be completed. Nevertheless, the study has identified some global aspects of breakdown in GaAs MES structures, particularly with regard to the assessment of the device waveforms during overstress which have not so far been reported. Hence, with an improved experimental system and consistent devices this study could be the basis of a
more comprehensive experimental study to verify the physics behind breakdown in structures of this kind.

A future study into the effects of EOS and ESD pulses on GaAs structures could be separated into four main areas:

a) *An improvement of the experimental system.*

b) *An investigation of EOS breakdown under constant current conditions.*

c) *An investigation of ESD breakdown in varying geometry devices.*

d) *The possible extension of the analytic and computer models.*

### 9.5.1 Improvement of the Experimental System

Some of the effects described in the experimental study have been attributed to the experimental apparatus. Even though this set-up is probably one of the best in the U.K. it still suffers from the fact that a large amount of ringing is present with any waveforms generated by the system. The presence of the transmission line also changes the profile of the current and voltage waveforms at the device. Unfortunately the transmission line is necessary in order to transfer consistent pulses to a device. These cannot be replaced if devices are to be probed on-wafer. The only possible solution to this is to make these as short as possible thus decreasing the capacitance to earth. Much has been gained from the existing literature on the various ESD profiles measured during characterisation experiments over the past decade, which has recently prompted the new MIL STD specification for an ESD pulse. The new MIL STD 883C specification is characterised by discharging the "body capacitance" into a zero ohm load[5]. This has the added advantage of defining the pulse under the worst case conditions. The current pulse must rise within 10ns and have virtually zero ringing at any point within the waveform. With this specification, any changes to the typical current waveform may be attributed to the device under stress and not the experimental system. The current version of the AutoZap ESD system has adopted this specification and this has resulted in many fundamental changes to the basic instrument used in this study.

It has been postulated that GaAs MES devices under forward bias stress
will exhibit different breakdown characteristics depending on the type of stress. Therefore an experimental system which can produce constant current or constant voltage pulses with a rise-time of less than 10ns and response time in the order of nanoseconds is required. This would allow the differences in the EOS threshold to be measured for each type of stimulus and thus give accurate $P_f$ vs $t_f$ data in the elusive time region below 100ns.

9.5.2 Constant Current EOS Breakdown

It is postulated that under current-controlled EOS breakdown the properties of a GaAs device will be different from those observed under constant-voltage breakdown. Therefore, an experimental study along lines similar to those reported in section 7.5, but using constant current pulses and a larger temperature range, will indicate whether this is in fact true. If this is the case it may be possible to account for some of the differences between the predicted ESD threshold and that observed in practice.

9.5.3 ESD Geometrical Sensitivity

The devices used in this study were fabricated using similar mask sets, but the measured differences between the devices on the same wafer were such that it has been difficult to relate any of the observed effects to geometrical differences between the devices on different wafers. A more comprehensive study, using the improved experimental system, would require fabrication of specific device structures to examine the geometrical effects on device sensitivity. The following device parameters would require study:

i) A study of the effect of gate length/width, channel depth and gate-ohmic distance on device sensitivity. This could also include the effects on crystal orientation which is known to effect the impact ionisation coefficients[6].

ii) The carrier density is likely to effect sensitivity and therefore a set of devices with the carrier density varying between $10^{15}$ to $10^{18}$ cm$^{-3}$ would
allow this to be ascertained. This could also include the effects of n+ wells under the ohmic contacts.

iii) The use of different gate and ohmic metals, such as TiPtAu and InGeAu, would identify whether the metallisation plays a role in the breakdown process. It has been assumed in the present study that burnout is initiated within the semiconductor and the metals play only a secondary role in the burnout process.

iv) GaAs has no good native oxide which allows the device to be passivated to prevent environmental damage. Polyimide has been used to passivate the devices used in this study. The presence of the surface depletion layers may be effected by the type and processing of different passivations. Therefore, a study of the effects of passivations such as SiO$_2$, and Si$_3$N$_4$, or even just a single passivation processed differently, may identify the role of the surface on device sensitivity.

9.5.4 Extension of the Analytic Models

The analytic models derived as part of this study represent a major step forward in the modelling of thermal breakdown. The models are quite general and could be used to predict the thermal breakdown characteristics in many semiconductor devices. The application of the simplified Wunsch & Bell and Tasca models have been extensively reported in the literature for Si based p-n structures[5-12], but no literature has been found by the author on the application of these models to GaAs based structures.

The EOS model derived as part of this study pictures the "defect" within a semiconductor device as a rectangular parallelepiped composed of a number of point heat sources providing uniform heat dissipation. This is unrealistic because in many semiconductor devices the heat distribution can be split into two separate regions, the power dissipated near the junction and the power dissipated in the bulk resistance. A natural extension to the analytic model would encompass these effects, this would lead to a more accurate ESD model, which at present assumes the two contributions to the dissipated power are contained
in a single region. One of the basic assumptions of the EOS model is that the thermal parameters $\rho$, $C_p$ and $K$ are temperature independent. This is not the case in practice[13]. Thus, a possible further extension of the model would be to include temperature dependent thermal parameters. This is likely to make the analytic solution very complex, if not impossible, and may require the use of finite element packages such as ANSYS or PATRAN.

The PSPICE circuit model has been shown to model the system with reasonable accuracy. The model can be extended to include the drop in voltage from $V_{th}$ to $V_{sb}$ which will increase the accuracy in the estimation of the voltage plateau duration. A further assessment of the possible parasitic elements present in the circuit will increase the accuracy further. This type of analysis will allow the differences between the circuit and device effects to be analysed.

9.6 Summary

This chapter has discussed the various degradation effects of ESD and EOS pulses in GaAs MES structures. The sensitivity of a GaAs MES device depends on the ESD voltage magnitude and polarity, available charge and ambient temperature. Two qualitative models have been proposed which have identified that under positive polarity stress the device exhibits a region of current controlled negative (positive) differential resistance and it is sustained operation in this mode which eventually leads to thermal breakdown. Under negative polarity ESD stress, the depletion layer plays an important role in limiting the current until the DC avalanche voltage is attained. Above this voltage, sufficient current can then flow though the device to induce thermal breakdown.

Possible areas of future study have been identified. These include improvements in the experimental system, investigation of device geometrical and structural changes and extensions to the analytic\computer models derived in this study.
9.7 References


APPENDICES

A - MathCad Computer Programs
B - PSPICE Computer Programs
C - IEEE Control Programs
D - Abstracts from Reports
E - Abstracts from Papers
APPENDIX A

MathCad COMPUTER PROGRAMS

The programs reproduced here are in ASC Text format. When these programmes are loaded into the MathCad package with an extension .MCD they are interpreted as expressions within a spreadsheet. The complex expressions are solved using internal subroutines within the software package.

A1 EOS Model

.MCD 20000 0
.CMD PLOTFORMAT logs=0,0 subdivs=1,1 size=5,15 type=1
.CMD FORMAT rd=d ct=56 im=i et=3 zt=15 pr=3 mass length time charge
.CMD SET ORIGIN 0
.CMD SET TOL 0.001000
.CMD MARGIN 0
.CMD LINELENGTH 78
.CMD SET PRNCOLWIDTH 8
.CMD SET PRNPRECISION 4
.CMD FILENAME ESDPOW.dat ESDPOW.dat
.CMD FILENAME ESDTIME.dat ESDTIME.dat
.TXT 2 17 1 42
  a1,41,61,40
Electrical Overstress 3-D Thermal Model
.TXT 3 11 1 16
  a1,15,57,14
A.J. Franklin
.TXT 3 -27 2 67
  a2,66,73,97
The Input power vs Failure time for the three thermal models is calculated using this package.
.TXT 1 0 3 69
  a3,68,75,189
The Input power vs Failure time for the three thermal models is calculated using this package. The a,b,c values correspond to the defect dimensions along the x,y,z axes. The Failure temperature is \( Q \) defined at its absolute value, i.e. for GaAs at 1511 K\( \).\( Q \)
.TXT 4 0 2 23
  a2,22,77,22
Define a,b,c in um \( Q \)
Define critical temperature in K

Now press escape and type GOTO 81 and WAIT!

If you require HELP for any MathCad statement press F1 at any time
The above plots represent the time to failure of a defect with a cuboid geometry. The differing patterns in the P vs t relationship are seen as straight lines on each graph.

To change the scale on any graph move to the xmin/xmax/ymin/ymax value, delete, and replace with the new value and press F9. Use the cursor keys to scroll around the screen if required.
A2  ESD Model

.MCD 20000 0
.CMD PLOTFORMAT logs=0,0 subdivs=1,1 size=5,15 type=1
.CMD FORMAT rd=d ct=56 im=i et=3 zt=15 pr=3 mass length time charge
.CMD SET ORIGIN 0
.CMD SET TOL 0.000000
.CMD MARGIN 0
.CMD LINELENGTH 78
.CMD SET PRNCOLWIDTH 8
.CMD SET PRNPRECISION 4
.CMD FILENAME CAP.DAT CAP.DAT
.CMD FILENAME time.DAT time.DAT
.CMD FILENAME vc.dat vc.dat
.CMD FILENAME c.dat c.dat
.EQN 1 41 2 15
A: 1.4*10^-6 Q
.EQN 0 19 2 16
B: 3.16*10^-3 Q
.EQN 1 -39 1 11
T: 1511 Q
.EQN 3 -8 2 21
K: 20800*(T^-1.09) Q
.EQN 0 22 2 25
\[ I: 5.32 -9.91*10^{-5} T^Q \]
.EQN 0 27 2 30
Cp: 3.02*10^{-5} T + 0.322324 Q
.EQN 3 -27 4 13
D: K*10^{-6}/[Cp] Q
.EQN 1 -23 3 17
c: (\pi D)^0.5 A/B Q
.EQN 0 40 2 15
r: 260*10^{-9} Q
.EQN 1 15 1 12
Rb: 1500 Q
.EQN 4 -56 2 16
c: 1.52*10^{-6} Q
.EQN 1 29 2 18
D= ?^Q
.EQN 4 -29 4 13
tc: c^2/(4*\pi*D) Q
.EQN 0 28 2 18
tc= ?^Q
.EQN 6 26 4 11
xc: (tc/r)^Q
.EQN 1 -34 1 9
Rd: 5 Q
.EQN 0 15 1 9
Vj: 5 Q
I_{o1} = ?^Q
.EQN 0 55 1 9
I_p = ?^Q
.EQN 4 -56 2 59
I_{o2} = \sqrt{\left((B^*r^{-0.5} - V_j I_p r^{-0.632} - R_d I_p r^{-2} 0.432), I_p \right)^2}
.EQN 2 81 1 26
V_c = I_{o2} (R_d + R_b) - V_j^Q
.EQN 1 -61 2 16
r = ?^Q
.EQN 0 20 2 18
V_c = ?^Q
.EQN 1 -40 1 15
I_{o2} = ?^Q
.Io2 - ?^Q
.EQN 4 -1 1 17
i_0.7;1500^Q
.EQN 0 30 3 14
t[i; i*10^{-9}^Q
.EQN 5 -30 6 17
[i; i*10^{-9} - (t[i/r])^Q
.EQN 6 26 2 14
P_d[i; i*10^{-9}^Q
.EQN 0 18 5 23
P[i; i*V_j i^Q
.EQN 4 -22 25 46
20 & 0 & V_t[i\{20, 15, 20, 40, 1\} @ 1.5*10^{-6} & t[i^Q
.EQN 25 1 5 24
WRITEPRN(ti.dat): t[i^Q
.EQN 5 0 5 25
WRITEPRN(Vt.dat): V_t[i^Q

A3 GaAs Resistivity Model

.MCD 20000 0
.CMD PLOTFORMAT logs=0,0 subdivs=1,1 size=5,15 type=1
.CMD FORMAT rd=dt ct=56 im=i et=3 zt=15 pr=3 mass length time charge
.CMD SET ORIGIN 0
.CMD SET TOL 0.000000
.CMD MARGIN 0
.CMD LINELENGTH 78
.CMD SET PRNCOLWIDTH 8
.CMD SET PRNPrecision 4
.CMD FILENAME GaAs.dat GaAs.dat
.CMD FILENAME TEMP.dat TEMP.dat
.CMD FILENAME one.dat one.dat
.CMD FILENAME temp.dat temp.dat
.EQN 1 14 1 21
i:300,320;1240^Q

A 6
.EQN 0 21 2 9
T[i]=i^Q
.EQN 3 -21 1 12
m=0.067^Q
.EQN 0 15 1 9
mo=1^Q
.EQN 0 31 6 37
E[i]=(1.519-5.405*10^-4*T[i]^2/(T[i]+204))^Q
.EQN 3 -46 1 13
mde=m*mo^Q
.EQN 4 0 3 35
mdh=(0.080*1.5+0.45^1.5)^0.6666^Q
.EQN 1 46 4 20
k=1.38066*10^-4/1.602^Q
.EQN 1 49 5 29
E[i]=^Q
.EQN 3 -95 1 9
Mc=1^Q
.EQN 4 0 8 52
N[i]=4.9*10^15*(mde*mdh/mo^2)^0.75*Mc^0.5*T[i]^1.5*e^-(E[i]/(2*k*T[i]))^Q
.EQN 3 61 5 21
\mu_h[i]=400*(300/T[i])^2.3^Q
.EQN 9 -66 3 33
n[i]:=if(N[i]>1*10^-17,N[i,1*10^-17]^Q
.EQN 0 37 5 26
\mu_h[i]=1/(\mu_h[i]^n[i]*1.602*10^-19)^Q
.EQN 7 -37 3 34
ns[i]:=if(N[i]>1*10^-13,N[i,1*10^-13]^Q
.EQN 0 36 5 28
\mu_h[i]=1/(\mu_h[i]^n[i]*1.602*10^-19)^Q
.EQN 7 -31 22 59
&-2&log(\mu_h[i],log(\mu_h[i]{6,13,20,40,1}@1573&273&T[i]^Q
.EQN 25 7 5 31
R[i]=i^5*10^-4/(0.15*10^-4*150*10^-4)^Q
.EQN 0 40 5 32
Rs[i]=i^5*10^-4/(0.5*10^-4*150*10^-4)^Q
.EQN 0 41 8 23
Rt[i]=(Rs[i]*R[i])/(Rs[i]+R[i])^Q
.EQN 7 -85 25 68
&1&log(R[i],log(Rs[i],log(Rt[i]{5,13,20,40,1}@1573&273&T[i]^Q
.EQN 23 8 2 26
WRITEPRN(one.dat):Rt[i]^Q
.EQN 0 32 67 13
R[i]=^Q
.EQN 4 -32 2 32
WRITEPRN(temp.dat):T[i-273]^Q
A4 Si Resistivity Model

.MCD 200000 0
.CMD PLOTFORMAT logs=0,0 subdivs=1,1 size=5,15 type=1
.CMD FORMAT rd=d ct=56 im=i et=3 zt=15 pr=3 mass length time charge
.CMD SET ORIGIN 0
.CMD SET TOL 0.000000
.CMD MARGIN 0
.CMD LINELENGTH 78
.CMD SET PRNCOLWIDTH 8
.CMD SET PRNPRECISION 4
.CMD FILENAME temp.dat temp.dat
.CMD FILENAME res.dat res.dat
.CMD FILENAME res1.dat res1.dat
.CMD FILENAME res2.dat res2.dat
.EQN 1 14 1 18
i:0,50;1300^Q
.EQN 0 21 2 15
T[i]=i+273^Q
.EQN 3 -21 3 25
m:((0.98*0.19^2)^33333^Q
.EQN 0 46 6 41
E[j:1.17-4.73*10^-4*T[i]^2/(T[i]+636)]*1.602^Q
.EQN 2 -18 1 9
mo:1^Q
.EQN 3 -28 1 13
mde:m^Q
.EQN 2 0 3 34
mdh:(0.16^1.5+0.49^1.5)^0.66666^Q
.EQN 1 46 2 19
k:1.38066*10^-5^Q
.EQN 4 -46 1 9
Mc:6^Q
.EQN 4 0 8 52
N[i:4.9*10^15*(mde*mdh/mo^2)^0.75*Mc^1.5*e^-E[i/(2*k*T[i])]^Q
.EQN 1 61 3 25
\mu h[i:2.5*10^8*(T[i])^-2.2^Q
.EQN 11 -66 3 35
n13[i:if[N[i]>1*10^13,N[i],1*10^13]^Q
.EQn 0 37 5 30
13[i:1/(\mu h[i]*n13[i]*1.602*10^-19)^Q
.EQN 9 -32 6 35
n15[i:if[N[i]>1*10^15,N[i],1*10^15]^Q
.EQN 0 40 8 32
15[i:1/(\mu h[i]*n15[i]*1.602*10^-19)^Q
.EQN 6 -46 6 35
n17[i:if[N[i]>1*10^17,N[i],1*10^17]^Q
.EQN 0 38 8 32
17[i:1/(\mu h[i]*n17[i]*1.602*10^-19)^Q
.EQN 8 -24 2 32
WRITEPRN(res.dat):log(13[i])^Q
.EQN 3 0 5 33
WRITEPRN(res1.dat):log(15[i])^Q
.EQN 3 0 5 33
WRITEPRN(res2.dat):log(17[i])^Q
.EQN 3 0 2 26
WRITEPRN(temp.dat):T[i]^Q
.EQN 9 -22 25 72
&&log(13[i]),log(15[i]),log(17[i])\{5,8,20,40,1\}@800&0&T[i-273]^Q
.EQN 41 25 2 32
WRITEPRN(temp.dat):T[i-273]^Q
APPENDIX B

PSPICE SOFTWARE PROGRAMS

The programs reproduced here are in ASC Text format. When such programmes are loaded into the PSPICE package with an extension .CIR, they are interpreted by the internal subroutines within the software package.

B1 ESD Characterisation Program

*ESD COAXIAL TRANSIENT MODEL
*A.J. Franklin Jan. 1989
*Positive polarity characteristic curves $R_{load} = 50\Omega$ to $1500\Omega$
Cx 0 1 100pF
Rx 1 2 1500
Lx 2 3 10uH
Cshunt 1 2 0.5pF
Tin 3 0 4 0 Z0=50 TD=7ns
Rp 4 5 1.0
Lp 4 5 5uH
Cp 4 0 1pF
Vm 5 6 0.0
Rload 6 0 1500
Cload 6 0 2pF
Rhp 6 0 10E6
Chp 6 0 3pF
.TRAN Ins 2us 10ps
.IC V(1)=100 V(2)=0 V(3)=0 V(4)=0 V(5)=0 V(6)=0
Cx1 0 8 100pF
Rx1 8 9 1500
Lx1 9 10 10uH
Cshunt1 8 9 0.5pF
Tin1 10 0 11 0 Z0=50 TD=7ns
Rp1 11 12 1.0
Lp1 11 12 5uH
Cp1 11 0 1pF
Vm1 12 13 0.0
Rload1 13 0 500
Cload1 13 0 2pF
Rhp1 13 0 10E6
Chp1 13 0 3pF
B2 EOS Characterisation Programme

*COAXIAL EOS CHARACTERISATION MODEL
*A.J. Franklin Jan 1989
*Positive polarity characteristic curves $R_{\text{load}} = 1500\Omega$
$\text{vpul} 10 0.0$
$R_{\text{pul}} 1250$
$T_{\text{in}} 2030 ZO=50 TD=7\text{ns}$
$R_{p} 341.0$
$L_{p} 345\mu\text{H}$
$C_{p} 301\text{pF}$
$\text{vm} 450.0$
$R_{\text{load}} 50 1500$
$C_{\text{load}} 502\text{pF}$
$R_{\text{hp}} 50 10\text{E}6$
$C_{\text{hp}} 503\text{pF}$
$\text{dc vpul} 0400.5$
$\text{probe}$
$\text{END}$
**B3 GaAs MES Diode DC Characterisation Program**

*GASFET COAXIAL POSITIVE TRANSIENT MODEL
*A.J. Franklin Jan 1989
*Positive polarity DC characteristic curve
Vg 6 0 0.0
Vm 6 7 0.0
D1 7 8 DIO
B1 8 0 0 GAS
D2 0 7 DIO1
Rs 8 0 1E6
.Model DIO D (IS=1E-12 TT=10E-12 EG=1.43 VJ=-0.7 RS=5)
.Model DIO1 D (IS=1E-12 TT=10E-12 BV=5 IBV=1 EG=1.43 VJ=-0.7 RS=11)
.Model GAS GASFET (RD=15 RG=1E12 VTO=-1.7 LAMBDA=0.05 ALPHA=10 BETA=0.01)
.Temp=27
.DC Vg 0 5 0.01
.Print DC v(6,0) i(vm)
.Probe
.End

**B4 GaAs MES Diode ESD Modelling Programe**

*GASFET COAXIAL POSITIVE TRANSIENT MODEL
*A.J. Franklin Jan 1989
*Positive polarity characteristic curves
Cx 1 0 100pF
Lx 2 3 10uH
Rx 1 2 1500
Cshunt 1 2 0.5pF
Tin 3 0 4 0 Z0=50 TD=7ns
Rp 4 5 1.0
Lp 4 5 5uH
Cp 4 0 1pF
Vm 5 6 0.0
D1 6 7 DIO
B1 7 0 0 GAS
D2 0 6 DIO1
Rhp 6 0 10E6
Chp 6 0 3pF
.Model DIO D (IS=1E-7 TT=10E-12 EG=1.43 VJ=-0.7 RS=5)
.Model DIO1 D (IS=1E-7 TT=10E-12 BV=5 IBV=1 EG=1.43 VJ=-0.7 RS=11)
.Model GAS GASFET (RD=15 RG=1E12 VTO=-1.7 LAMBDA=0.05 ALPHA=10 BETA=0.01)
.Temp=27
.IC V(1) = 300 V(2) = 0 V(3) = 0 V(4) = 0 V(5) = 0 V(6) = 0 V(7) = 0
Cx1 8 0 100pF
Lx1 9 10 10uH
Rx1 8 9 1500
Cshunt 1 8 9 0.5pF
Tin1 10 0 11 0 Z0 = 50 TD = 7ns
Rp1 11 12 1.0
Lp1 11 12 5uH
 Cp1 11 0 1pF
Vm1 12 13 0.0
D11 13 14 DIO
B11 14 0 0 GAS
D21 0 13 DIO1
Rhp1 13 0 10E6
Chp1 13 0 3pF
.TC V(8) = 600 V(9) = 0 V(10) = 0 V(11) = 0 V(12) = 0 V(13) = 0 V(14) = 0
Cx2 15 0 100pF
Lx2 16 17 10uH
Rx2 15 16 1500
Cshunt 2 15 16 0.5pF
Tin2 17 0 18 0 Z0 = 50 TD = 7ns
Rp2 18 19 1.0
Lp2 18 19 5uH
Cp2 18 0 1pF
Vm2 19 20 0.0
D12 20 21 DIO
B12 21 0 0 GAS
D22 0 20 DIO1
Rhp2 20 0 10E6
Chp2 20 0 3pF
.TC V(15) = 900 V(16) = 0 V(17) = 0 V(18) = 0 V(19) = 0 V(20) = 0 V(21) = 0
.TRAN 1ns 1.5us 1ns
.PRINT TRAN v(6,0) v(13,0) v(20,0) i(vm) i(vm1) i(vm2)
.PROBE
.END
APPENDIX C

IEEE Control Programs

The waveform capture program has been written in GWBASIC for use on an IBM DOS machine with a National Instruments IEEE card. The C-V program(s) have been written in BBC BASIC for use on the BBC microcomputer with a PROYCON IEEE card and internal GDUMP and WATFORD Electronics ROM.

C1 Waveform Capture Program - GWBASIC

10 CLEAR,60000!: IBINIT1=60000!: IBINIT2=IBINIT1+3: BLOAD "bib.m",IBINIT1
20 CALL IBINIT1(IBFIND, IBTRG, IBCLR, IBPCT, IBISC, IBLOC, IBPPC, IBSE, IBONL, IBRSC, IBRSE, IBRSV, IBPAD, IBSD, IBIST, IBDMA, IBEOS, IBTMO, IBOT, IBDF, IBWRTF, IBTRP)
30 CALL IBINIT2(IBGTS, IBGAC, IBWALT, IBPOKE, IBWRT, IBWRTA, IBCMD, IBCTA, IBRD, IBRDA, IBSTOP, IBPP, IBRS, IBPMDI, IBXTRC, IBRI, IBWRTI, IBRTMA, IBWRTIA, IBSTA%, IBERR%, IBCTNT%)
40 NAM$ = "hpsscope"
50 CALL IBFIND(NAM$, BD%)
60 COLOR 2
70 GOTO 1360
80 CLS
90 PRINT
100 PRINT
110 PRINT
120 PRINT
130 PRINT*" Do You Wish to Recall a Set-Up Configuration?"" 
140 PRINT
150 PRINT
160 PRINT*" IF YES then Input the Set-Up Number" 
170 PRINT
180 PRINT
190 PRINT*" IF NO then Press Space Bar" 
200 PRINT
210 PRINT
220 PRINT
230 PRINT
240 PRINT
250 Q$ = INPUT$(1)
260 IF Q$ = "* " GOTO 310
270 RECALLS = "recall"+Q$
280 CALL IBWRT (BD%, RECALLS)
290 PRINT
300 PRINT* Set-Up ";Q$;" Recalled"
310 CLS
320 PRINT
330 PRINT
340 PRINT
350 PRINT
360 PRINT
370 PRINT
380 PRINT
390 PRINT
400 PRINT
410 PRINT
420 PRINT
430 PRINT" Ready for Waveform Capture?"
440 PRINT
450 CLERS$ = "erase mem 5 mem 6"
460 CALL IBWRT (BD%, CLERS$)
470 FINS$ = "timebase mode single local"
480 CALL IBWRT (BD%, FINS$)
490 Q$ = INPUT$(1)
500 IF Q$ = "y" THEN 530
510 IF Q$ = "n" THEN STOP
520 GOTO 490
530 DATS$ = "acquire type filtered"
540 CALL IBWRT (BD%, DATS$)
550 DIGITISES$ = "dig1,2"
560 CALL IBWRT (BD%, DIGITISES$)
570 CLS
580 COLOR 23
590 PRINT
600 PRINT
610 PRINT
620 PRINT
630 PRINT
640 PRINT
650 PRINT
660 PRINT
670 PRINT
680 PRINT" Trigger Scope"
690 CHECKS$ = "READY?"
700 CALL IBWRT (BD%, CHECKS$)
710 CALL IBRD(BD%,STATUS$)
720 IF VAL(STATUS$) = 255 THEN 740
730 CLS
740 BEEP
750 PRINT
760 PRINT
770 PRINT
780 PRINT
790 PRINT
800 PRINT
810 PRINT
820 PRINT" Data in HP 54111D Storage Buffer"
830 PRINT
840 PRINT
850 PRINT
860 PRINT" Hit Return to Continue"
865 WAIT$ = INKEY(1)
870 GOTO 1360
880 PROT$ = "header off longform off eoi on"
890 CALL IBWRT (BD%, PROT$)
900 FOR I = 5 TO 6
910 IF I = 5 THEN ID$ = "v"
920 IF I = 6 THEN ID$ = "c"
930 IF ID$ = "v" THEN IDENT$ = "voltage.dat"
940 IF ID$ = "c" THEN IDENT$ = "current.dat"
950 CHANNEL$ = STRS(I)
960 TRANS$ = "waveform source memory"+CHANNEL$+" format ascii"
970 CALL IBWRT (BD%, TRANS$)
980 OUPUT$ = "data?"
990 CALL IBWRT (80 %, OUPUT$)
1000 CLS
1010 PRINT" Data Saved in "+DIRECTORY$+" directory"
1020 PRINT
1030 PRINT
1040 PRINT" File name ",IDENT$
1050 SAV$ = DIRECTORY$+IDENT$
1060 CALL IBRDF (BD%, SAV$)
1070 A$ = "xinc?"
1080 FS = DIRECTORY$+ID$+"xinc.dat"
1090 CALL IBWRT (BD%, A$)
1100 CALL IBRDF (BD%, FS)
1110 PRINT
1120 PRINT
1130 A$ = "yinc?"
1140 FS = DIRECTORY$+ID$+"yinc.dat"
1150 CALL IBWRT (BD%, A$)
1160 CALL IBRDF (BD%, FS)
1170 A$ = "xref?"
1180 FS = DIRECTORY$+ID$+"xref.dat"
1190 CALL IBWRT (BD%, A$)
1200 CALL IBRDF (BD%, FS)
1210 A$ = "yref?"
1220 FS = DIRECTORY$+ID$+"yref.dat"
1230 CALL IBWRT (BD%, A$)
1240 CALL IBRDF (BD%, FS)
1250 A$ = "xorg?"
1260 FS = DIRECTORY$+ID$+"xorg.dat"
1270 CALL IBWRT (BD%, A$)
1280 CALL IBRDF (BD%, FS)
1290 A$ = "yorg?"
1300 FS = DIRECTORY$+ID$+"yorg.dat"
1310 CALL IBWRT (BD%, A$)
1320 CALL IBRDF (BD%, FS)
1330 FIN$ = "LOCAL"
1340 CALL IBWRT (BD%, FIN$)
1350 NEXT I
1360 CLS
1370 PRINT
1380 PRINT" HP 54111D Waveform Capture Program 2.3"
1390 PRINT
1400 PRINT" A.J. Franklin May 89"
1410 PRINT
1420 PRINT
1430 PRINT
1440 PRINT" Transfer Data Files from Floppy to MathCad Directory? - Press T"
1450 PRINT
1460 PRINT" Examine Data in MathCad - Press E"
1470 PRINT
1480 PRINT" Save Data on Disc? - Press D"
1490 PRINT
1500 PRINT" Return to GPIB Menu? - Press M"
PRINT Begin Waveform Capture? - Press C
PRINT
PRINT Exit Programme? - Press Q
PRINT
PRINT
Q$ = INPUT$(1)
IF Q$ = "m" THEN SYSTEM
IF Q$ = "c" THEN GOTO 80
IF Q$ = "q" THEN STOP
IF Q$ = "d" THEN 1660
IF Q$ = "t" THEN 1860
IF Q$ = "e" THEN SHELL "mathcad.bat"
IF Q$ ="e" THEN GOTO 1360
GOTO 1570
CLS
PRINT Specify Drive?
PRINT
PRINT Drive C - Input c:
PRINT
PRINT Drive A - Input a:
PRINT
PRINT
INPUT Q$
IF Q$ = "c:" THEN DIRECTORY$ = "c:\mead\"
PRINT
IF Q$ = "a:" THEN PRINT "Subdirectory name";
PRINT
IF Q$ = "a:" THEN INPUT SUB$
BATCH$ = "change.bat "+SUB$
IF Q$ ="a:" THEN SHELL BATCH$
IF Q$ ="a:" THEN DIRECTORY$ = "A:\"+SUB$+"\"
GOTO 880
CLS
SHELL "dir a:/w"
PRINT
PRINT
PRINT
PRINT
PRINT
PRINT
INPUT SELEC$
CLS
SUBDIR$ = "a:\"+SELECT$+"\"
BATCH$ = "trans.bat "+SUBDIR$
SHELL BATCH$
GOTO 1360
C2 C-V Measurement Program - BBC BASIC

10 DIM G$(40)
20 DIM CAP(4)
25 K = 49: GOTO 30
30 MODE 1
40 COLOUR 2
50 CLS: PRINTTAB(17); "MENU"
60 COLOUR 1
70 PRINT: PRINT: PRINT: PRINT" 1. C-V Measurement?"
80 PRINT: PRINT" 2. Display Curve?"
90 PRINT: PRINT" 3. Save File to Disc?"
115 PRINT: PRINT" 4. Curve Processing?"
120 K = INKEY(100)
130 IF K = 49 THEN MODE 0: PROCAPSET: PROCMEAS: PROCSORT: PROCAXIS:
PROCDISPLAY: Y$ = GET$: GOTO 30
140 IF K = 50 THEN PROCFILE: GOTO 30
170 IF K = 52 THEN PROCLOAD1
195 GOTO 120
200 DEF PROCAXIS
210 CLS: F = 1; P = 0.25
220 MOVE 167, 860; P = 0.25
230 DRAW 167, 132; DRAW 1190, 132
240 PRINTTAB (33, 31); "Gate Bias Voltage"
250 A$ = "Capacitance"; F = 1
260 FOR G = 8 TO 18
270 B$ = MID$(A$, F, 1)
280 PRINTTAB(1, G); B$
290 F = F + 1
300 NEXT G
310 PRINTTAB (1, 21); "pF"
320 PRINTTAB(10, 28); "0"
330 PRINTTAB(22, 28); "0.312"
340 PRINTTAB(38, 28); "0.625"
350 PRINTTAB(55, 28); "0.94"
360 PRINTTAB(71, 28); "1.25"
370 FOR T = 25 TO 73 STEP 16
380 PRINTTAB(T, 26); "0"
390 NEXT T
400 ENDPROC
410 DEF PROC DISPLAY
420 Y = 0: REM V = MAX Value of C-V Measurement
430 IF V < 0.01 AND V > 0 THEN V = 0.01
440 IF V < 0.1 AND V > 0 THEN V = 0.1
450 IF V < 1 AND V > 0.1 THEN V = 1
460 IF V < 5 AND V > 1 THEN V = 5
470 IF V < 10 AND V > 5 THEN V = 10
480 IF V < 20 AND V > 10 THEN V = 20
490 IF V < 50 AND V > 20 THEN V = 50
500 IF V < 100 AND V > 50 THEN V = 100
510 IF V < 150 AND V > 100 THEN V = 150
520 IF V < 1000 AND V > 150 THEN V = 1000
530 IF V < 3000 AND V > 1000 THEN V = 3000
540 PLOT 4, 170, 167 + CAP(0) * 720 / V
540 FOR X = 180 to 1155 STEP 25
560 Y = Y + 1
570 DRAW X, 167 + CAP(Y) * 720 / V
580 NEXT X
590 VDU5
600 MOVE -17,178+720:PRINT " 
610 MOVE -17,178+540:PRINT " 
620 MOVE -17,178+360:PRINT " 
630 MOVE -17,178+180:PRINT " 
640 MOVE -17,178+720:PRINTV," -" 
650 MOVE -17,178+540:PRINT(INT(3*V/4*100))/100); -" 
660 MOVE -17,178+360:PRINT(INT(V/2*100)); -" 
670 MOVE -17,178+180:PRINT(INT(V/4*100));/-" 
680 VDU4 
690 ENDPROC 
700 DEFPROCSCREENDUMP 
710 *GDUMP 3 2 1 
720 ENDPROC 
770 DEFPROCLOAD1 
780 *DR.0 
790 CHAIN"DISPLAY" 
800 ENDPROC 
810 DEFPROCFIELD 
820 *DISC 
830 *DR.1 
840 *DIR A 
840 CLS 
850 PRINTTAB(3);" File will be Loaded to Drive 1" 
860 PRINT:PRINT:PRINTTAB(10);"File Name "; 
870 INPUT AS 
890 1=OPENOUTA$ 
900 FOR B=0 TO 40 
910 PRINT#1,CAP(B) 
910 NEXTB 
920 CLOSE#1 
930 ENDPROC 
940 DEFPROCMEOAS 
950 B=0 
960 *SDC7 
970 FORS=0 TO -125 STEP -3.125 
980 ZS="12ROV"+STR$(S/100)+"FIX " 
990 Print #7,ZS 
1000 FOR O=0 TO 20:NEXTQ 
1015 PRINT#10,D4 
1020 FOR O=0 to 2000:NEXTQ 
1030 INPUT#10,D$ 
1040 G5(B)=D$ 
1050 *SDC7 
1060 B=B+1 
1070 NEXTS 
1080 ENDPROC 
1090 DEFPROCCAPSET 
1100 *IEEE 
1110 *REN 
1130 REM SET WAYNE KERR 
1140 PRINT#10,"PF" 
1150 PRINT#10,"FU" 
1160 PRINT#10,"C" 
1170 PRINT#10,"PA" 
1180CLS:PRINTTAB(32,15);"Trim Required?" 
1190 INPUT AS 
1200 IF A$="Y" THEN PRINT#10,"O/";":FOR S=0 TO 2000:NEXTS 
1210 CLS:PRINTTAB(32,15); " READY?";Y$=GET$ 
1220 CLS
C2  C-V Display Program - BBC BASIC

10 DIM CAP(50)
20 DIM CAPA(50)
30 DIM CAPB(50)
40 DIM CAPC(50)
50 DIM CAPD(50)
60 V=0: U=0
70 MODE 1
80 COLOUR 2
90 CLS: PRINTTAB(13); "MAIN MENU"
100 COLOUR 1
110 PRINT: PRINT: PRINT: PRINT: PRINT 1. Download C-V File(s) from Disc?"
120 PRINT: PRINT* 2. Download R-V File(s) from Disc?"
130 PRINT: PRINT* 3. Download I-V File(s) from Disc?"
140 PRINT: PRINT* 4. ScreenDump Curves to Printer?"
150 PRINT: PRINT* 5. Carrier Density Profile?"
160 PRINT: PRINT* 6. C-V Measurement?"
170 PRINT: PRINT* 7. R-V Measurement?"
180 PRINT: PRINT* 7. I-V Measurement?"
190 K=INKEY(100)
200 IF K=49 THEN V=0: N=0: A$="": B$="": C$="": D$="": PROCDOWN: MODE 0:
PROCSORT: Y$=GET$: GOTO 70
210 IF K=50 THEN V=0: N=1: A$="": B$="": C$="": D$="": PROCDOWN: MODE 0:
PROCSORT: Y$=GET$: GOTO 70
220 IF K=51 THEN V=0: A$="": B$="": C$="": D$="": PROCPLT: GOTO 70
230 IF K=52 THEN MODE 0: PROCSORT: PROCTITLE: PROCSRENDUMP: Y$=GET$: GOTO 70
240 IF K=53 THEN PROCLOAD
250 IF K=54 THEN PROCLOAD1
260 IF K=55 THEN PROCLOAD2
270 IF K=56 THEN PROCLOAD3
280 GOTO 190
290 DEFPROC AXIS
300 CLS; F=1; P=0.25
310 MOVE 167,860; P=0.25
320 DRAW 167,132; DRAW 1190,132
330 PRINTTAB(33,31); "Gate Bias Voltage"
340 A$="Capacitance": F=1
350 FOR G=8 TO 18
360 BS=MID$(A$, F, 1)
370 PRINTTAB(1, G); BS

C7
380 F=F+1
390 NEXTG
400 PRINTTAB(1,21);"pF"
410 PRINTTAB(10,28);"0"
420 PRINTTAB(22,28);"-0.312"
430 PRINTTAB(38,28);"-0.625"
440 PRINTTAB(55,28);"-0.94"
450 PRINTTAB(71,28);"-1.25"
460 FOR T=25 TO 73 STEP 16
470 PRINTTAB(T,26);":"
480 NEXTT
490 ENDPROC
500 DEFPROC DISPLAY
510 Y=0:REM V = MAX Value of C-V Measurement
520 IF V<0.00001 AND V>0 THEN V=0.00001
530 IF V<0.00001 AND V>0.00001 THEN V=0.0001
540 IF V<0.001 AND V>0.001 THEN V=0.001
550 IF V>0.01 AND V>0.01 THEN V=0.01
560 IF V<0.1 AND V>0.1 THEN V=0.1
570 IF V<0.5 AND V>0.1 THEN V=0.5
580 IF V<1 AND V>0.1 THEN V=1
590 IF V<5 AND V>1 THEN V=5
600 IF V<10 AND V>5 THEN V=10
610 IF V<20 AND V>10 THEN V=20
620 IF V<50 AND V>20 THEN V=50
630 IF V<75 AND V>50 THEN V=75
640 IF V<100 AND V>50 THEN V=100
650 IF V<150 AND V>100 THEN V=150
660 IF V<200 AND V>150 THEN V=200
670 IF V<300 AND V>150 THEN V=300
680 PLOT 4,170,167+CAP(0)*720/V
690 FORX=180 to 1155 STEP 25
700 Y=Y+1
710 DRAW X,167+CAP(Y)*720/V
720 NEXTX
730 VDU5
740 MOVE -17,178+720:PRINT* *
750 MOVE -17,178+540:PRINT* *
760 MOVE -17,178+360:PRINT* *
770 MOVE -17,178+180:PRINT* *
780 MOVE -17,178+720:PRINTV,* -*
790 MOVE -17,178+540:PRINT(INT(3*V/4*100))/100;" -*
800 MOVE -17,178+360:PRINT(INT(V/2*100))/100;" -*
810 MOVE -17,178+180:PRINT(INT(V/4*100))/100;" -*
820 VDU4
830 ENDPROC
840 DEFPROCS CREE NDUMP
850 *GDUMP 3 2 1
860 ENDPROC
870 DEFPROCL OAD
880 *DR.0
890 CHAIN"DATAM"
900 ENDPROC
910 DEFPROCL OAD1
920 *DR.0
930 CHAIN"CV-MEAS"
940 ENDPROC
950 DEFPROCL OAD1
960 *DR.0
970 CHAIN"LN-FOR"

C 8
ENDPROC
DEFPROCDOWN
1000 "DISC
1010 U=0:CLS
1020 "DR.1
1030 IF K=49:*DIR A
1040 IF K=50:*DIR B
1050 IF K=51:*DIR C
1060 "CAT
1070 PRINT:PRINT:PRINT"File(s) will be Downloaded from Drive 1"
1080 PRINT:PRINT:PRINT"File Name(s)"
1090 INPUT AS,BS,CS,DS
1100 IF LEN(AS)>0 AND U=0 THEN Z$=AS:GOTO1150
1110 IF LEN(BS)>0 AND U=1 THEN Z$=BS:GOTO1150
1120 IF LEN(CS)>0 AND U=2 THEN Z$=CS:GOTO1150
1130 IF LEN(DS)>0 AND U=3 THEN Z$=DS:GOTO1150
1140 GOTO1260
1150 I=OPENINZ$
1160 FOR B=0 TO 40
1170 INPUT #I,A
1180 IF Z$=AS THEN CAPA(B)=A
1190 IF Z$=BS THEN CAPB(B)=A
1200 IF Z$=CS THEN CAPC(B)=A
1210 IF Z$=DS THEN CAPD(B)=A
1220 NEXTB
1230 CLOSE#I
1240 U=U+1
1250 GOTO 1100
1260 ENDPROC
1270 DEFPROCSORT
1280 U=0:PROCAXIS
1270 FOR Z=0 TO 40
1280 IF CAPA(Z)>V THEN V=CAPA(Z)
1290 IF CAPB(Z)>V THEN V=CAPB(Z)
1300 IF CAPC(Z)>V THEN V=CAPC(Z)
1310 IF CAPD(Z)>V THEN V=CAPD(Z)
1320 NEXTZ
1330 IF LEN(AS)>0 AND U=0:FOR Z=0 TO 40:CAP(Z)=CAPA(Z):NEXTZ:GOTO 1380
1340 IF LEN(BS)>0 AND U=1:FOR Z=0 TO 40:CAP(Z)=CAPB(Z):NEXTZ:GOTO 1380
1350 IF LEN(CS)>0 AND U=2:FOR Z=0 TO 40:CAP(Z)=CAPC(Z):NEXTZ:GOTO 1380
1360 IF LEN(DS)>0 AND U=3:FOR Z=0 TO 40:CAP(Z)=CAPD(Z):NEXTZ:GOTO 1380
1370 GOTO 1410
1380 U=U+1
1390 PROCDISPLAY
1400 GOTO 1330
1410 ENDPROC
1420 DEFPROCTITLE
1430 PRINTTAB(15,4);"TITLE - Key in Here ";
1440 INPUT IS$
1450 PRINTTAB(15,4);"*
1460 PRINTTAB(20,4)IS$
1470 ENDPROC
1480 DEFPROCLOAD2
1490 "DR.0
1500 CHAIN"RV-MEAS"
1510 ENDPROC
1520 "DISC
1530 "DR.0
1540 CHAIN"PLOT"
1550 ENDPROC

C 9
APPENDIX D

ABSTRACTS FROM REPORTS

Report No. 1 - Failure in GaAs Devices
(Loughborough University - 1985)

GaAs component reliability has been studied and a foundation of knowledge has been established concerning the possible failure mechanisms of GaAs low-noise and power metal-semiconductor field effect transistors (MESFETs).

Experimental work has been carried out to assess the susceptibility of GaAs depletion-mode MESFETs to electrostatic discharge pulses. The results indicate different failure mechanisms operate within the devices according to the polarity of the discharge pulse. In both polarity cases, lower voltages will produce "walking wounded" devices which will operate normally but will show an increase in gate leakage current and a decrease in transconductance when analysed.

Other experimental work has established a base for further work into accelerated lifetesting of D-type and E-type MESFETs, and for the generation of crystal dislocations by ohmic alloying and contact bonding.

Report No. 2 - Failure in GaAs Devices
(Loughborough University - 1987)

Further studies of the degradation and burnout properties of GaAs D-MESFETS has been completed.

Detailed electrical parameter changes of FET and diode structures have been studied. Five modes of degradation have been found related to changes the drain current $I_{ds}$ vs drain voltage $V_{ds}$, subsequent to ESD pulses. DC
parametric variations in $I_{dss}$, $g_m$, $R_{on}$, $V_p$, and $R_s$ have been studied at high (100°C) and ambient (25°C) temperatures.

Studies have shown that a failure site can be linked to the DC biased (gate-ohmic) diode white light emission point in the channel region in some cases.

SAM micrographs reveal the possible existence of subsurface metallic diffusion of the alloyed ohmic contacts creating high field regions when a device is DC biased or pulsed.

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**Report No. 3 - Failure in GaAs Devices**

(Loughborough University - 1989)

This report outlines the studies on the contract titled "Failure in GaAs Devices", undertaken during the period April 1987 until February 1989.

During this period the following areas have been addressed:

1) The purchase and utilisation of equipments in order to set-up a "state of the art" pulsing and measurement system.

2) Analysis of existing thermal breakdown models for semiconductor devices, and the device and circuit parameters which control thermal breakdown.

3) Development of a new thermal model which could be used for EOS thermal breakdown in semiconductor devices.

4) Initial experimental studies relating to the thermal models, in order to verify their validity in GaAs MES structures.

5) Utilisation of the computer circuit modelling algorithm PSPICE in order to fully characterise the electrostatic discharge pulsing system and develop a simple device circuit model.

The study has reached a stage where a model has been defined for thermal runaway in MES structures and is in the process of being tested. The initial results have shown that the models are more applicable to the structures
under investigation than previous models.

*Report No. 4 - Failure in GaAs Devices*

(Loughborough University - 1990)

Over the past 5 years, a study has been carried out at Loughborough University into the electrical overstress failure mechanisms in GaAs MESFET and MES diode structures. This is the final report for the period April 1989 - December 1989 of the study undertaken for the MOD contract D/ER1/9/4/2170/115 (DCVD), "Failure in GaAs Devices".

This report contains the full derivation of the EOS and ESD thermal breakdown models. The EOS model can be used to predict the $P_f$ vs $t_f$ relationship over the full time domain. The ESD model predicts the minimum ESD charge voltage, derived from the "human body model" circuit, which can induce thermal failure in a semiconductor device. Both of these models have been investigated using GaAs MES structures. Within the limitations of the experimental system the results compare favourably with the predicted values.
APPENDIX E

ABSTRACTS FROM PUBLISHED PAPERS

The following abstracts are taken form the six papers published, or in the process of being published, based on the study undertaken in this thesis.

A Comparison between GaAs MESFET and Si MOSFET ESD behaviour
(Presented at the ERA seminar on Electrostatic Damage in Electronics, Regent Crest Hotel, London, 1986)

Work is in progress at Loughborough University to investigate and compare ESD sensitivity of GaAs D-MESFETs and unprotected enhancement mode NMOS structures.

The work to date has revealed that NMOS structures can be severely degraded with an ESD pulse above 200V as compared with 200V for GaAs MESFETs. It has also been shown that both NMOS and GaAs structures are polarity sensitive.

The breakdown of the oxide for NMOS devices can be explained by impact ionisation. The effect of the Schottky barrier to explain the polarity behaviour is discussed.

A Comparison between GaAs MESFET and Si MOSFET ESD behaviour
(Published in Elec. Comp. Sci. and Tech., 12, pp. 201-211, 1987)

Work is in hand at Loughborough University to investigate and compare ESD sensitivity of GaAs D-MESFETs and unprotected enhancement mode NMOS structures.

The work to date has shown that GaAs MESFET structures can be severely degraded with ESD pulses above 600V as compared with 200V for Si
MOS. It has also been shown that both GaAs and NMOS structures are polarity sensitive.

The behaviour of the Schottky barrier is used to explain the polarity behaviour in GaAs MESFETs. The breakdown of the oxide in NMOS devices can be explained by impact ionisation.

**Thermal Failure in Semiconductor Devices**

(Accepted for publication in Solid State Electronics, 1990)

A first principles approach to the problem of thermal breakdown in semiconductor devices is developed using Green's function formalism.

The problem of thermal runaway at a defect of arbitrary geometry, subject to an arbitrary power profile, is considered.

A solution is presented for the specific case of a rectangular parallelepiped shaped defect, subject to constant input power. It is expected that this geometry will model the defect in many semiconductor devices more accurately than the defect geometries used in the past. Unlike previous work, this allows all three dimensions of the defect to take on the full range of values.

The theory developed here provides a natural framework for the explanation of results previously reported in the literature. It is shown that there are four time domains and not three as previously thought, and these exist for all shapes of defect. Thus, it is wrong to conclude that a pulse power/time to failure dependence of the form $P_f \propto t_r^{\gamma}$ necessarily implies a roughly two dimensional defect.

Several relationships are found to exist within the model which allow estimates to be made of the defect dimensions and failure temperature.

Experimental data drawn from the literature, produce $P_f$ vs $t_r$ profiles similar to those indicated by the theory.
Thermal Breakdown in GaAs MES Diodes
(Accepted for publication in Solid State Electronics, 1990)

Thermal breakdown analysis of planar GaAs metal-semiconductor diodes is presented and three models relating failure power \( (P_f) \) to corresponding failure times \( (t_f) \) are compared. The standard Wunsch & Bell model, a modified form of the Tasca model, and a three dimensional model (developed by the authors) are fitted to experimental data. The results indicate that, within given failure time domains, GaAs structures of this kind follow the same general patterns, \( P_f \alpha t_f^{-\eta} \), as those previously reported for silicon semiconductor devices. There is one exception. In the time domain roughly between 1 and 20\( \mu \)s, the failure power is given by \( P_f \alpha 1/\log_e (t_f) \).

Analytic expressions are used to extract three "defect" dimensions from forward bias experimental data. These "defect" dimensions are discussed with reference to the device dimensions and the ambient temperature. Two distinct visible and electrical failure modes have been observed and these are linked to the channel conductance changing subsequent to an applied pulse.

Electrostatic Thermal Failure in Semiconductor Devices
(Submitted for publication in IEEE Transactions on Electron Devices, 1990)

The problem of thresholding in ESD induced thermal failure is considered by the thermal convolution integral technique. It is shown that a common assumption that threshold breakdown occurs after five time constants is unjustified and that the simple "average power" method for assessing threshold parameters is, consequently, invalid.

New expressions for the threshold parameters are presented here which retain the simplicity of the "average power" method, yet represent only a small sacrifice of the accuracy (typically 5%) of more complex methods.

In addition, the relaxation of the constraints of a pure Wunsch-Bell damage profile and of an exponentially decaying current pulse are considered.
Many models for ESD thermal failure in semiconductor diodes picture the device as a perfect diode in series with a bulk resistor. Recent work by the authors using this generic model predicts the existence of an allowed "window" of possible failure times. This window provides upper and lower limits for the threshold failure time. The model also predicts simple analytic approximations for the threshold parameters, peak current, ESD voltage and failure time, based on the "human body" ESD circuit. An experimental analysis of this model, based on forward biased GaAs diodes, is presented. The results obtained show very good agreement with the theory.