Microprocessor controlled novel 4-quadrant DC-DC converter

This item was submitted to Loughborough University's Institutional Repository by the/an author.

Additional Information:

- A Doctoral Thesis. Submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy of Loughborough University.

Metadata Record: https://dspace.lboro.ac.uk/2134/19477

Publisher: © Aidong Xu

Rights: This work is made available according to the conditions of the Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International (CC BY-NC-ND 4.0) licence. Full details of this licence are available at: https://creativecommons.org/licenses/by-nc-nd/4.0/

Please cite the published version.
<table>
<thead>
<tr>
<th>VOL. NO.</th>
<th>CLASS MARK</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LOUGHBOROUGH UNIVERSITY OF TECHNOLOGY LIBRARY**

**AUTHOR/FILING TITLE**

- **Xu, A**

**ACCESSION/COPY NO.**

- **036000311**

**VOL. NO.**

- **LUNA COPY**
  - **1 JUL 1994**
  - **1 MAY 1994**

- **30 NOV 1992**
  - **2 JUL 1993**
  - **5 FEB 1993**

- **1 MAY 1993**
  - **2 JUL 1993**
  - **3-0-JUN 1995**

- **1 MAY 1993**
  - **2 JUL 1993**
  - **3-0-JUN 1995**

- **1 MAY 1993**
  - **2 JUL 1993**
  - **3-0-JUN 1995**

**CLASS MARK**

- **036000311 7**
AUTHOR'S DECLARATION: I AGREE THE FOLLOWING CONDITIONS:

OPEN access work shall be made available (in the University and externally) and reproduced as necessary at the discretion of the University Librarian or Head of Department. It may also be copied by the British Library in microfilm or other form for supply to requesting libraries or individuals, subject to an indication of intended use for non-publishing purposes in the following form, placed on the copy and on any covering document or label. The statement itself shall apply to ALL copies:

THIS COPY HAS BEEN SUPPLIED FOR NON-PUBLISHING PURPOSES ON THE UNDERSTANDING THAT IT IS COPYRIGHT MATERIAL AND THAT NO QUOTATION NOR ANY INFORMATION DERIVED FROM THE THESIS MAY APPEAR IN PUBLISHED FORM WITHOUT PRIOR WRITTEN CONSENT BY OR VIA THE UNIVERSITY LIBRARIAN.

RESTRICTED / CONFIDENTIAL WORK: All access and any photocopying shall be strictly subject to the written permission from the University Head of Department and any external sponsor if any.

Author's signature ___________________________ Date 14/1/92

USER'S DECLARATION for signature during any Moratorium period (Not Open work):

I UNDERTAKE TO UPHOLD THE ABOVE CONDITIONS:

Date Name(Capitals) Signature Address

(Continue overleaf if necessary)
To my Wife

JIANJIN SHI
MICROPROCESSOR-CONTROLLED
NOVEL 4-QUADRANT DC-DC
CONVERTER

by

AIDONG XU

A Doctoral Thesis
Submitted in partial fulfilment of
the requirements for the award of
the Degree of Doctor of Philosophy
of the Loughborough University of Technology

December 1991

Supervisor: Mr. J G Kettleborough

Department of Electronic and Electrical Engineering
Loughborough University of Technology
Loughborough - Leics. - England

© by AIDONG XU
SYNOPSIS

The thesis describes a novel 4-quadrant DC-DC converter, supplied by a 28V DC voltage source, with an output voltage which may be continuously varied between +180V and -180V DC.

A prototype 1.2kW DC-DC converter was designed and built, with emphasis given to the optimization of both the converter size and efficiency. This was achieved by means of a computer-based simulation study, which determined the optimal switching frequency and the size of the inductors and capacitors while maintaining a high unit efficiency. Mos-Gated Bimos switches, which feature the advantages of both mosfets and bipolar transistors, were developed to achieve high switching speed during high power operation.

A digital-controlled DC servo system based on a 16-bit Intel 8086 microprocessor was designed, to provide both motor speed and position control. Speed and position detection circuits and the structure and the interfacing arrangement of the microprocessor system were designed and constructed. Several control algorithms were developed, including PID Control Algorithm and Current-Limit Control Algorithm. Based on open loop transfer function of the system, derived through mathematical modelling using the State-Space Averaging Method, the constants for the control algorithms were obtained to meet the dynamic performance specified for the system.

Computer simulation was carried out to assist with the design of the converter and the control system.
It is expected that drives into which the novel converter is incorporated will find many applications in situations where accurate positional control is required, particularly in battery-operated DC-servo system, such as satellite system, robots and some military vehicles.
ACKNOWLEDGEMENT

I would like to express my thanks to Mr. J G kettleborough for his valuable guidance and encouragement throughout the years of my research.

I would like also to express my deepest gratitude to Professor I R Smith for reading many drafts and making constructive comments that improved the overall presentation.

Many thanks go to my friends and colleagues in the Electronic and Electrical Engineering Department of Loughborough University for many useful discussions held.

Finally I would like to extend my acknowledgement to British Council and the government of P R China for their financial support.
LIST OF PRINCIPAL SYMBOLS

B  Flux density
C  Capacitance
\( \delta \)  Variation in duty cycle
\( d \)  Dynamic duty cycle
\( d' = 1-d \)
D  Switching duty cycle at steady state.
\( D' = 1-D \)
\( E_a \)  Armature applied voltage
\( E_b \)  Armature generated back emf
\( E_f \)  Motor field applied voltage
f  Switching frequency
g  Air gap of the inductor
h  Integration step size
\( I_{L1}, I_{L2} \)  Inductor current
\( I_a \)  Armature current
\( I_f \)  Field current
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_o$</td>
<td>Output current</td>
</tr>
<tr>
<td>$I_m$</td>
<td>Inductor peak current</td>
</tr>
<tr>
<td>$J$</td>
<td>System moment of inertia</td>
</tr>
<tr>
<td>$K_a$</td>
<td>Torque constant of motor</td>
</tr>
<tr>
<td>$K_d$</td>
<td>Derivative controller constant</td>
</tr>
<tr>
<td>$K_f$, $F$</td>
<td>Viscous friction coefficient of the motor</td>
</tr>
<tr>
<td>$K_i$</td>
<td>Integral controller constant</td>
</tr>
<tr>
<td>$K_p$</td>
<td>Proportional controller constant</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance</td>
</tr>
<tr>
<td>$L_a$</td>
<td>Armature self inductance</td>
</tr>
<tr>
<td>$M_a$</td>
<td>Acceleration torque</td>
</tr>
<tr>
<td>$M_e$</td>
<td>Electromagnetic torque</td>
</tr>
<tr>
<td>$M_L$</td>
<td>Load torque</td>
</tr>
<tr>
<td>$n$</td>
<td>Number of sampling interval</td>
</tr>
<tr>
<td>$P_{con}$</td>
<td>The conduction loss of transistors</td>
</tr>
<tr>
<td>$P_{swon}$</td>
<td>The switch-on loss of transistors</td>
</tr>
<tr>
<td>$P_{swf}$</td>
<td>The switch-off loss of transistors</td>
</tr>
<tr>
<td>$P_{total}$</td>
<td>The total switching loss</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>$R_1$</td>
<td>Parasitic resistance</td>
</tr>
<tr>
<td>$R_a$</td>
<td>Armature circuit resistance</td>
</tr>
<tr>
<td>$s$</td>
<td>Laplace transform</td>
</tr>
<tr>
<td>$S_1-S_4$</td>
<td>The converter switches</td>
</tr>
<tr>
<td>$T$</td>
<td>Converter Switching period</td>
</tr>
<tr>
<td>$t_1$</td>
<td>ON time interval of the switch</td>
</tr>
<tr>
<td>$t_2$</td>
<td>OFF time interval of the switch</td>
</tr>
<tr>
<td>$t$</td>
<td>Time</td>
</tr>
<tr>
<td>$t_{swon}$</td>
<td>The switch-on time of transistors</td>
</tr>
<tr>
<td>$t_{swf}$</td>
<td>The switch-off time of transistors</td>
</tr>
<tr>
<td>$V_{c1}, V_{c2}, V_{c3}$</td>
<td>Voltage across capacitor</td>
</tr>
<tr>
<td>$V_L$</td>
<td>Voltage across inductor</td>
</tr>
<tr>
<td>$V_o$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$V_s$</td>
<td>Voltage source</td>
</tr>
<tr>
<td>$X_n$</td>
<td>$n$th sample of $X$</td>
</tr>
<tr>
<td>$Y_n$</td>
<td>$n$th sample of $Y$</td>
</tr>
<tr>
<td>$\theta_r$</td>
<td>Required motor position</td>
</tr>
<tr>
<td>$\theta_n$</td>
<td>Motor position at $n$th sampling instant</td>
</tr>
</tbody>
</table>
\( \omega \)  
Angular speed of the motor

\( \omega_c \)  
Cut-off frequency

\( \omega_n \)  
Motor speed at \( n \)th sampling instant

\( \omega_r \)  
Required motor speed

\( \phi \)  
Armature flux
# Table of Contents

CHAPTER 1 INTRODUCTION ............................................. 1

CHAPTER 2 DC DRIVES .................................................. 6
  2.1 DC MOTOR SPEED CONTROL ........................................ 6
  2.1.1 FIELD CURRENT CONTROL ..................................... 7
  2.1.2 ARMATURE RESISTANCE CONTROL .............................. 8
  2.1.3 ARMATURE VOLTAGE CONTROL ................................ 8
  2.2 ELECTRICAL BRAKING ............................................. 8
     2.2.1 REGENERATIVE BRAKING ................................... 9
  2.3 SOLID-STATE DRIVES ............................................ 9
     2.3.1 AC TO DC CONVERTERS .................................... 10
        2.3.1.1 PHASE CONTROL ..................................... 11
        2.3.1.2 INTEGRAL CYCLE CONTROL .......................... 12
     2.3.2 DC-TO-DC CONVERSION .................................. 12
        2.3.2.1 INVERTER/RECTIFIER SCHEME ......................... 12
        2.3.2.2 DC CHOPPERS ....................................... 12
        2.3.2.3 DC-TO-DC CONVERTERS .............................. 13

CHAPTER 3 DC-TO-DC CONVERTER ..................................... 16
  3.1 BUCK CONVERTER .............................................. 16
  3.2 BOOST CONVERTER ............................................. 20
     3.2.1 BOOST CONVERTER OPERATION .............................. 20
     3.2.2 LARGE-SIGNAL STEADY-STATE CHARACTERISATION
        OF THE BOOST CONVERTER ................................ 20
     3.2.3 BIDIRECTION BOOST CONVERTER .......................... 22
  3.3 BUCK/BOOST CONVERTER ........................................ 23
  3.4 4-QUADRANT DC-to-DC CONVERTER .............................. 24
     3.4.1 BASIC PRINCIPLE ....................................... 24
     3.4.2 LARGE SIGNAL STEADY-STATE CHARACTERISATION
        .................................................................. 25

CHAPTER 4 MODELLING AND ANALYSIS OF DC-TO-DC CONVERTER .... 42
  4.1 STATE-SPACE-AVERAGING METHOD ................................ 42
  4.2 MODELLING PROCEDURE .......................................... 43
  4.3 MODELLING OF A BOOST CONVERTER ............................. 44
     4.3.1 STEADY-STATE CONDITION ................................ 47
     4.3.2 DYNAMIC CONDITION ..................................... 47
  4.4 MODEL FOR THE NOVEL 4-QUADRANT CONVERTER ............... 51
  4.5 EQUIVALENT CIRCUIT MODEL FOR A BOOST CONVERTER ....... 53
     4.6 DISCUSSION .................................................. 55
        4.6.1 FIRST-ORDER RIGHT HALF-PLANE ZERO .................. 55
        4.6.2 INSIGHT INTO THE MATRICES $A_1$, $A_2$, $B_1$, $B_2$,
            $C_1$, $C_2$ ............................................. 56

CHAPTER 5 SIMULATION .................................................. 62
  5.1 4TH-ORDER RUNGE-KUTTA NUMERICAL INTEGRATION
      METHOD ....................................................... 62
  5.2 BOOST CONVERTER SIMULATION ................................ 64
     5.2.1 PARAMETER DETERMINATION .............................. 64
     5.2.2 SYSTEM EQUATIONS ...................................... 66
5.2.3 PROGRAM DESCRIPTION AND SIMULATION RESULTS ............................................. 67
5.3 SIMULATION OF A 4-QUADRANT DC/DC CONVERTER ........................................ 68
  5.3.1 OPEN-LOOP PERFORMANCE ............................................................................. 68
    5.3.1.1 PARAMETER DETERMINATION ................................................................. 68
    5.3.1.2 BASIC EQUATIONS .................................................................................. 69
    5.3.1.3 RESULTS ............................................................................................... 70
  5.3.2 CLOSED-LOOP 4-QUADRANT CONVERTER-DC MOTOR DRIVE ............................. 70
      5.3.2.1 SYSTEM EQUATIONS ........................................................................... 71
      5.3.2.2 CLOSED-LOOP EQUATIONS ................................................................ 73
      5.3.2.3 PROGRAM DESCRIPTION AND RESULTS ............................................. 73

CHAPTER 6 POWER CIRCUIT DESIGN ................................................................. 92
  6.1 SWITCH DESIGN ............................................................................................. 92
    6.1.1 CHARACTERISTICS OF POWER MOSFET AND BIPOLAR TRANSISTOR .......... 93
      6.1.1.1 ADVANTAGES OF BIPOLAR TRANSISTORS ........................................... 93
      6.1.1.2 DISADVANTAGES OF BIPOLAR TRANSISTORS ....................................... 94
      6.1.1.3 ADVANTAGES OF POWER MOSFETS .................................................... 95
      6.1.1.4 DISADVANTAGES OF POWER MOSFETS ............................................ 96
    6.1.2 MOS-GATED BIMOS TRANSISTOR ............................................................... 96
      6.1.2.1 SWITCH CONFIGURATION .................................................................... 96
      6.1.2.2 ADVANTAGES OF THE MOS-GATED BIPOLAR
             POWER TRANSISTOR .............................................................................. 97
      6.1.2.3 PRACTICAL CONSIDERATION ............................................................. 98
  6.2 OPTIMUM FREQUENCY .................................................................................. 99
    6.2.1 INDUCTANCE AND CAPACITANCE CALCULATIONS .................................. 100
    6.2.2 POWER LOSSES ...................................................................................... 101
      6.2.2.1 SWITCHING LOSSES ......................................................................... 101
      6.2.2.2 INDUCTOR WINDING LOSSES ............................................................. 102
      6.2.2.3 DIODE LOSS ...................................................................................... 103
      6.2.2.4 Efficiency And Component Optimization ............................................ 104
  6.3 INDUCTOR DESIGN ....................................................................................... 104
    6.3.1 CORE SELECTION ...................................................................................... 105
    6.3.2 INDUCTOR CALCULATIONS ....................................................................... 105
    6.3.3 FLUX FRINGING ....................................................................................... 107
  6.4 HEATSINKS ................................................................................................. 108
    6.4.1 SAFE OPERATION AREA .......................................................................... 108
    6.4.2 SWITCH POWER LOSSES ........................................................................ 110
    6.4.3 HEATSINK DESIGN .................................................................................. 110
  6.5 DIODES AND CAPACITORS .......................................................................... 112
    6.5.1 DIODES ................................................................................................... 112
    6.5.2 CAPACITOR .............................................................................................. 113
  6.6 PROTECTION CIRCUIT DESIGN ..................................................................... 114
    6.6.1 SNUBBER CIRCUIT DESIGN ..................................................................... 115
    6.6.2 HIGH-SPEED CLAMPING DEVICES ......................................................... 116
    6.6.3 RINGING EFFECT ..................................................................................... 116
    6.6.4 CIRCUIT LAYOUT ..................................................................................... 117

CHAPTER 7 DRIVE CIRCUIT DESIGN ................................................................. 135
  7.1 PWM SIGNAL GENERATOR ........................................................................... 135
  7.2 ISOLATOR .................................................................................................... 135
    7.2.1 ISOLATION TRANSFORMER ..................................................................... 136
    7.2.2 OPTO-COUPLER ..................................................................................... 136
9.2.2 DRIVE SYSTEM RESPONSE WITH CLOSED-LOOP
CONTROL ........................................ 231
9.2.2.1 SYSTEM RESPONSE TO SPEED DEMAND ..... 231
9.2.2.2 SYSTEM RESPONSE TO POSITION DEMAND .... 233
9.2.2.3 SYSTEM RESPONSE TO LOAD VARIATION .... 233

CHAPTER 10 CONCLUSIONS .............................. 256

REFERENCE.................................................. 260

BIBLIOGRAPHY............................................. 263

APPENDIX I SWITCH POWER LOSSES ......................... 266

APPENDIX II FLUX FRINGING EFFECT ......................... 268

APPENDIX III CALCULATION OF VOLTAGE GAIN IN THE DISCONTINUOUS MODE ........................................ 269

APPENDIX IV PUBLISHED WORK .............................. 273
CHAPTER 1 INTRODUCTION

In the 1960s, the demands of the space program led to the development of highly reliable, efficient and lightweight electrical power systems for spacecraft. As a consequence of the limited availability of energy, engineers found innovative solutions for the necessary power processing and management, in which bulky dissipative methods were replaced by more efficient and space-saving techniques. A number of new power electronics techniques evolved, using switched-mode power processing in conjunction with modern power semiconductors.

DC-to-DC converters offer high efficiency and performance for small size and weight. They provide a natural interface with direct energy sources, such as solar cells and thermo-electric generators. An essential feature of efficient power processing is the use of semiconductors in a switching mode to achieve low losses, while controlling the transfer of energy from source to load through the use of pulse-width-modulation or resonant techniques. Inductive and capacitive energy storage elements are used to smooth the flow of energy, while again keeping losses to a low level. As the switching frequency increases, the size of both the magnetic and capacitive elements decrease almost in direct proportion. Due to their superior performance, high efficiency, small size and weight and relatively low cost, switched-mode DC-to-DC converters are displacing conventional linear power converters even at very low power levels.

Considerable literature on switched-mode converters has appeared in the past decade and, particularly in the area of power supplies and battery-operated equipment, industrial applications have been expanding rapidly. Unfortunately, most circuit designs are confined to low voltage and power
levels and to single-quadrant operation. The H-bridge chopper is the only converter suitable for the 4-quadrant control of high-power variable-speed DC drives, and it provides only step-down conversion.

This thesis investigates a novel high-power buck/boost 4-quadrant DC-to-DC converter, which exhibits the advantages of existing modern switched-mode DC-to-DC converters and is capable of both step-up and step-down conversion. A 1.2kW prototype converter supplied from a 28V battery and with an output voltage continuously variable between -180V and +180V is designed and constructed. The new converter is ideal for battery-operated servo drive systems, such as satellite power supplies, aerospace, robots and military vehicles, where a low-voltage battery supply is provided and a high DC voltage may be required to drive a DC servo motor.

To reduce physically the size of the converter a high switching frequency is required, and the recent development of the power mosfet makes high-power switching rates possible. The combination of a power mosfet and a power bipolar transistor, known as a bimos switch, offers particularly attractive properties. The power handling capability of the transistor is higher than that of the mosfet, while the switching rate of the mosfet is higher than that of the transistor. The bimos switch can thus work with the power rating of a bipolar transistor, while switching at the frequency of a mosfet.

Microprocessors have played an important part in many modern developments in variable-speed drives. They can be utilised to trigger power-switching devices according to an established switching strategy, and to perform complicated control tasks by executing digital algorithms stored in their memory. As a result of this, sophisticated control techniques are now feasible.
Analogue control systems are well established, and many of their techniques have been utilised in digital control schemes. In general, a variable-speed motor control scheme will contain both outer speed feedback loop and inner current feedback loops. In some cases a position feedback loop is also included. Information on the motor speed and position may be obtained from a digital tachometer and applied directly to a digital controller. However, information on the motor armature current requires an analogue-to-digital converter in the current loop, which inevitably increases the hardware complexity.

The microprocessor-based DC drive described in this thesis used the novel DC-to-DC converter to provide armature-voltage control of a separately-excited DC motor. Although the drive is expected to find a wide range of industrial applications, attention is focused on applications where the accurate control of position is a prime requirement. Both motor speed and position control are achieved entirely by digital techniques, and the scheme described eliminates the need for the analogue-to-digital converter necessary in an inner current-feedback loop. Both theoretical and practical closed-loop operations are investigated and different control strategies are used.

The equivalent circuit of a separately-excited DC motor is presented in chapter 2 of the thesis, with the corresponding motor performance equations being derived. The chapter also contains an overview of the operating principles of various types of solid-state power converter and considers their application to DC motor control.

Chapter 3 introduces three basic converters and describes their operation. The novel 4-quadrant converter is then fully investigated and analysed. The analysis and mathematical modelling of DC-to-DC converters, which leads to a
transfer function for the 4-quadrant converter, is presented in chapter 4. Since the converter is essentially a non-linear circuit, the powerful state-space averaging method was used in the modelling process.

Chapter 5 presents computer simulations for both a boost converter and the novel 4-quadrant DC-to-DC converter. The variation of current and voltage gain for the two converters with different switching duty cycles is illustrated. A 2-loop(speed and current) DC servo system fed by the novel converter was simulated and the results obtained from the simulations were used as a guide in designing both the power circuit and the control structure for the actual drive.

The design of the power circuit is presented in chapter 6. An optimal switching frequency which minimises the size of the circuit inductors and capacitors, while maintaining a high unit efficiency, was determined by computer simulation and, on this basis, a 40kHz 1.2kW 28V battery supplied converter was constructed. Several circuit protection measures are also discussed in this chapter.

Chapter 7 examines the drive requirements for mosfets. To meet the requirements of a large duty cycle, several methods of isolation between the power and control circuits were investigated, with an optocoupler finally being chosen on the basis of its reliable and superior performance.

Digital control structures, which include speed, position and current control, are presented in chapter 8. An optimized digital PID controller was developed using the Engineering Design Method and implemented using an 8086 microprocessor. Circuits for measuring the motor speed and position and the interface arrangements between the
speed/position demand and the controller are discussed. The control software written in 8086 Assembly language is also explained in this chapter.

Chapter 9 presents practical results from a prototype converter which are compared with the theoretically predicted results obtained in the previous chapters.

A paper entitled "4-Quadrant DC/DC Chopper", which was published in the IEEE PESC Record, 1989, is included as Appendix IV.
CHAPTER 2 DC DRIVES

DC motors are widely used in industrial applications, due to the ease by which their speed may be adjusted and their superior speed-torque characteristics. Speed variation may be achieved by several methods, which are outlined below.

2.1 DC MOTOR SPEED CONTROL

The equivalent circuit of a separately-excited motor is shown in Fig 2.1, in which there are six terminal variables: the field voltage and current \((E_f, I_f)\), the armature voltage and current \((E_a, I_a)\), and the mechanical angular velocity and shaft torque \((\omega_m, M_L)\).

The equations relating these variables are

for the field circuit

\[ E_f = R_f I_f + L_f \frac{dI_f}{dt} \]  \hspace{1cm} (2.1)

for the armature circuit

\[ E_a = K_a \phi \omega_m + L_a \frac{dI_a}{dt} + R_a I_a \]  \hspace{1cm} (2.2)

and for the mechanical system

\[ M_L = M_{INT} - J \frac{d\omega_m}{dt} - M_{LOSS} \]  \hspace{1cm} (2.3)

where the electromagnetically produced torque is given by

\[ M_{INT} = K_a \phi I_a \]
If any of the quantities $I_f, I_a$ or $\omega_m$ remains constant, the term in equations (2.1) to (2.3) which contains its time derivative is zero. With constant flux, the generated armature voltage $E_a$ is directly proportional to the angular velocity $\omega_m$, or

$$E_a = K_a \phi \omega_m$$

During steady-state operation, the armature current is constant and, from equation (2.2), the steady-state speed of the motor is

$$\omega_m = \frac{E_a - I_a R_a}{K_a \phi}$$

(2.4)

This relationships shows that the steady-state speed may be varied by adjustment of either

a) Flux (using field current control)

b) Armature circuit resistance, or

c) Armature terminal voltage.

2.1.1 FIELD CURRENT CONTROL

With field current control the highest speed obtainable is restricted by armature reaction effects, which eventually cause either the speed to become unstable or the commutation to become poor. This type of control is referred to as a constant power drive, since the maximum output power available remains constant over the entire speed range, whereas the torque varies directly with the motor flux.
2.1.2 ARMATURE RESISTANCE CONTROL

Armature-resistance control is achieved by the insertion of external series resistance. However, for a fixed value of resistance the speed varies widely with load and, in addition, the power loss in the resistor is large especially when the speed is low. Armature-resistance control provides a constant torque drive, because both the flux and the maximum armature current remain constant as the speed changes.

2.1.3 ARMATURE VOLTAGE CONTROL

Armature-voltage control utilises the fact that a change in armature voltage is accompanied by an almost proportionate change in both the generated emf and the motor speed. Traditionally, a motor/generator set has been used to provide a controlled armature voltage but, with the development of high-power solid-state devices, the range of possibilities for the precise control of this voltage has increased considerably.

Control by reduction of the armature voltage provides speeds below the rated or base value, while for speeds above the base value field control must be adopted. The direction of rotation of the motor depends on the polarity of the main magnetic field and the direction of the armature current, so that a reversal of rotation is achieved by a reversal of either, but not both, of these quantities.

2.2 ELECTRICAL BRAKING

Electrical braking using either dynamic or regenerative techniques is often a feature of a motor drive, to enable the kinetic energy of the rotating system to be converted to electrical energy. With dynamic braking the electrical
energy is dissipated in a resistor stack, whereas with regenerative braking it is returned to the supply, thereby improving the drive efficiency.

2.2.1 REGENERATIVE BRAKING

Regenerative braking is conceptually simple and, in the case of the separately-excited motor, it may be achieved with no circuit changes. An increase in speed due to load rejection may cause the back emf to exceed the line voltage, resulting in a reversal of the armature current and power thereby being returned to the supply. Furthermore, if for any other reason the supply voltage falls and becomes less than the armature emf, regeneration will again take place. Braking by this means is however only available over a limited speed range, and to bring the drive to rest requires either plugging or the use of a mechanical brake. At high speed the braking effect produced by regeneration is far less than that provided by dynamic braking, but it is widely used because of its efficiency and simplicity, especially in transit vehicles and battery-operated electric cars.

2.3 SOLID-STATE DRIVES

Historically, variable armature-voltage control was achieved using a Ward-Leonard arrangement, but modern power electronic techniques, such as those indicated in Fig 2.2, have many advantages over such a scheme, since:

a) The field and armature time constants inherent in the Ward-Leonard set are eliminated
b) The control circuit is simple and reliable
c) Minimal maintenance is required
d) The efficiency is high

e) The small size and weight together result in reduced space requirements and lower cost.

There are however a number of attendant disadvantages, since:

a) The ripple content of the drives outputs is relatively high

b) No power factor improvement is achievable (if the supply is AC)

There are however a number of attendant disadvantages, since:

c) The overload capability is comparatively small

d) The AC supply voltage may be distorted and RF interference produced.

The considerable extent to which solid-state converters are now used indicates that these disadvantages are not generally too serious or else that they can readily be overcome. The three basic methods which are available for the provision of a variable DC voltage from a constant AC or DC supply are phase control, integral cycle control, and chopper control. The first two of these achieve conversion by AC-to-DC rectification, whereas the third involves DC-to-DC conversion.

2.3.1 AC TO DC CONVERTERS

In both phase and integral cycle control schemes the AC supply voltage turns off the semiconductor switches in the converter. No commutation circuits are necessary and the schemes are simple and inexpensive. Phase control is widely used, since it can control the output voltage smoothly over a wide range, but it has the disadvantage that the supply power factor decreases at low output voltages. Integral
cycle control is satisfactory if the supply frequency is high, otherwise the motor speed may oscillate about a mean value.

2.3.1.1 PHASE CONTROL

A phase controller connects the motor to the supply for only a portion of each half-cycle of the AC supply, to provide the armature voltage waveform shown in Fig 2.2(a). Commutation occurs naturally, since the incoming thyristor reverse-biases the outgoing thyristor and thereby turns it off. No additional commutation circuitry is required.

Phase-controlled converters may be broadly classified into single-phase or 3-phase types. Semiconverters are one-quadrant devices, in that only one polarity of voltage and current is possible at the DC terminals. Full converters are 2-quadrant devices, in that although the voltage polarity can reverse the current is always unidirectional. Dual or inverse-parallel converters can operate in all four quadrants.

In many single-phase converters the motor armature current may become discontinuous, causing a deterioration of the drive performance. In 3-phase converters the motor current is usually continuous, and the higher ripple frequency at the motor terminal results in less onerous filtering requirements.

The 3-phase half-wave converter is impractical for most purposes, because the supply current contains a DC component. Semi-converters and full-converters are most commonly used in practice, with dual converters being employed in reversible drives having power ratings of up to several megawatts.
2.3.1.2 INTEGRAL CYCLE CONTROL

With integral-cycle control the converter connects the motor to the supply for a discrete number of complete half cycles, followed by disconnection again for a discrete number of half cycles. This process provides armature voltage waveforms as shown in Fig 2.2(b).

2.3.2 DC-TO-DC CONVERSION

Fig 2.2(c) to (e) show the three main methods of DC to DC conversion using solid-state switching devices, these being inverter/rectifier combinations, H-bridge choppers and switched-mode DC-to-DC converters.

2.3.2.1 INVERTER/RECTIFIER SCHEME

In this technique (see Fig 2.2(c)), the DC supply is first converted to AC, which is stepped up or down by a transformer before rectification back to DC. Since the conversion is in two stages the scheme is costly, bulky and less efficient than the other methods considered below. However the electrical isolation provided by the transformer between the supply and the load is a useful and often required feature.

2.3.2.2 DC CHOPPERS

The 4-quadrant H-bridge chopper of Fig 2.2(d) can replace the series resistor sometimes used to provide speed control of a DC motor, so that it can be used in battery-operated vehicles where energy saving is of prime concern. However, the H-bridge chopper suffers from the following drawbacks:
a) The ripple content of the converter output is high if the switching frequency is low, with significant harmonics being present in both input and output currents.
b) The input voltage may only be stepped down, so that the output voltage is always less than that of the input voltage.

2.3.2.3 DC-TO-DC CONVERTERS

This is a direct method of DC-to-DC conversion, in which energy is transferred from the input to the output through an inductor. The output voltage is stepped either up or down by changing the ratio of the switch turn-on and turn-off times. Fig 2.2 (e) shows that the DC-to-DC converter may be visualised as the DC equivalent of a variable-ratio transformer.

A novel form of 4-quadrant DC-to-DC converter is described in detail in chapter 3. This converter provides a superior, highly efficient and easily controlled supply for a DC motor drive.
Fig 2.1 Equivalent Circuit for Separately-Excited DC Motor
Fig 2.2 Control Techniques For Obtaining Variable DC-Voltage
CHAPTER 3 DC-TO-DC CONVERTER

A switched-mode power converter provides a highly efficient method of DC-to-DC conversion. There are many types of converters, all having varying degrees of cost, reliability, complexity and efficiency.

The three basic configurations which are commonly used are termed buck, boost and buck/boost converters. A buck converter steps down the input voltage and a boost converter steps it up, while a buck/boost converter provides either step-up or step-down operation. There are other forms of converter, such as the flyback and the forward converter, each of which is derived from one of the basic configurations. The new 4-quadrant converter described in this chapter is derived from the boost converter and is designed specifically to meet the requirements of 4-quadrant operation for a high-efficiency DC servo system.

3.1 BUCK CONVERTER

The idealized buck converter of Fig 3.1 steps down the input voltage by variation of the switching duty cycle. During the switching cycle, switch $S$ alternates between positions A and B. When $S$ is in position A, the inductor current $I_L$ increases and energy is stored in the magnetic field of the inductor. When $S$ switches to position B, the voltage across $L$ changes polarity and the current $I_L$ decays. The energy stored in the inductor is thereby released to the output.

There are two distinct operating modes for the buck converter; the continuous conduction mode, in which the inductor current never falls to zero and the discontinuous conduction mode, in which the current remains at zero for a portion of each switching period. Figs 3.2 and 3.3 show
respectively various converter waveforms for these two modes of operation, from which the converter voltage gain and the inductor current may be obtained. Switch S is in position A for time $t_1$ and position B for $t_2$. The switching period is $T_s = t_1 + t_2$. In these figures, and others which follow throughout the thesis, the waveforms of inductor and source current are almost straight lines as a consequence of the high operating frequency.

In the continuous conduction-mode, the time integral of the inductor voltage $V_L$ over a switching period is zero. Thus

$$\int_0^{T_s} V_L dt = \int_0^{t_1} V_L dt + \int_{t_1}^{T_s} V_L dt = 0$$

From Fig 3.2, this gives

$$(V_s - V_o)t_1 = V_o(T_s - t_1)$$

from which the voltage gain $M$ of the converter is

$$M = \frac{V_o}{V_s} = \frac{t_1}{T_s} = D \quad (3.1)$$

where $D$ is the duty cycle. During steady-state operation, the energy released from the inductor during time $t_2$ is dissipated in the load resistor $R$. Thus,

$$\frac{1}{2}LI_b^2 - \frac{1}{2}LI_a^2 = \frac{V_o^2}{R}t_2 \quad (3.2)$$

where $I_a$ and $I_b$ are respectively the minimum and maximum values of the inductor current. Since the average capacitor current is zero the average output current equals the aver-
age inductor current, or

\[
\frac{I_a + I_b}{2} = I_o = \frac{V_o}{R}
\]

giving

\[
I_a = \frac{2V_o}{R} - I_b
\]  \hspace{1cm} (3.3)

Substituting for \( I_a \) from equation (3.2) into equation (3.3) gives,

\[
I_b = \frac{V_o}{R} \left[ 1 + \left( \frac{1-D}{2\tau} \right) \right]
\]

and therefore

\[
I_a = \frac{V_o}{R} \left[ 1 - \left( \frac{1-D}{2\tau} \right) \right]
\]

where

\[
\tau = \frac{L}{RT_s}
\]

is the time constant normalized with respect to the switching period.

For discontinuous operation, the equations which govern the buck converter currents may similarly be obtained from Fig 3.3, and the voltage gain becomes (Appendix III):

\[
M = \frac{2}{1 + \sqrt{1 + 8\tau/D^2}}
\]

Both sets of equations are listed in Table 3.1.
Continuous Mode | Discontinuous Mode
---|---
\( M = \frac{V_o}{V_s} \) | \( D \)
\( \frac{2}{1+\sqrt{1+8\tau/D^2}} \)
\( I_a(I_{L(min)}) = \frac{V_o}{R} \left[ 1-\left(\frac{1-D}{2\tau}\right) \right] \) | 0
\( I_b(I_{L(max)}) = \frac{V_o}{R} \left[ 1+\left(\frac{1-D}{2\tau}\right) \right] \) | \( \frac{4V_o}{RD(1+\sqrt{1+8\tau/D^2})} \)
\( I_s(Ave) = \frac{V_o D}{R} \) | \( \frac{V_o D}{R} \)

Table 3.1 Buck Converter Current And Voltage Gain

For a given value of \( M \), the boundary between the two modes is determined by \( \tau \), which is dependent on both \( L \) and \( R \). The boundary value of the normalized time constant for the transition between the discontinuous and continuous modes is \([1,2]\)

\[
\tau_{LC} = \frac{1-M}{2}
\]

(3.4)

If \( \tau < \tau_{LC} \) the mode is discontinuous, whereas if \( \tau > \tau_{LC} \) it is continuous.

Fig 3.4 shows the relationship between the voltage gain \( M \) and the duty cycle \( D \), for various values of the normalized time constant \( \tau \). It is evident that the output-to-control transfer characteristics are quite different for the two modes of operation. In the continuous mode \( M \) is equal to \( D \), and is independent of the circuit elements \( L \) and \( R \). In the discontinuous mode \( M \) is a function of all these elements, as well as of \( T_s \).
3.2 BOOST CONVERTER

3.2.1 BOOST CONVERTER OPERATION

A circuit diagram for the ideal boost converter is shown in Fig 3.5(a). During each switching cycle S moves from position A to position B, and the circuit topology changes correspondingly as shown in Fig 3.5(b). Idealised circuit waveforms for both continuous and discontinuous operations are given in Fig 3.6 and 3.7. At the beginning of the switching cycle S is in position A for time $t_1$, and the inductor current $I_L$ increases from $I_a$ at $t=0$ towards a peak of $I_b$. Switch S then moves to position B, and the energy stored in the inductor is released to the output network (R and C), with the current $I_L$ falling during the time interval $t_2$. If the converter is operating in the continuous conduction mode the current ramps down to $I_a$ at the end of the switching cycle as shown in Fig 3.6. If it is in the discontinuous mode the current $I_L$ at the end of $t_2$ is zero, as shown in Fig 3.7, with all the energy stored in the inductor having been delivered to the output. After a time during which the current remains zero, the switching cycle is repeated.

For both modes of operation it is evident that the output voltage is greater than the input voltage, otherwise the energy stored in L is not released to the output during time $t_2$.

3.2.2 LARGE-SIGNAL STEADY-STATE CHARACTERISATION OF THE BOOST CONVERTER

Equations defining the circuit currents and voltages for the ideal boost converter, and obtained in a manner similar to those of Section 3.1, are summarized in Table 3.2.
The boundary between the continuous and discontinuous conduction modes occurs at a time constant \( \tau = \tau_{LC} \), where [1, 2]

\[
\tau_{LC} = \frac{D(1-D)^2}{2}
\]  

(3.5)

or

\[
\tau_{LC} = \frac{(M-1)}{2M^3}
\]  

(3.6)

The converter is in the continuous mode if \( \tau > \tau_{LC} \) and the discontinuous mode if \( \tau < \tau_{LC} \). The boundary between these two modes is shown in Figs 3.8 and 3.9 as a function of D and M respectively.

<table>
<thead>
<tr>
<th></th>
<th>Continuous Mode</th>
<th>Discontinuous Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M )</td>
<td>( \frac{1}{1-D} )</td>
<td>( \frac{1+\sqrt{1+2D^2/\tau}}{2} )</td>
</tr>
<tr>
<td>( I_a )</td>
<td>( \frac{V_o}{R} \left[ \frac{1}{1-D} + \frac{1}{2\tau}D(1-D) \right] )</td>
<td>0</td>
</tr>
<tr>
<td>( I_b )</td>
<td>( \frac{V_o}{R} \left[ \frac{1}{1-D} - \frac{1}{2\tau}D(1-D) \right] )</td>
<td>( \frac{V_o(-1+\sqrt{1+2D^2/\tau})}{RD} )</td>
</tr>
<tr>
<td>( I_{L(Ave)} )</td>
<td>( \left( \frac{V_o}{R} \right) \frac{1}{1-D} )</td>
<td>( \frac{V_o(1+\sqrt{1+2D^2/\tau})}{2R} )</td>
</tr>
<tr>
<td>( I_{T(Ave)} )</td>
<td>( \left( \frac{V_o}{R} \right) \frac{D}{1-D} )</td>
<td>( \frac{V_o(-1+\sqrt{1+2D^2/\tau})}{2R} )</td>
</tr>
<tr>
<td>( I_{D(Ave)} )</td>
<td>( \frac{V_o}{R} )</td>
<td>( \frac{V_o}{R} )</td>
</tr>
</tbody>
</table>

Table 3.2 Boost Converter Current And Voltage Gain
For continuous operation, consideration of the voltage-time integral balance for the inductor voltage $V_L$ of Fig 3.6 gives

$$V_s t_1 = (V_o - V_s) t_2$$

from which the voltage gain is

$$M = \frac{V_o}{V_s} = \frac{t_1 + t_2}{t_2} = \frac{1}{1 - D} \quad (3.7)$$

For discontinuous operation the voltage gain $M$ is (see Appendix III)

$$M = \frac{1 + \sqrt{1 + 2D^2/\tau}}{2} \quad (3.8)$$

Variations of $M$ with $D$ for various values of $\tau$, determined using equation (3.8), are given in Fig 3.10, together with the variation for continuous operation. It is noted that, for continuous operation, the relationship between $M$ and $D$ is nonlinear, with the value $M$ rising rapidly with $D$. In contrast, during discontinuous operation the relationship is almost a straight line, irrespective of the time constant. It is also evident that, for a given duty cycle, the voltage gain in the discontinuous mode is larger than that when it is in the continuous mode.

3.2.3 BIDIRECTION BOOST CONVERTER

With the boost converter circuit of Fig 3.5(a) energy can be extracted from, but not returned to, the supply since there is no return path for the current. In other words, the circuit is incapable of regeneration.
To obtain bi-directional energy flow capability, an extra switch \( S_2 \) and a diode \( D_2 \) are added as shown in Fig 3.11. The voltage and current waveforms corresponding to this circuit are given in Fig 3.12. Switches \( S_1 \) and \( S_2 \) operate in complementary fashion, such that during time \( t_2 \), \( S_1 \) is open and \( S_2 \) is closed. The decaying inductor current \( I_L \) then flows via diode \( D_1 \) to charge the capacitor \( C \). If \( I_L \) reduces to zero, it now has a path through which it can reverse and flow via \( S_2 \) to return energy to the source.

During time \( t_1 \), switch \( S_2 \) is open and \( S_1 \) is closed. Initially, if \( I_L \) is negative and energy is being returned to the supply, \( I_L \) decays to zero through the freewheeling diode \( D_2 \). Since \( S_1 \) is closed, the current \( I_L \) again reverses and ramps up via \( S_1 \) until it reaches \( I_b \) at the end of \( t_1 \).

Since \( I_L \) is continuous, the voltage gain of the converter may be obtained from equation (3.7) as

\[
M = \frac{1}{1 - D}
\]  

(3.9)

3.3 BUCK/BOOST CONVERTER

The buck/boost converter shown in Fig 3.13 is capable of both step-up and step-down operation. During the switching cycle the switch \( S \) moves between positions A and B, so that when it is at A, the inductor current increases and energy from the supply is stored in the inductor. When the switch moves to position B, the stored energy is released to the output and power conversion is realised.

Both continuous and discontinuous modes of operation are again possible and the voltage gains in the different modes are [1,2]:
Continuous mode

\[
M = \frac{D}{1-D} \tag{3.10}
\]

from which it is evident that, if D<0.5, M<1 and the converter performs as a buck converter and that if D>0.5, M>1 and the converter performs as a boost converter.

Discontinuous mode

\[
M = \frac{D}{\sqrt{2\tau}} \tag{3.11}
\]

The variation of M with D for various values of \(\tau\), determined using equation (3.11), are shown in Fig 3.14. Once again, the boundary between the modes is dependent on \(\tau\) and now \([1,2]\):

\[
\tau_{nc} = \frac{(1-D)^2}{2} \tag{3.12}
\]

3.4 4-QUADRANT DC-TO-DC CONVERTER

The output voltage of the novel 4-quadrant converter described below can be either greater or less than the supply voltage, and it can be of either positive or negative polarity. With a non-passive load, 4-quadrant operation may be achieved.

3.4.1 BASIC PRINCIPLE

The new converter is formed by parallelling two bidirectional boost converters, as shown in Fig 3.15, with the
power switches $S_1$, $S_3$ and $S_2$, $S_4$ operating in a complementary mode. During time $t_1$ switches $S_1$, $S_3$ are closed and $S_2$, $S_4$ are open, as shown in Fig 3.16(a). As the current $I_{L1}$ builds up, energy is stored in the inductor $L_1$. During period $t_2 (=T_s-t_1)$, $S_1$, $S_3$ are open and $S_2$, $S_4$ are closed, as shown in Fig 3.16(b). The energy stored previously in $L_1$ is released through diode $D_1$ to charge the capacitor $C_1$ to a voltage $V_{c1}$. Similarly, the build-up of the current $I_{L2}$ stores energy in the inductor $L_2$ which, at the commencement of the next duty cycle, is released through diode $D_2$ to charge the capacitor $C_2$ to a voltage $V_{c2}$.

It is evident from section 3.2 that the voltages $V_{c1}$ and $V_{c2}$ are dependent on the turn-on times of the switches $S_1$ and $S_2$. If $t_1 > t_2$, $V_{c1} > V_{c2}$ and the overall output voltage, which is the difference between $V_{c1}$ and $V_{c2}$, is positive. The load current $I_o$ is in the direction shown in Fig 3.15 and energy is taken from the supply. At the same time energy is returned to the source through $S_3$, although more energy is taken than is returned.

If $V_{c2}$ is raised so that it exceeds $V_{c1}(t_2 > t_1)$, the polarity of $V_o$ reverses but the direction of the load current remains unchanged. More energy is returned to the supply via $S_3$ than is taken via $S_1$ and the converter operates in a regenerative mode. Fig 3.17 shows theoretical voltage and current waveforms for this condition.

3.4.2 LARGE SIGNAL STEADY-STATE CHARACTERIZATION

If the losses in the converter are ignored, the voltage gain of the bidirectional boost converter is, from section 3.2
\[ M = \frac{1}{1-D} \]

and the duty cycle for the complementary converter is

\[ D' = 1 - D = \frac{t_2}{T_s} \]

It follows that the capacitor voltages are

\[ V_{c1} = \frac{V_s}{1-D} \]

and

\[ V_{c2} = \frac{V_s}{1-D'} = \frac{V_s}{D} \]

respectively, which gives an output voltage of

\[ V_o = V_{c1} - V_{c2} = \left( \frac{1}{D'} - \frac{1}{D} \right) V_s \]

and a voltage gain of

\[ M = \frac{V_o}{V_s} = \frac{2D-1}{DD'} \quad (3.13) \]

Considerations of equation (3.13) show that variation of \( D \) between zero and 1 enables the output voltage to be either less than or greater than the input voltage and the polarity of the output voltage to be reversed. Table 3.3 presents equations for the complete operational range of the converter and Fig 3.18 shows the variation of voltage gain with duty cycle.
<table>
<thead>
<tr>
<th>$\sqrt{5}-1 &lt; D &lt; 1$</th>
<th>$V_{cl} &gt; V_{c2}$</th>
<th>$M &gt; 1$</th>
<th>$V_o &gt; V_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0.5 &lt; D &lt; \frac{\sqrt{5}-1}{2}$</td>
<td>$V_{cl} &gt; V_{c2}$</td>
<td>$0 &lt; M &lt; 1$</td>
<td>$0 &lt; V_o &lt; V_s$</td>
</tr>
<tr>
<td>$D = 0.5$</td>
<td>$V_{cl} = V_{c2}$</td>
<td>$M = 0$</td>
<td>$V_o = 0$</td>
</tr>
<tr>
<td>$\frac{3-\sqrt{5}}{2} &lt; D &lt; 0.5$</td>
<td>$V_{cl} &lt; V_{c2}$</td>
<td>$-1 &lt; M &lt; 0$</td>
<td>$-V_s &lt; V_o &lt; 0$</td>
</tr>
<tr>
<td>$0 \leq D &lt; \frac{3-\sqrt{5}}{2}$</td>
<td>$V_{cl} &lt; V_{c2}$</td>
<td>$M &lt; -1$</td>
<td>$V_o &lt; -V_s$</td>
</tr>
</tbody>
</table>

Table 3.3 Operation Range Of 4-Quadrant DC-to-DC Converter
Fig 3.2 Buck Converter Waveforms
(Continuous Mode)
Fig 3.3 Buck Converter Waveforms
(Discontinuous Mode)
Fig 3.4 Voltage Gain For Buck Converter
Fig 3.5(a) Boost Converter

Fig 3.5(b) Boost Converter With Different Position Of Switch
Fig. 3.6 Boost Converter Waveforms (Continuous Mode)
Fig 3.7 Boost Converter Waveforms
(Discontinuous Mode)
Fig 3.8 Mode Boundary Of Boost Converter As A Function Of Duty Cycle

Fig 3.9 Mode Boundary Of Boost Converter As A Function Of Voltage Gain
Fig 3.10 Voltage Gain For Boost Converter

Fig 3.11 2-way Boost Converter
Fig 3.12 2-Way Boost Converter Waveforms
Fig 3.13 Buck/Boost Converter

Fig 3.14 Voltage Gain For Buck/Boost Converter
**Figure 3.15** 4-Quadrant DC/DC Converter

**Figure 3.16** Two Switching States of 4-Quadrant DC-DC Converter

(a) $S_1$, $S_3$ Closed & $S_2$, $S_4$ Open
(b) $S_1$, $S_3$ Open & $S_2$, $S_4$ Closed
Fig 3.17 Waveforms of 4-Quadrant Converter
Fig 3.18 Voltage Gain For 1-Quadrant DC/DC Converter
CHAPTER 4 MODELLING AND ANALYSIS OF DC-TO-DC CONVERTER

A mathematical model was developed for the converter, in order to examine its dynamic performance in terms of stability, output impedance and step-load transient response. The performance criteria can be established using the transfer functions relating to the various blocks of Fig 4.1, which shows the basic closed-loop switched-mode regulator.

Modelling of the linear blocks in the closed-loop system is straightforward, and the problem reduces to that of finding a transfer function for the non-linear modulator and switching power stages. It is apparent that the non-linear sub-system is a 3-port system, with two input ports, $V_s(t)$ and $V_c(t)$, and one output port $V_o(t)$. The relationships required are the input-to-output transfer function $V_s(t)$ to $V_o(t)$, and the control-to-output transfer function $V_c(t)$ to $V_o(t)$. The latter may be divided into two parts: the relationship between the control signal $V_c(t)$ and the duty cycle $d(t)$, which is a property of the modulator, and that between the duty cycle $d(t)$ and the output $V_o(t)$, which is a property of the power stage. The mathematical modelling of the power stage is discussed in this chapter, with the design of the modulator, which depends on the dynamic performance of the power stage, being discussed later in chapter 8.

4.1 STATE-SPACE-AVERAGING METHOD

The converter has two operating states corresponding to the different states of the switches, and for each of these there is a linear equivalent circuit. There is no closed form solution for the circuit equations and the numerical solution which is necessary fails to reveal any analytical relationships between the various parameters.
During the last ten years many continuous analytical methods have been developed, which employ linear continuous models to produce approximate closed-form solutions for switched-mode circuits. One method, termed the State-Space Averaging approach [3,4] has many advantages over the others. It is very general, relatively easy to comprehend and straightforward in its application to the solution of practical converter problems. Furthermore, the method reveals completely the properties of the converter and arrives therefore at the complete linearised converter model which other methods fail to do. Due to these advantages, the State-Space Averaging method was used to model the 4-quadrant converter described in the thesis.

4.2 MODELLING PROCEDURE

State-Space Averaging provides the designer with a choice of either a mathematical or an equivalent circuit model. The mathematical model is very useful, since it enables the designer to calculate the voltages, currents, and small-signal transfer functions for the converter circuit. However, it does not readily explain the circuit operation and a full understanding of this is normally obtained from an equivalent circuit model, and both models are often used to solve practical design problems. The development of either model starts with the manipulation of the circuit equations until a satisfactory mathematical model is obtained. From there, the procedure continues with the synthesis of an equivalent circuit model.

The procedure follows a number of well-defined steps:

a) the construction of a linear equivalent circuit for the converter, relating to each switch position.

b) the development in state-variable form of the circuit
equations for each equivalent circuit of step(a).

c) the averaging of each set of equations, using the switch duty cycle as a weighting factor and the combination by summation of the two sets to form a single set.

d) the perturbation of the averaged set of equations of step(c) to produce DC and small-signal terms and to eliminate any nonlinear cross products.

e) the transformation of the small-signal or AC terms of step(d) into the complex frequency or s domain.

f) the production of an equivalent circuit model corresponding to the mathematical equations formed by the earlier steps.

4.3 MODELLING OF A BOOST CONVERTER

Assuming ideal circuit components, fig 4.2 shows the equivalent circuits for each of the two switching states of the converter. The corresponding circuit equations in state-variable form are:

a) During interval $t_1$,

\[
\begin{bmatrix}
\dot{I}_L \\
\dot{V}_c
\end{bmatrix} = \begin{bmatrix}
0 & 0 \\
0 & -\frac{1}{RC}
\end{bmatrix} \begin{bmatrix}
I_L \\
V_c
\end{bmatrix} + \begin{bmatrix}
\frac{1}{L} \\
0
\end{bmatrix} V_s
\]
where \[ I_t = \frac{dI_t}{dt} \]
and \[ V_c = \frac{dV_c}{dt} \]

or \[ \dot{X} = A_1 X + B_1 V_s \]

where \[ \dot{X} = \frac{dX}{dt} \] \[ X = \begin{bmatrix} I_L \\ V_c \end{bmatrix} \]

\[ A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \]
\[ B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \]

and \[ V_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} \]

or \[ Y = C^T_1 X \]

where \[ Y = V_o \]
\[ C^T_1 = [0 \ 1] \]

b) During interval \( t_2 \)

\[ \begin{bmatrix} I_L \\ V_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_s \]

or \[ \dot{X} = A_2 X + B_2 V_s \]

where \[ A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \]
\[ B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \]
and \( V_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_o \end{bmatrix} \)

or \( Y = C^T_2 X \)

where \( C^T_2 = \begin{bmatrix} 0 & 1 \end{bmatrix} \)

Taking the average of the state-space equations for the two switch intervals, with the duty cycle \( d \) used as a weighting factor, results in a single state-space description, which represents approximately the behaviour of the circuit over the whole period \( T \), as

\[
\dot{X} = AX + BV, \quad (4.1)
\]

\[
y = C^T X \quad (4.2)
\]

where \( A = dA_1 + d'A_2 \)
\( B = dB_1 + d'B_2 \)
\( C^T = dC^T_1 + d'C^T_2 \)
\( d \) is the duty cycle and \( d' = 1 - d \)

Equation (4.1) and (4.2) may be expanded to

\[
\begin{bmatrix} I_L \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{1-d}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_o, \quad (4.3)
\]

and \( V_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_o \end{bmatrix} \quad (4.4) \)

A single set of equations (4.3) and (4.4) in state-variable form is thus obtained and its DC (steady state) and small-signal (dynamic) terms may be produced by perturbing
the supply voltage \( V_s \), and the duty cycle \( d \) respectively.

### 4.3.1 STEADY-STATE CONDITION

Under steady-state conditions, the duty cycle \( d \) attains a steady value \( D \) so that \( x = 0 \) and from equations (4.1) to (4.4)

\[
X = -A^{-1}BV_s 
\]

or

\[
\begin{bmatrix} I_L \\ V_c \end{bmatrix} = \frac{V_s}{R'} \begin{bmatrix} 1 \\ (1-D)R \end{bmatrix}
\]

where \( R' = (1-D)^2R \)

\[
V_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ (1-D)R \end{bmatrix} \frac{V_s}{R'}
\]

or

\[
V_o = \frac{V_s(1-D)R}{R'} = \frac{V_s}{1-D}
\]  \hspace{1cm} (4.5)

which corresponds to the result obtained in chapter 3.

### 4.3.2 DYNAMIC CONDITION

A small signal model for the converter may be obtained by considering perturbations of the supply voltage \( V_s \), and the switching duty cycle \( d \).

Thus, let

\[
V_s = \overline{V_s} + 
\]

\[
d = D + \delta
\]

and

\[
d' = 1 - d = D' - \delta
\]

where \( D, D', \overline{V_s} \) are the steady-state values, \( \delta \) is the variation in \( V_s \).
and \( \Delta \) is the variation in \( d \).

These perturbations cause corresponding perturbations in the state and output vectors \( X = \overline{X} + \bar{X} \) and \( Y = \overline{Y} + \bar{Y} \) where \( \overline{X}, \overline{Y} \) are the steady state values and \( \bar{X}, \bar{Y} \) the variations in \( X \) and \( Y \) respectively.

It now follows from equation (4.1) that

\[
\dot{X} = \overline{A}X + \overline{B}V_s + \overline{A}\dot{X} + \overline{B}\dot{V}_s + \Delta[(A_1 - A_2)\overline{X} + (B_1 - B_2)\overline{V}_s]
\]

\[
+ \Delta[(A_1 - A_2)\bar{X} + (B_1 - B_2)\bar{V}_s]
\]

where

\[
\overline{A} = DA_1 + D'A_2
\]

\[
\overline{B} = DB_1 + D'B_2
\]

Since \( \overline{A}X + \overline{B}V_s = \overline{X} \) (steady-state equation)

and

\[
\overline{X} = \frac{d\overline{X}}{dt} = 0
\]

thus,

\[
\overline{A}X + \overline{B}V_s = 0
\]

If it is assumed that

\[
\frac{\dot{V}_s}{V_s} \ll 1, \quad \frac{\Delta}{D} \ll 1, \quad \frac{\bar{X}}{\overline{X}} \ll 1
\]

small nonlinear terms, such as second-order terms, are negligible and a linear system is obtained for which

\[
\dot{X} = \overline{A}X + \overline{B}V_s + [(A_1 - A_2)\overline{X} + (B_1 - B_2)\overline{V}_s]\Delta
\]  (4.6)

and

\[
\dot{Y} = C^T\dot{X}
\]  (4.7)
Expressing equations (4.6) and (4.7) in terms of Laplace Transforms gives

\[ s\hat{x}(s) = \bar{A}\hat{x}(s) + \bar{B}\hat{V}_s(s) + [(A_1 - A_2)\bar{x} + (B_1 - B_2)\bar{V}_s]d(s) \]  
(4.8)

and

\[ Y(s) = \hat{V}_o(s) = C^T\hat{x}(s) \]  
(4.9)

where \( \hat{V}_o \) is the perturbation in \( V_o \).

Substituting equation (4.8) in (4.9) gives

\[ \hat{V}_o(s) = C^T(sI - \bar{A})^{-1}\bar{B}\hat{V}_s(s) + C^T(sI - \bar{A})^{-1}[(A_1 - A_2)\bar{x} + (B_1 - B_2)\bar{V}_s]d(s) \]

or

\[ \hat{V}_o(s) = G_{vs}(s)\hat{V}_s(s) + G_{vd}(s)d(s) \]  
(4.10)

For constant duty cycle, \( \bar{d} = 0 \) and \( d = D \) and the voltage input-to-output transfer function may be obtained. Thus, from equation (4.10), since \( \bar{d} = 0 \)

\[ \hat{V}_o(s) = G_{vs}(s)\hat{V}_s(s) \]

or

\[ \frac{\hat{V}_o(s)}{\hat{V}_s(s)} = G_{vs}(s) = C^T(sI - \bar{A})^{-1}\bar{B} \]

Since

\[ \bar{A} = \begin{bmatrix} 0 & - \frac{1-D}{L} \\ \frac{1-D}{C} & - \frac{1}{RC} \end{bmatrix} \]

and

\[ \bar{B} = \begin{bmatrix} 1 \\ \frac{1}{L} \end{bmatrix} \]
thus
\[
\frac{\dot{V}_o(s)}{V_s(s)} = \frac{1}{D' \left[ L/C / D' s^2 + (L/R D') s + 1 \right]}
\]

If \( V_s \) is constant, \( \dot{V}_s = 0 \) and \( V_s = \overline{V}_s \), the control-to-output transfer function may be obtained from equation (4.10) as
\[
\dot{V}_o(s) = G_{eq}(s) \dot{d}(s) = C^T (S I - \overline{A})^{-1} [(A_1 - A_2) \overline{x} + (B_1 - B_2) \overline{V}_s] \dot{d}(s)
\]

where
\[
A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}, \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ -\frac{1}{R C} & 0 \end{bmatrix}, \quad \overline{A} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{RC} \end{bmatrix}
\]

\[
C^T = [0 \quad 1], \quad \overline{B} = B_1 = B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}
\]

and since for steady-state conditions,
\[
\overline{x} = -\overline{A}^{-1} \overline{B} \overline{V}_s
\]

then
\[
\frac{\dot{V}_o(s)}{d(s)} = G_{eq}(s) = \frac{\overline{V}_s}{(1-D)^2} \frac{(1-s L_s / R)}{(1+s L_s / R + s^2 L_s C)}
\]

where
\[
L_s = \frac{L}{(1-D)^2}
\]

On the basis of the analysis above, it may be concluded that:
1) In the steady state condition

\[ \bar{X} = -\bar{A}^{-1} \bar{B} \bar{V}_s \]
\[ \bar{Y} = \bar{V}_o = \frac{\bar{V}_s}{1 - D} \]

2) In the dynamic state (AC model)

\[ \dot{V}(s) = \dot{V}_0(s) = G_{us}(s)\dot{V}_s(s) + G_{vd}(s)\dot{d}(s) \]

where

\[ G_{us}(s) = \frac{1}{D' \frac{D}{D'} s^2 + \frac{1}{(RD' s + 1)}} \]

\[ G_{vd}(s) = \frac{\bar{V}_s}{(1-D)^2} \frac{(1-sL_s/R)}{\frac{1+L_s/R}{s^2 L_o C}} \]

in which

\[ L_o = \frac{L}{(1-D)^2} \]

If \( \dot{d} = 0 \),

\[ G_{us}(s) = \frac{\dot{V}_0(s)}{\dot{V}_s(s)} \]

and if \( \dot{V}_s = 0 \),

\[ G_{vd}(s) = \frac{\dot{V}_o(s)}{\dot{d}(s)} \]

4.4 MODEL FOR THE NOVEL 4-QUADRANT CONVERTER

The 4-quadrant converter shown in Fig 4.3 comprises two boost converters with a differential load. The supply volt-
age \( V \), is assumed constant and the only variation considered is the switching duty cycle. Since operation of the switches \( S_1 \) and \( S_2 \) is complementary, any variation in the duty cycle \( d \) of \( S_1 \) will change the duty cycle \( d' \) of \( S_2 \), to maintain \( d + d' = 1 \)

If \( d = D + \hat{d} \)
then \( d' = D' + (-\hat{d}) \)

An increase in the duty cycle of the upper converter of Fig 4.3 is accompanied by a decrease in that of the lower converter and the output voltage \( V_o \) is given by

\[
V_o = V_{c1} - V_{c2}
\]

In the dynamic condition,

\[
\dot{V}_o = \dot{V}_{c1} - \dot{V}_{c2}
\]

Expressed in terms of Laplace Transforms,

\[
\mathcal{L}\{\dot{V}_o\} = \mathcal{L}\{\dot{V}_{c1}\} - \mathcal{L}\{\dot{V}_{c2}\}
\]

or

\[
\frac{V_o(s)}{d(s)} = \frac{V_{c1}(s)}{d(s)} - \frac{V_{c2}(s)}{d(s)} = \frac{V_{c1}(s)}{d(s)} + \frac{V_{c2}(s)}{d(s)}
\]

According to equation (4.12), obtained for a single boost converter,

\[
\frac{V_{c1}(s)}{d(s)} = G_{vd}(s, D) = \frac{V_s}{(1-D)^2} \cdot \frac{1-sL_s/R}{1+sL_s/R+s^2L_sC}
\]

and
\[
\frac{V_{e2}}{(-d)}(s) = G_{sd}(s,D') = \frac{V_s}{(1-D')^2} \cdot \frac{1-sL_e'/R}{1+sL_e'/R+s^2L_e'C}
\]

Hence for the converter of Fig 4.3

\[
\frac{V_o(s)}{d} = \frac{V_s}{(1-D)^2} \cdot \frac{1-sL_e/R}{1+sL_e/R+s^2L_eC} + \frac{V_s}{(1-D')^2} \cdot \frac{1-sL_e'/R}{1+sL_e'/R+s^2L_e'C}
\]

where:

\[
L_e = \frac{L}{(1-D)^2} \quad L_e' = \frac{L}{(1-D')^2}
\]

When \( D = D' = 0.5 \), \( V_o = V_{e1} - V_{e2} = 0 \), so that \( D = D' = 0.5 \) is set as the base value, and \( d = d - 0.5 \).

thus,

\[
\frac{V_o(s)}{d} = 8V_s \cdot \frac{1-4L/Rs}{1+4L/Rs+4LCs^2}
\] (4.13)

4.5 EQUIVALENT CIRCUIT MODEL FOR A BOOST CONVERTER

As mentioned earlier, the State-Space Averaging method enables an equivalent circuit model to be developed for a converter, which explicitly explains the circuit operation and provides a deeper understanding of its behaviour. The 4-quadrant converter is derived from two boost converters and, from equations (4.12) and (4.13), it follows that the dynamic properties of the 4-quadrant converter are fundamentally the same as those of the boost converter. Only the boost converter is therefore discussed below, but the results obtained may be readily extended to the 4-quadrant converter.

The two switching conditions for the time intervals \( t_1 \) and \( t_2 \) for the converter are shown in Fig 4.2 and, from these, the equivalent circuit of Fig 4.4(a) may be drawn, in which
\(d(t)=1\) indicates that the switch closed and \(d(t)=0\) indicates this switch open.

Using the averaging method described in section 4.3, gives

\[
\begin{bmatrix}
\frac{dI_L}{dt} \\
\frac{dV_o}{dt}
\end{bmatrix} = \begin{bmatrix}
0 & -\frac{d'}{L} \\
\frac{d'}{c} & -\frac{1}{RC}
\end{bmatrix} \begin{bmatrix}
I_L \\
V_o
\end{bmatrix} + \begin{bmatrix}
\frac{1}{L} \\
0
\end{bmatrix} V_s
\]

(4.14)

The equivalent circuit of Fig 4.4(b) may be synthesized from equation (4.14), which in turn becomes Fig 4.4(c) for the steady-state condition \((d=D)\). If the dynamic response \((d=D+d)\) is considered, as discussed in section 4.3, then

\[
\begin{bmatrix}
\frac{dI_L}{dt} \\
\frac{dV_o}{dt}
\end{bmatrix} = (A_1-A_2)dX + A\bar{X} + \bar{B}V_s
\]

(4.15)

Based on equation (4.15), the equivalent circuits shown in Fig 4.4(d) and Fig 4.4(e) may be derived. The two parts of the circuit of Fig 4.4(e) can be seen respectively as the primary and secondary sides of a special 'transformer', which are related through the primary current and secondary voltage. Referring the secondary to the primary side in the familiar way gives the single unified equivalent circuits shown in Fig 4.4(f) and Fig 4.4(g), where the voltage source \(e(s)\) is defined as

\[
e(s) = \frac{\hat{\alpha} I_L}{D^{'2}sL}
\]
and for steady state condition

\[ I_l = \frac{V_o}{D'R} \]

thus

\[ e(s) = \frac{\partial}{\partial s} \frac{V_o}{D'R} sL \]

An extra voltage source \( e'(s) \) is thus generated in the input side, in addition to the original voltage source \( V_o/D' \) where

\[ e'(s) = \frac{\partial}{\partial s} V_o - e(s) \]

\[ = \frac{\partial}{\partial s} V_o \left( 1 - \frac{1}{D'^2 R sL} \right) \]  
(4.16)

4.6 DISCUSSION

4.6.1 FIRST-ORDER RIGHT HALF-PLANE ZERO

It was shown in section 4.5 that the development of a unified equivalent circuit for a boost converter created an equivalent power source \( e'(s) \), which contains the first-order right half-plane zero, evident in equation (4.16). This zero arises because the LC link in the converter is broken by a switch such that the effective parameters of the LC filter are a function of the duty cycle. This is shown in the small-signal circuit model of Fig 4.4(f) by a controlled current source to ground between the inductance and capacitance of the effective filter.

This right half-plane zero means that, to increase the output voltage \( V_o \), the duty cycle \( d \) has also to increase. An increase of \( d \) means however that the inductor spends less
time connected to the capacitor. The increase in duty cycle could thus be construed as a tendency to oppose the increase of $V_o$, and hence the phase lag characteristic of a right half-plane zero. In some other converters, such as the buck converter, the filter is not effected by any switches during the whole period $T_o$, and no right half-plane zero is produced.

4.6.2 INSIGHT INTO THE MATRICES $A_1$, $A_2$, $B_1$, $B_2$, $C_1$, $C_2$

a) $A_1$ and $A_2$

The fact that $A_1$ and $A_2$ are different shows that two distinct switching conditions exist for the converter, one for the period $(0-dT)$ and the other for $(dT-T)$.

b) $B_1$ and $B_2$

The condition $B_1 = B_2$ (such as in a boost converter) indicates that there is no pulsation in the input current (the input current from the power supply is always continuous), whereas if $B_1 \neq B_2$ (such as in buck converter), there is a pulsation in the input current.

c) $C_1$ and $C_2$

The condition $C_1 = C_2$ shows the continuity of output current, while $C_1 \neq C_2$ means that there is a pulsation in the output current. As far as the 4-quadrant converter is concerned, there is no current pulsation in either the input or the output. Therefore $B_1$ always equals $B_2$ and $C_1$ always equals $C_2$. 
Fig 4.1 Switched-mode Regulator
Fig 4.2 Two Switching States For Boost Converter

(a) Interval $t_1$
(b) Interval $t_2$
Fig 4.3 4-Quadrant DC-DC Converter
Fig 4.4 Development Of Single Unified Equivalent Circuit for Boost Converter
Fig 4.4 Development Of Single Unified Equivalent Circuit For Boost Converter
CHAPTER 5 SIMULATION

The design and development of an efficient and economic drive requires the accurate prediction of both its steady-state and transient performance and, at the design stage, computer simulation provides a powerful tool for this purpose. The effect of parameter changes are easily studied, and any undesirable features of the performance corrected, without the complication and cost that are required in a practical circuit.

Mathematical models for the boost converter and the 4-quadrant converter were developed in chapter 4, in the form of s-domain transfer functions. These unified models, which provide information on the dynamic properties of the circuit, such as stability and transient response, are very useful when designing closed-loop control systems. They are however unsuitable for determining the behaviour of the individual components, and for indicating the voltage and current waveforms at different points in the circuit. Due to this difficulty, a mathematical model was developed for the converter in the form of a set of differential equations, which can be solved using a 4th-order Runge-Kutta numerical integration technique.

This chapter first examines the performance of a boost converter, after which a model of the 4-quadrant DC-to-DC converter is developed. Finally, a 2-loop speed/current controlled converter-fed DC drive system is simulated.

5.1 4TH-ORDER RUNGE-KUTTA NUMERICAL INTEGRATION METHOD

Due to its high accuracy, the 4th-order Runge-Kutta method [5] is widely used in the computer solution of systems of
linear and non-linear differential equations. The general form of such a system may be written in the state-variable form [5]

\[
\begin{bmatrix}
\dot{y}_1 \\
\dot{y}_2 \\
\vdots \\
\dot{y}_m
\end{bmatrix} =
\begin{bmatrix}
\alpha_{11} & \alpha_{12} & \cdots & \alpha_{1m} \\
\alpha_{21} & \alpha_{22} & \cdots & \alpha_{2m} \\
\vdots & \vdots & \ddots & \vdots \\
\alpha_{m1} & \alpha_{m2} & \cdots & \alpha_{mm}
\end{bmatrix}
\begin{bmatrix}
y_1 \\
y_2 \\
\vdots \\
y_m
\end{bmatrix} +
\begin{bmatrix}
b_1 \\
b_2 \\
\vdots \\
b_m
\end{bmatrix}
\]  

(5.1)

where

\[y_m = f_m(t) \quad \dot{y}_m = \frac{df_m(t)}{dt}\]

Equation (5.1) may be written in the abbreviated form

\[
\dot{Y} = AY + B
\]  

(5.2)

The Runge-Kutta solution [5] for equation (5.2) is then

\[
Y_{(n+1)} = Y_{(n)} + \frac{1}{6}(\overline{K}_{(1)} + 2\overline{K}_{(2)} + 2\overline{K}_{(3)} + \overline{K}_{(4)})
\]  

(5.3)

Where  

- \( h \) is the integration step-length
- \( Y_{(n)} \) and \( Y_{(n+1)} \) are respectively the vectors of state variables at the beginning and end of an integration step

\[
\overline{K}_{(1)} = h[AY_{(n)} + B]
\]

\[
\overline{K}_{(2)} = h\left[ A\left(Y_{(n)} + \frac{1}{2}\overline{K}_{(1)} \right) + B \right]
\]

\[
\overline{K}_{(3)} = h\left[ A\left(Y_{(n)} + \frac{1}{2}\overline{K}_{(2)} \right) + B \right]
\]
The equations above allow \( Y_{(n+1)} \) to be calculated from equation (5.3).

5.2 BOOST CONVERTER SIMULATION

A 28/180V boost converter supplying a rated load current of 5A was simulated, using the parameters derived in the next section.

5.2.1 PARAMETER DETERMINATION

Assuming that circuit resistance in the converter of Fig 5.1 may be neglected, energy transfer considerations define the following relations

\[
\frac{1}{2}V_s I_m t_1 = \frac{1}{2}LI_m^2 \tag{5.4}
\]
\[
\frac{1}{2}LI_m^2 = V_o I_o t_1 \tag{5.5}
\]

where \( I_m \) is the peak inductor current.

\( t_1 \) and \( t_2 \) are respectively the times for which switch \( S \) is closed and open.

From equations (5.4) and (5.5)

\[
\frac{1}{2}V_s I_m = V_o I_o \tag{5.6}
\]

Substituting the rated conditions into equation (5.6) gives the peak inductor current as

\[ I_m = 64A \]
The voltage ratio follows from equation (3.7) as

\[ \frac{180}{28} = \frac{1}{1 - D} = 6.4 \]

and therefore

\[ D = 0.84 \]

With a switching period \( T_s \) of 25\( \mu \)s

\[ t_1 = DT_s = 21\mu s \]

and from equation (5.4),

\[ L = 9.2\mu H \]

From energy transfer consideration,

\[ \frac{1}{2}C\left(V_o + \frac{1}{2}\Delta V\right)^2 - \frac{1}{2}C\left(V_o - \frac{1}{2}\Delta V\right)^2 = V_o I_o t_1 \]

then

\[ \Delta V C = I_o t_1 \]

(5.7)

For a required voltage ripple of \( \pm 5\% \) of \( V_o \),

\[ \Delta V = 18V \]

so that from equation (5.7)

\[ C = 5.8\mu F \]
5.2.2 SYSTEM EQUATIONS

The two circuit topologies which relate to the closed and open switch conditions of the boost converter are shown in Fig 5.2. A mathematical model in the form of a set of differential equations may be defined for each circuit as follows,

Switch closed (see Fig 5.2(a))

\[
\frac{dI_l}{dt} = -\frac{R_1}{L} I_l + \frac{V_o}{L}
\]

and

\[
\frac{dV_o}{dt} = -\frac{1}{CR} V_o
\]

In matrix form

\[
\begin{bmatrix}
I_l \\
V_o
\end{bmatrix} = \begin{bmatrix}
-\frac{R_1}{L} & 0 \\
0 & -\frac{1}{CR}
\end{bmatrix} \begin{bmatrix}
I_l \\
V_o
\end{bmatrix} + \begin{bmatrix}
\frac{V_o}{L} \\
0
\end{bmatrix}
\]

or

\[\dot{Y} = A_1 Y + B_1\]

Switch open (see Fig 5.2(b))

\[
\frac{dI_l}{dt} = -\frac{R_1}{L} I_l - \frac{V_o}{L} + \frac{V_z}{L}
\]

and

\[
\frac{dV_o}{dt} = \frac{I_l}{C} - \frac{1}{CR} V_o
\]

In matrix form
\[
\begin{bmatrix}
I_L \\
V_o
\end{bmatrix} = \begin{bmatrix}
\frac{-R_1}{L} & -1 \\
\frac{1}{C} & \frac{-1}{CR}
\end{bmatrix}\begin{bmatrix}
I_L \\
V_o
\end{bmatrix} + \begin{bmatrix}
\frac{V_s}{L} \\
0
\end{bmatrix}
\]

or \[ \dot{Y} = A_2Y + B_2 \]

where the load resistance

\[ R = \frac{V_o}{I_o} = 36\Omega \]

and the resistance of the inductor

\[ R_1 = 0.1\Omega \]

5.2.3 PROGRAM DESCRIPTION AND SIMULATION RESULTS

A flowchart for the program is given in Fig 5.3. The program commences by reading the input data, after which it checks the switch status and chooses the relevant equivalent circuit equations, which are then integrated numerically. The values obtained for \( I_L \) and \( V_o \) are stored in a plotting file. The elapsed time \( t \) is incremented by one step \( h \) and compared with the simulation time \( T \). If the incremented time is less than \( T \) the program checks the switch status and repeats the above procedure. If it is greater than \( T \), the program is terminated. Typical simulation results based on the parameters obtained in section 5.2.1 are shown in Fig 5.4.
5.3 SIMULATION OF A 4-QUADRANT DC/DC CONVERTER

In this section a mathematical model is developed for a 4-quadrant DC-to-DC converter, as shown in Fig 5.5, operating in both open-loop and closed-loop. The converter parameters are derived in the following section.

5.3.1 OPEN-LOOP PERFORMANCE
5.3.1.1 PARAMETER DETERMINATION

Circuit component values are again calculated for the values of maximum output voltage and current and operating frequency given in section 5.2.1.

Thus from equation (3.13)

\[ \frac{V_o}{V_s} = \frac{2D-1}{(1-D)D} = \frac{180}{28} \]

it follows that

\[ D = 0.87 \quad \text{and} \quad t_1 = 21.7\mu s \]

From equation (5.6)

\[ \frac{1}{2}V_s I_{1m} = V_{cl} I_o \]

where \( I_{1m} \) is the peak value of \( I_{\text{in}} \)

and from equation (3.7)

\[ V_{cl} = \frac{V_s}{1-D} = \frac{28}{1-0.87} = 215V \]
Thus

\[ I_o = 5A, \quad V_s = 28V \]

and

\[ I_{im} = 76.8A, \quad L_1 = 7.9\mu F \]

Assuming that a 10% output voltage ripple is required, equation (5.7) gives

\[ C_1 = \frac{I_o I_1}{\Delta V} = 5.05\mu F \]

Similarly, \( L_2 \) and \( C_2 \) may be calculated from considerations of the maximum reverse output voltage and current, which gives the same values as for \( L_1 \) and \( C_1 \) due to the symmetry of the circuit. The load resistance is again 36\( \Omega \).

### 5.3.1.2 BASIC EQUATIONS

In a manner similar to that developed for the boost converter, the two circuit topologies of Fig 5.6(a) and (b) may be defined for the different states of switches in the converter. The two sets of equations relating to these topologies are

a) Switches \( S_1 \) and \( S_3 \) of Fig 5.5 closed, \( S_2 \) and \( S_4 \) open,

\[
\begin{bmatrix}
I_{11} \\
I_{12} \\
V_{c1} \\
V_{c2}
\end{bmatrix} =
\begin{bmatrix}
\frac{-R_1}{L} & 0 & 0 & 0 \\
0 & \frac{-R_1}{L} & 0 & -\frac{1}{L} \\
0 & 0 & \frac{-1}{RC} & \frac{1}{RC} \\
0 & \frac{1}{C} & \frac{1}{RC} & \frac{1}{RC}
\end{bmatrix}
\begin{bmatrix}
I_{11} \\
I_{12} \\
V_{c1} \\
V_{c2}
\end{bmatrix} +
\begin{bmatrix}
\frac{V_s}{L} \\
\frac{V_s}{L} \\
0 \\
0
\end{bmatrix}
\]
or \[ y = A_1 y + B_1 \]

b) Switches \( S_2 \) and \( S_4 \) closed, \( S_1 \) and \( S_3 \) open,

\[
\begin{bmatrix}
    \frac{1}{L} & 0 & -\frac{1}{L} & 0 \\
    0 & \frac{R_1}{L} & 0 & 0 \\
    \frac{1}{C} & 0 & -\frac{1}{RC} & \frac{1}{RC} \\
    0 & 0 & \frac{1}{RC} & -\frac{1}{RC}
\end{bmatrix}
\begin{bmatrix}
    I_{L1} \\
    I_{L2} \\
    V_{c1} \\
    V_{c2}
\end{bmatrix}
+
\begin{bmatrix}
    V_s \\
    V_s \\
    V_s \\
    0
\end{bmatrix} \frac{L}{L}
\]

or \[ y = A_2 y + B_2 \]

5.3.1.3 RESULTS

A program developed in a similar manner to that described in section 5.2.3, was used to determine the voltage and current waveforms at various points of the converter circuit, as shown in Fig 5.7(a) to (c). It is evident that, when \( D \) is greater than 50\%, the converter output voltage is positive and when \( D \) is less than 50\%, it is negative. With \( D=50\% \) the voltage is zero.

5.3.2 CLOSED-LOOP 4-QUADRANT CONVERTER-DC MOTOR DRIVE

The 4-quadrant converter-DC motor drive with speed and current control loops is shown in Fig 5.8. Simulation of
the circuit was used to examine the change of inductor current and output voltage of the converter, as well as the response of the armature current and speed of the motor, following a change in the speed command input.

5.3.2.1 SYSTEM EQUATIONS

a) Switches $S_1$ and $S_3$ closed, $S_2$ and $S_4$ open

$$
\begin{bmatrix}
    -\frac{R_1}{L} & 0 & 0 & 0 & 0 & 0 \\
    0 & -\frac{R_1}{L} & 0 & -\frac{1}{L} & 0 & 0 \\
    0 & 0 & 0 & 0 & -\frac{1}{C} & 0 \\
    0 & \frac{1}{C} & 0 & 0 & \frac{1}{C} & 0 \\
    0 & 0 & \frac{1}{L_a} & -\frac{1}{L_a} & -\frac{R_a}{L_a} & -\frac{K_b}{L_a} \\
    0 & 0 & 0 & 0 & K_b & -\frac{K'_{f}}{J} \\
\end{bmatrix}\begin{bmatrix}
    \dot{I}_{t1} \\
    \dot{I}_{t2} \\
    V_{e1} \\
    V_{e2} \\
    I_a \\
    \dot{\omega}
\end{bmatrix} = \begin{bmatrix}
    \dot{V}_s \\
    \dot{V}_s \\
    V_{e1} \\
    V_{e2} \\
    I_a \\
    \dot{\omega}
\end{bmatrix} + \begin{bmatrix}
    0 \\
    0 \\
    0 \\
    0 \\
    0 \\
    0
\end{bmatrix}
$$

or

$$\dot{Y} = A_1 Y + B_1$$

where

$$K_b = K_a \phi, \quad K'_{f} = K_f + \frac{K'^2}{R_0}$$

b) Switches $S_2$ and $S_4$ closed, $S_1$ and $S_3$ open
The DC motor parameters were measured as

\( K_b = 1.06 \text{Vs/rad} \quad K_{f_1} = 0.95 \times 10^{-3} \text{Nms/rad} \)

\( L_a = 180.1 \text{mH} \quad R_a = 26 \Omega \quad J_1 = 5 \times 10^{-3} \text{ kgm}^2 \)

and for the DC generator

\( K' = 1.08 \text{Vs/rad} \quad K_{f_2} = 5.56 \times 10^{-3} \text{Nms/rad} \)

\( J_2 = 0.0139 \text{kgm}^2 \quad R_g = 100 \Omega \)

Thus, the overall Motor-Generator mechanical constants are,

\( K_f = K_{f_1} + K_{f_2} = 6.51 \times 10^{-3} \text{Nms/rad} \)

\( J = J_1 + J_2 = 0.0189 \text{ kgm}^2 \)
5.3.2.2 CLOSED-LOOP EQUATIONS

The speed loop of Fig 5.8 contains a speed controller, for which

\[ I_n = K_p \Delta \omega_n + K_d \frac{\Delta \omega_n - \Delta \omega_{n-1}}{\Delta T} + K_i \sum_{n=0}^{m} \Delta \omega_n \]

where \( K_p, K_d \) and \( K_i \) are constants, \( \Delta T \) is the sampling time and \( \Delta \omega_n \) and \( \Delta \omega_{n-1} \) are respectively the speed error at nth and (n-1)th sampling time.

The output of the speed loop \( I_n \) forms the reference signal to the current loop. The current loop contains a PI controller for which

\[ V_n = K_p' \Delta I_n + K_i' \sum_{n=0}^{m} \Delta I_n \]

where \( K_p' \) and \( K_i' \) are constants, \( \Delta I_n \) the current error and \( V_n \) the output from the current loop which determines the duty cycle of the converter switches.

5.3.2.3 PROGRAM DESCRIPTION AND RESULTS

Fig 5.9 shows a program flowchart for simulating the complete servo system. The details are self explanatory, except for the PID controller subroutine which determines the required switch duty cycle based on the demand speed and feedback current and speed.

Simulated results obtained from the program are shown in Figs 5.10(a) to (g).

Fig 5.10(a) shows the no-load response to a change in
demand speed from zero to maximum forward speed. The armature current is initially high as the motor accelerates towards the demand speed, after which it reduces to the value required to maintain the demand speed. A slight overshoot in speed is evident.

Fig 5.10(b) shows the speed response to a change in demand speed from standstill to full reverse speed, and Fig 5.10(c) the speed response to a change in demand from full forward to full reverse speed. In the latter case, both the output voltage and armature current can be seen to be reversed, to force a rapid reversal of the motor speed.

Figs 5.10(d) and (e) respectively show the response to a change in demand from full forward speed to zero and from full reverse speed to zero. Once again the responses are rapid, with very little overshoot.

Fig 5.10(f) shows the response when an electrical load of $R_g = 100\Omega$ is applied suddenly at the generator terminals. The sudden increase in load causes an initial fall in the motor speed, followed by a rapid recovery to the demand value.

Fig 5.10(g) shows the system response when the load is suddenly removed from the generator. In this case, the speed suddenly increases, but soon recovers to the demand value as the closed loop control senses and corrects the error. It is evident that the drive has a good stability against load variation.
Fig 5.1 Ideal Boost Converter
Fig 5.2 Two Switching States Of Boost Converter
(a) Interval $t_1$   (b) Interval $t_2$
Switch Closed       Switch Open
START

OPEN FILES FOR PLOTTING

INPUT \( V_s \), \( t_1 \), \( t_2 \)
AND MATRIX A

INPUT STEP SIZE \( h \)
AND FINAL TIME \( T \)

SET INITIAL VALUE
OF I AND Vo

SET A=A2

CALL RUNGE-KUTTA
INTEGRATION ROUTINE

OUTPUT \( I_L \) AND \( V_o \)

\( t=t+h \)

NO

\( t > T \)?

YES

END

Fig 5.3 Flowchart For Simulation Of Boost Converter
Fig 5.4 Inductor Current And Output Voltage
Of Boost Converter With D=84%
Fig 5.5 4-Quadrant DC-DC Converter

Fig 5.6 Two Switching States Of 4-Quadrant DC-DC Converter
(a) $S_1, S_3$ Closed & $S_2, S_4$ Open
(b) $S_1, S_3$ Open & $S_2, S_4$ Closed
Fig 5.7(a) Current and Voltage Waveforms for 4-quadrant Converter with D=87%
Fig 5.7(b) Current And Voltage Waveforms For 4-quadrant Converter With D=13%
Fig 5.7(c) Current And Voltage Waveforms For 4-quadrant Converter With D=50%
Fig 5.8 Closed-Loop Controlled DC Drive
Fig 5.9 Flowchart For Closed-loop Controlled DC Drive
Fig 5.10(a) System Response From Zero To Forward Full Speed (No Load)
Fig 5.10(b) System Response From Zero To Reverse Full Speed (No Load)
Fig 5.10(c) System Response From Forward To Reverse Full Speed (No Load)
Fig 5.10(d) System Response From Forward Full Speed To Zero (No Load)
Fig 5.10(e) System Response From Reverse Full Speed To Zero (No Load)
Fig 5.10(f) System Response To Sudden Application Of 100Ω Load At Generator Terminals
Fig 5.10(g) System Response To Sudden Removal Of 100Ω Load From Generator Terminals
CHAPTER 6 POWER CIRCUIT DESIGN

This chapter describes the design and construction of the prototype 1.2kW 4-quadrant DC-to-DC converter shown in Fig 6.1, with a supply voltage of 28V DC and an output voltage variable between -180V to +180V.

A description is given of how the optimal switching frequency of the converter was obtained from a detailed computer simulation. This is followed by an explanation of the inductor design and the core selection, together with the principles of the Mos-Gated bimos switch. Since the converter operation relies on both high-power and high-frequency switching, the circuit layout is very important, and very careful arrangement of circuit ground and component connections is necessary. Over-current protection is provided by means of a Hall-effect current sensor, while RCD-snubbers limit the rate-of-rise of voltage across the power devices.

6.1 SWITCH DESIGN

The theoretical results presented in chapter 5 show that the peak voltage across the switches may reach 250V, while section 6.3 will show that the peak current is 55A. Many transistors are capable of handling this power level at a switching rate of 40kHz, which is the optimal frequency obtained in section 6.2. However, in order to obtain an output of 180V, consideration of equation (3.13) shows that

\[
\frac{V_o}{V_s} = \frac{2D-1}{D(D-1)} \frac{180}{28}
\]

or \( D = 0.87 \)
so that $t_1 = DT = 21.75\mu s$, $t_2 = D'T = 3.25\mu s$ and $S_2$ has only about $3\mu s$ to switch on and off. In practice it is necessary to consider parasitic circuit resistance, in which case $D$ may need to be increased to as high a value as 0.94 to provide the required 180V output, as shown in Fig 6.2. In this case $S_2$ must switch on and off within about $1.25\mu s$, and this switching rate at the required power level is difficult to achieve using either a single mosfet or bipolar transistor. It can however be easily achieved by combining two mosfets and one bipolar transistor, to form the Mos-Gated bimos switch shown in Fig 6.3.

6.1.1 CHARACTERISTICS OF POWER MOSFET AND BIPOLAR TRANSISTOR

A complete understanding of the operation and limitations of mosfets and bipolar transistors is essential for the design of a Mos-Gated bimos switch. Some features of mosfet operation are more desirable than those of bipolar transistors, while the reverse is also true [6]. Combining the advantages of the two technologies, while eliminating their undesirable features, produces a very useful switch.

6.1.1.1 ADVANTAGES OF BIPOLAR TRANSISTORS

a) Conductivity Modulation: For a given chip area and the same working voltage capability, the bipolar transistor has lower saturation conduction losses than a mosfet. Conductivity modulation enables the fabrication of very high voltage devices ($V_{CBO}$ up to 2kV) with reasonably low on-state losses. For working voltages above 600V, the disparity between bipolar and mosfet losses is large.

b) Lower Unit Cost: A bipolar transistor has a better silicon utilization in terms of conductivity per unit area, and thus a lower unit cost than a mosfet of comparable rating.
c) **Ruggedness**: Most power switching bipolar transistors are reasonably rugged.

d) **High Voltage Capability**: Since the bipolar transistor has low on-state losses at high voltage, it is well suited for applications in which a voltage capability above 600V is required.

### 6.1.1.2 DISADVANTAGES OF BIPOLAR TRANSISTORS

a) **Storage Time**: Since the bipolar transistor is a minority carrier device, the storage time during which the minority carriers are swept out of the base region is appreciable (typically greater than 1.0 μs). This time represents one of the main limitations imposed on the operating frequency.

b) **Safe Operating Area (SOA)**: Unfortunately a bipolar power transistor features two secondary-breakdown mechanisms, which are a potential hazard during both forward and reverse bias operation. Forward bias secondary breakdown is primarily the net result of a rapid and severe fall in gain, with increased collector current beyond a value usually referred to as \( I_{c(sat)} \).

Reverse-bias secondary breakdown is the main limitation imposed on the bipolar safe operating area. It is due to avalanche injection occurring at the collector \( n-n^+ \) junction when the transistor is subjected to a large collector-emitter voltage. The predominant feature is the transition to a low-voltage high-current mode, occurring at some critical point in the collector characteristic [7]. Due to this, bipolar transistors often require extra circuits to ensure that they operate within the confines of the SOA, particularly during turn-off.
c) **Switching Speed:** The bipolar transistor has a relatively low switching speed, as the result of the finite time required by the drive circuit to deliver charge to and recover charge from its base. Quite complicated base-drive circuits are consequently required for high-frequency operation, which may considerably increase the total cost.

### 6.1.1.3 ADVANTAGES OF POWER MOSFETS

a) **Switching Speed And Operating Frequency:** The power mosfet can, regardless of the circuit configuration, switch at frequencies at least one order of magnitude higher than those achievable by even the fastest bipolar transistor. The reason is that, being a majority carrier device, the power mosfet does not suffer from long storage time limitations. A high switching speed is readily achievable with a relatively simple drive circuit, and this inevitably results in low switching losses.

b) **Simple Drive Circuit:** Since it is predominantly voltage driven, a mosfet may be controlled satisfactorily by any low impedance drive circuit. The resulting drive circuit simplicity makes the use of mosfets very cost effective.

c) **Ruggedness:** The complete absence of secondary breakdown means that no bipolar transistor of equal chip size can approach the mosfet's overload capability.

d) **Thermal Stability:** When fully enhanced, the mosfet has a positive temperature coefficient of resistance. The switching time, in turn, does not display any temperature dependency. These two factors provide the mosfet with excellent thermal stability and eliminate the need for ballast circuits when devices are parallelled.
6.1.1.4 DISADVANTAGES OF POWER MOSFETS

a) On-state resistance and Losses: Due to the inability of the mosfet to modulate its conductivity, the device has higher static conduction losses than a comparable bipolar transistor. The exponential increase in on-state losses with increasing voltage capability limits the mosfets useful working voltage capability to about 600V.

b) Unit Cost: A relatively poor silicon utilization makes the unit cost of the mosfet higher than that of a comparable bipolar transistor.

6.1.2 MOS-GATED BIMOS TRANSISTOR

A comparison between the characteristics of bipolar transistors and mosfets shows that the mosfet has advantages in drive circuit simplicity, switching speed, and secondary breakdown ruggedness. It suffers however from the drawback that, at higher power level, its operation is restricted by its relative high on-state resistance. These considerations indicate that a combination of the two technologies, which overcomes the disadvantages of both devices, will prove to be attractive. The Mos-Gated bimos switch is one such combination [8], in which two FETs and one BJT are combined to form a 3-terminal device.

6.1.2.1 SWITCH CONFIGURATION

Fig 6.3 shows the circuit diagram for the Mos-Gated bipolar transistor, in which $Q_1$ is the main bipolar power transistor, $Q_2$ and $Q_3$ are power mosfets, and $D_2$ a high-speed varistor. The mosfet $Q_2$ is in a Darlington configuration with $Q_1$, and $Q_3$ is cascaded with $Q_1$. When the gate voltage is high both $Q_2$ and $Q_3$ conduct; $Q_1$ therefore also conducts and
the switch is on. When the gate voltage is low both $Q_2$ and $Q_3$ are turned off, which open-circuits the emitter of $Q_1$ and causes a high transient base discharge current almost equal to the collector current. This in turn considerably reduces the storage time, so that the switch turns off rapidly [9]. The varistor $D_z$ has two purposes: (a) to provide a reverse current path for the base of $Q_1$ at emitter-open turn-off, at the same time clamping the base terminal voltage at the varistor clamping voltage; and (b) to provide a forward current path for discharging the $Q_2$ gate capacitance at turn-off.

The voltage rating of $Q_2$ is the same as that of $Q_1$, while its current rating corresponds to the base current of $Q_1$. Mosfet $Q_3$ conducts the same current as $Q_1$ but is a low-voltage device (typically less than 50V), to make use of the low on-state resistance of low voltage mosfets. Varistor $D_z$ must be capable of dissipating the high transient power during turn-off and it requires a breakdown voltage lower than the maximum drain-source voltage of $Q_3$.

6.1.2.2 ADVANTAGES OF THE MOS-GATED BIPOLAR POWER TRANSISTOR

a) The switch is not subject to reverse bias secondary breakdown (RBSB) due, in the case of a bipolar transistor, to emitter current crowding when turning off an inductive load. Since $Q_1$ is turned off by open-circuiting the emitter, collector current is extracted from the base terminal and emitter current constriction does not occur. Consequently, secondary breakdown is avoided.

b) The drive circuit is simple, due to the simple voltage drive for the mosfet.
c) Switching speed is very fast, and is limited primarily by the speed of $Q_1$. However, $Q_1$ is provided inherently with the nearly ideal base-drive current waveform shown in Fig 6.4. A large reverse base current, almost equal to the collector current, is withdrawn from the base and the excessive carriers in the base region are swept out rapidly by the large reverse base current. The storage time and fall time are therefore substantially reduced and $Q_1$ can be switched very rapidly.

d) The on-state resistance is low, since it is due to the low on-state resistances of the bipolar transistor $Q_1$ and the low voltage mosfet $Q_3$.

6.1.2.3 PRACTICAL CONSIDERATION

A 60A, 500V Mos-Gated bimos switch was constructed using the following devices

$Q_1$: BUS14 with $V_{CEO}=400V$, $V_{CBO}=850V$, $I_e=30A$, $I_{CM}=50A$.
$Q_2$: IRFP450 with $V_{DS}=500V$, $I_d=14A$, $I_{DM}=56A$
$Q_3$: IRFZ42 with $V_{DS}=50V$, $I_d=35A$, $I_{DM}=160A$ and an extremely low on-state resistance $R_{on}=0.035 \Omega$
$D_x$: high speed transient voltage suppressor IN6277 with a reverse stand-off voltage $V_Z=14.5V$.

Practical considerations inherent in the design of the switch were

a) **Paralleling**: To achieve the required current rating, two devices were paralleled for both $Q_1$ and $Q_3$ and, in this respect, two options exist as shown in Figs 6.5(a) and (b). Due to their positive temperature coefficient, when mosfets are paralleled the device with the lower on-state resistance will carry a higher current with a correspondingly larger $P_{loss}$. This causes the junction temperature and the
on-state resistance to increase and the current is thereby reduced. Due to this self-adjusting property, the connection shown in Fig 6.5(b) was selected to achieve better current sharing in both the mosfets and the bipolar transistors.

b) **Varistor**: The main advantage of a varistor over a zener diode is that it is voltage rather than current dependent and it is able to withstand high transient voltage spikes. The varistor impedance changes from a very high standby value to a very low conducting value, thus clamping the transient voltage to a protective level. The excess energy associated with the high voltage pulse is first absorbed and then dissipated by the varistor.

c) **Stray Inductance**: Since the switch is operating at 40kHz and a peak current of 50A, any stray lead inductance will generate high-voltage spikes which put severe stress on the devices. To minimize lead length, all the components of each switch are assembled on one heatsink.

### 6.2 Optimum Frequency

It is common to use a high switching frequency in DC-to-DC converters, to minimize the weight, cost and size of inductors and capacitors. Although the inductor losses may fall, due to the reduced physical size, the transistor and diode switching losses will however increase with frequency. At a certain frequency the switching loss becomes the dominant component of the total loss, and any further increase in frequency brings about a significant decrease in efficiency. Furthermore, above a certain frequency the equivalent-series-resistance (ESR) of the capacitor exceeds its reactance and no further reduction in capacitor size or
cost is possible. This occurs normally in the range 1 to 50 kHz [10], depending on the quality of the capacitor in terms of its ESR.

A computer-aided-design study was performed to determine an optimum switching frequency which keeps the inductor size small while maintaining a high overall converter efficiency. The inductance and capacitance were calculated for a given frequency and the various power losses in the circuit were determined for that frequency. The process was repeated over a range of frequencies, and the results enabled the optimum frequency to be established.

6.2.1 INDUCTANCE AND CAPACITANCE CALCULATIONS

Assuming a constant load current $I_L$ and a linear increase in supply current from zero to $I_m$ during the turn-on time $t_1$, it follows from equations (5.4) and (5.5) that

$$\frac{1}{2}V_s I_m t_1 = \frac{1}{2} L I_m^2$$

and

$$\frac{1}{2} L I_m^2 = V_o I_o t_1$$

so that

$$L = \frac{2V_o I_o t_1}{I_m^2} = \frac{2P_{out} t_1}{I_m^2}$$

From equation (5.6)

$$I_m = \frac{2 \cdot P_{out}}{V_s}$$
Since \[ t_1 = D T = \frac{D}{f} \]

then \[ L = \frac{D V_s^2}{2 p_{out} f} \] \hspace{1cm} (6.1)

and from equation (5.7)

\[ C = \frac{I_o t_1}{\Delta V} = \frac{I_o D_{\text{max}}}{\Delta V} \frac{1}{f} \] \hspace{1cm} (6.2)

The inductance and capacitance at any given frequency may be calculated using equations (6.1) and (6.2).

6.2.2 POWER LOSSES

The converter power losses include switching and conduction losses associated with the power transistors, mosfets and diodes, together with the inductor losses.

6.2.2.1 SWITCHING LOSSES

Fig 6.6 shows switching current and voltage waveforms for the bimos switch described in section 6.1. The turn-on loss of the switch is

\[ P_{\text{swon}} = \frac{V_2 I_o t_{\text{swon}}}{2 T_s} = \frac{V_2 I_o t_{\text{swon}}}{2 f} \] \hspace{1cm} (6.3)

and the switch-off loss is

\[ P_{\text{swoff}} = \frac{V_2 I_o t_{\text{swoff}}}{2 T_s} = \frac{V_2 I_o t_{\text{swoff}}}{2 f} \] \hspace{1cm} (6.4)
where \( I_a \) and \( I_b \) are respectively the minimum and maximum inductor currents, which may be obtained from Table 3.2, \( t_{\text{swon}} \) and \( t_{\text{swf}} \) the turn-on time and the turn-off time, as obtained from the device specification.

The on-state power loss may be calculated from

\[
P_{\text{con}} = \frac{V_{\text{sat}} I_b t_1}{2 T_s} = D \cdot \frac{V_{\text{sat}} I_b}{2}
\]

(6.5)

6.2.2.2 Inductor Winding Losses

The inductor is formed by a number of turns of copper strip, in which various losses occur.

a) DC Loss \((P_{\text{dc}})\)

The DC loss in the winding resistance may be calculated from

\[
P_{\text{dc}} = \frac{1}{3} I_m^2 R_{\text{dc}}
\]

(6.6)

where the DC winding resistance is

\[
R_{\text{dc}} = \frac{l}{\rho s}
\]

b) Skin Effect Loss

Direct current is evenly distributed throughout the cross-section of the conductors, but skin effect causes
alternating current to crowd towards the surface of the conductor. This decreases the effective cross-sectional area and increases the effective resistance by [11]

\[ R_{ac} = \frac{4}{45} \left( \frac{b}{\delta} \right)^4 R_{dc} \]  

(6.7)

where the skin depth

\[ \delta = \sqrt{\frac{2}{\omega \sigma \mu_0}} \]

\[ \frac{1}{\sigma} = \rho = 1.7 \times 10^{-8} \]

and \( b \) = thickness of the copper strip

The total copper loss is therefore

\[ P_{ac} = \frac{1}{3} I_m^2 (R_{ac} + R_{dc}) \]  

(6.8)

6.2.2.3 DIODE LOSS

The power loss associated with a conducting diode is

\[ P_D = \frac{V_D I_m t_2}{2T_s} \]  

(6.9)

where \( V_D \) is the on-state diode voltage drop.
6.2.2.4 Efficiency And Component Optimization

Results provided by a computer program written to determine the variation of inductance, capacitance, losses and efficiency with frequency, are shown in Fig 6.7. It is evident that, at low frequency, the required inductance decreases rapidly as the frequency increases, and that the power loss also decreases due to the reduced winding loss. The efficiency reaches its peak value at about 40 kHz, after which the increasing switching loss starts to dominate the total loss, with a consequent drop in efficiency. Although the inductance still decreases with a further increase in frequency, this effect is relatively small.

Fig 6.7 shows that, to achieve the best compromise between high efficiency and low inductance, a switching frequency of 40kHz should be chosen for the converter.

6.3 INDUCTOR DESIGN

The value of the inductor L as calculated above is the minimum value \( L_{\text{min}} \) required to maintain continuous current operation, as indicated in Fig 6.8. For a chopping frequency of 40kHz, equation (6.1) gives \( L_{\text{min}} \) as 7\( \mu \)H, from which

\[
I_{m} = \frac{V_{s}}{L_{\text{min}}} t_{i} = 85.75A
\]

The semiconductor devices are subjected to severe stress at the maximum current of 86A, due to high-voltage spikes and high switching losses, and consequently a larger inductance than \( L_{\text{min}} \) is desirable. The average inductor current for this condition \( I_{av} = \frac{I_{m}}{2} = 43A \). Assuming a peak supply current of 55A the peak-to-peak current (\( \Delta I \)) is 24A,
as shown in Fig 6.8(a).
Hence,

\[ L = \frac{V_s}{\Delta I} t_1 = 25\, \mu H \]

### 6.3.1 CORE SELECTION

The current-handling capability of an inductor depends upon its core geometry, the number of turns, the operating frequency, the maximum core flux density and the core loss. A pair of ferrite cores (Type FX3750), with an air-gap between them, was selected on the basis of these requirements.

### 6.3.2 INDUCTOR CALCULATIONS

For the core shown in Fig 6.9 the diameter of the central leg is 17mm, and its effective cross-sectional area is

\[ A_t = \frac{17^2\pi}{4} = 227\, mm^2 \]

The rms current is

\[ I_{rms} = \sqrt{\frac{1}{T} \int_0^T \frac{l_m^2 t^2}{T^2} \, dt} = \frac{l_m}{\sqrt{3}} = 32\, A \]

The conductor current density \( J \) is

\[ J = \frac{NI_{rms}}{A_w} \]

where \( A_w \) is the effective cross-sectional area of the
coil and $N$ the number of turns. Since the maximum current density for copper strip when used in the present type of application is $20\text{A/mm}^2$, the minimum cross-sectional conductor area is

$$\rho b = \frac{A_w}{N} = \frac{I_{\text{rms}}}{J_{\text{max}}} = \frac{32}{20} = 1.6\text{mm}^2$$

(6.10)

where $\rho$ and $b$ are respectively the width and thickness of the copper strip. The thickness is kept as low as possible to reduce skin effect.

If $b=0.25\text{mm}$ the minimum width of the copper strip is $1.6/0.25=6.4\text{mm}$. Using a core window factor $K_w$ of 0.2 gives a width $\rho$ of 20mm.

The window area of a pair of EC cores $=(68-26)\times13=546\text{mm}^2$. The effective coil area is thus

$$A_w=546\times0.2=109\text{mm}^2$$

From equation (6.10), the number of turns $N$ is

$$N = \frac{A_w}{\rho b} = 21$$

and the airgap required for the inductor $L$ is [12]

$$g = \frac{N^2 \mu_0 A_i}{L k_i} = 5.0\text{mm}$$

Summarising the above results, the inductor design is:

$L=25\mu\text{H}, \ g=5\text{mm}, \ b=0.2\text{mm}, \ \rho=20\text{mm}, \ N=21$ turns
The working flux density of

\[ B = \frac{LI_{\text{rms}}}{NA_i} = 0.18T \]

is smaller than the value of 0.32T corresponding to the knee point of the magnetisation characteristic for the ferrite material.

6.3.3 FLUX FRINGING

In a gapped ferrite core, the flux crossing the airgap is not confined to a path having the same cross-section as the core but exists also in fringe fields around the airgap [13]. The effective airgap cross-sectional area is therefore larger than its physical dimensions and, as a result, the actual inductance exceeds that calculated using the physical dimensions. Since the cross-sectional areas in other parts of the core remains unchanged the fringing flux, which also goes through these areas, causes a higher flux density. It is therefore necessary to re-examine the flux density by including the effect of the fringing.

For the core chosen, the additional pole face areas labelled E and F in Fig 6.10(a) can be obtained according to the curves shown in Fig 6.10(b). The detail of the calculation is given in Appendix II, from which

\[ \text{area } E = 44.2\text{mm}^2 \]
\[ \text{area } F = 68.5\text{mm}^2 \]

the effective cross-sectional area of the central pole


\[ A'_i = 372.5 \text{mm}^2 \]

and the actual winding inductance is

\[ L' = (A'_i / A_i) L = 31.5 \mu H \]

The flux density in the core of

\[ B' = \frac{L' \times I_{\text{rms}}}{N \cdot A_i} = 0.23 T \]

is less than \( B_{\text{max}} \).

6.4 HEATSINKS

To ensure that the power semiconductor devices work within their safe operating area (SOA), an appropriate heatsink must be provided. By examining the power loss and heat dissipation within the device, the required heatsink thermal resistance to keep the junction temperature below the safe limit may be determined and the type and size of heatsinks may be chosen.

6.4.1 SAFE OPERATING AREA

The four limits to the SOA of a bipolar transistor, i.e. collector current limit, voltage limit, power and temperature and secondary breakdown, are all illustrated in Fig 6.11. Excess power dissipation causes a rise in the junction temperature which, in turn, causes irreversible chemical and metallurgical changes.
Fig 6.12 shows that the heat dissipated in the collector-base junction flows through the thermal resistance between the junction and the mounting base $R_{thj-mb}$.

The power dissipation in the junction is therefore

$$P = \frac{T_j - T_{mb}}{R_{thj-mb}}$$

and Fig 6.13 shows the relationship between the maximum power dissipation $P_{\text{max}}$ and the temperature of the mounting base. The maximum power is limited by either the maximum junction temperature $T_{j_{\text{max}}}$ or $\Delta T_{j-mb}(\text{max})$, which is defined by

$$\Delta T_{j-mb}(\text{max}) = T_{j_{\text{max}}} - T_{mbk}$$

where $T_{mbk}$ is the maximum value of $T_{mb}$ for which the power dissipation is large enough to cause the operating point to move outside the safe operating area.

For $T_{mb} > T_{mbk}$, $P_{\text{max}}$ is limited by the maximum junction temperature to

$$P_{\text{max}} = \frac{T_{j_{\text{max}}} - T_{mb}}{R_{thj-mb}} \quad (6.11)$$

For $T_{mb} \leq T_{mbk}$, the power dissipation has a fixed limit

$$P_{\text{max}} = \frac{\Delta T_{j-mb}(\text{max})}{R_{thj-mb}} \quad (6.12)$$
6.4.2 SWITCH POWER LOSSES

The full load current and voltage waveforms for the three devices IRFP450, IRFZ42 and BUS14 are shown in Fig 6.14. Calculation of the various power loss components is given in full in Appendix I, and the results are summarised below.

For IRFP450
\[
P_{\text{sun}} = 7.68\text{W} \\
P_{\text{swf}} = 4.84\text{W} \\
P_{\text{con}} = 24.31\text{W} \\
P_{\text{tot}} = P_{\text{swf}} + P_{\text{sun}} + P_{\text{con}} = 36.85\text{W} \quad (6.13)
\]

For IRFZ42
\[
P_{\text{sun}} = 1.26\text{W} \\
P_{\text{swf}} = 2.51\text{W} \\
P_{\text{con}} = 19.5\text{W} \\
P_{\text{tot}} = P_{\text{swf}} + P_{\text{sun}} + P_{\text{con}} = 23.24\text{W} \quad (6.14)
\]

For BUS14
\[
P_{\text{sun}} = 10\text{W} \\
P_{\text{swf}} = 29.3\text{W} \\
P_{\text{con}} = 47.25\text{W} \\
P_{\text{tot}} = P_{\text{swf}} + P_{\text{sun}} + P_{\text{con}} = 86.25\text{W} \quad (6.15)
\]

6.4.3 HEAT SINK DESIGN

a) The maximum junction temperature for MOSFET IRFP450 is \( T_j = 150^\circ\text{C} \), with a junction-to-heatsink thermal resistance \( R_{\text{thj-sink}} \) of 0.94°C/W [14] and an ambient temperature of
The required heatsink thermal resistance $R_{ths-amb}$ may therefore be calculated from equation (6.11) and (6.13) as

$$R_{thJ-amb} = \frac{T_{jmax} - T_{amb}}{P_{tot}} = 3.4°C/W$$

and

$$R_{ths-amb} = R_{thJ-amb} - R_{thJ-sink} = 2.46°C/W$$

b) For IRFZ 42, $T_{jmax} = 150°C$ and $R_{thJ-sink} = 2.0°C/W$

From equations (6.11) and (6.14)

$$R_{thJ-amb} = \frac{T_{jmax} - T_{amb}}{P_{tot}} = 5.38°C/W$$

$$R_{ths-amb} = R_{thJ-amb} - R_{thJ-sink} = 3.38°C/W$$

c) For the device BUS 14, $T_{jmax} = 200°C$ and $R_{thJ-mb} = 0.7°C/W$

From equations (6.11) and (6.15)

$$R_{thJ-amb} = \frac{T_{jmax} - T_{amb}}{P_{tot}} = 2.03°C/W$$

Since $R_{thJ-amb} = R_{thJ-mb} + R_{mb-s} + R_{s-amb}$

then

$$R_{ths-amb} = R_{thJ-amb} - R_{thJ-mb} - R_{thmb-s}$$

If the devices are mounted flat on heatsinks, with heatsink compound between the two surfaces, the thermal resistance between the mounting base of the device and the heatsink $R_{thmb-s}$ may be neglected, and

$$R_{ths-amb} = R_{thJ-amb} - R_{thJ-mb} = 1.33°C/W$$

The three commonly available types of heatsink are termed diecast finned, extruded finned and flat plate and the material normally used is aluminium. Since there were no
size restrictions on the prototype converter, flat plate heatsinks were used and painted black to give greater emissivity. An important advantage of a flat heatsink is that its high-frequency noise emission is low.

The thermal resistance depends on the thickness, area, and orientation of the plate [7]. The thickness of the heatsink chosen was 4mm and, from the nomograms given in Fig 6.15, the area =\(1.2 \times 10^4\, \text{mm}^2\), and the length=390mm.

6.5 DIODES AND CAPACITORS

6.5.1 DIODES

The diodes D1 and D2 of Fig 6.1 provide current paths for energy transfer between the inductors and capacitors, while D3 and D4 are freewheeling diodes as discussed in chapter 3. The characteristics of these diode are very important in determining the overall circuit performance.

It was emphasised in section 6.3.1 that high-speed transistors have a reduced switching loss. However, fast switching transistors do not necessarily result in lower switching losses unless the diodes used have recovery times 2 to 3 times faster than the transistor current rise time [15]. A fast transistor increases the peak recovery current in the diode and thus the overall switching losses. Furthermore, the reverse recovery delay time of the diodes increases the peak collector current, as shown in Fig 6.16, and consequently the switching loss in the transistor. The broken lines in Fig 6.16 show the current, voltage and power waveforms for an ideal diode with negligible reverse recovery time. The reverse recovery current of the diode is shown in the \(I_r\) curve. The transistor must conduct this reverse diode current as well as the inductor current. The
hatched areas of \( P_T \) and \( P_D \) represent the additional transistor and diode dissipation due solely to the diode recover delay.

To minimise these problems, a diode with a very fast recovery time was chosen:

\[
\text{BYV 30-400 : } V_{RRM(\text{max})}=400V \quad I_{F(AV)}=14A \\
I_{FSM(A)}=150A \quad t_{rr}=50\text{ns}
\]

6.5.2 CAPACITOR

The maximum output voltage ripple \( \Delta V_o \) of the 4-quadrant converter (see Chapter 5) was set at 10% of the mean output voltage \( V_o \), and since \( V_o=180V \) then \( \Delta V_o=18V \). The required capacitance follows from equation (5.7) as

\[
C = \frac{I_o t_1}{\Delta V_o} = 8.6\mu F
\]

and the nearest standard value of 10\( \mu F \) was used.

An equivalent circuit for the capacitor is shown in Fig 6.17(a), with the relevant circuit waveforms being given in Fig 6.17(b).

Since \( V_o = V_c + V_{ESR} \) the voltage ripple \( \Delta V_o \) is either \( \Delta V_c \) or \( \Delta V_{ESR} \), whichever is the greater. In high-frequency applications the equivalent series resistance ESR often dominates the voltage ripple and, to avoid this, the ESR must be sufficiently low to make \( \Delta V_{ESR} \) less than the maximum allowable value of 18V.
\[ \Delta V_{ESR} = I_{L \max} \cdot ESR + I_L \cdot ESR \]

then

\[ ESR(\text{max}) = \frac{18}{55 \cdot 6.5} \approx 290 \text{m} \Omega \]

A polypropylene capacitor designed for pulse applications was chosen. It has a high contact reliability and low losses at high frequency, due to the very low ESR. The ESR may be determined from [10]

\[ ESR = \frac{\tan \delta}{Cf} \quad (6.40) \]

where \( C \) is the capacitance, \( f \) the switching frequency and \( \tan \delta \) the dissipation factor.

For the capacitor chosen, it can be seen from Fig 6.18 that \( \tan \delta \) is \( 7 \times 10^{-4} \) at a frequency of \( 40 \text{kHz} \), giving

\[ ESR \approx 1.2 \text{m} \Omega \]

This is much less than \( ESR(\text{max}) \) and shows that the capacitor selected is quite suitable for the present application.

6.6 PROTECTION CIRCUIT DESIGN

Fig 6.19 shows a section of the converter power circuit. The stray inductances in the circuit can cause serious voltage spikes and high rates-of-change of voltage during switching, and it is necessary to provide protection circuits to limit these effects to acceptable levels. Overcurrent protection is also important and this is achieved using the microprocessor-controlled circuit discussed in detail in chapter 8.
6.6.1 SNUBBER CIRCUIT DESIGN

The RCD snubber circuit used in the power circuit is shown in Fig 6.20. For this arrangement

\[ C_s \frac{\Delta V}{\Delta t} = I_T \]

and with:

\[ \Delta t = t_{swf} = 0.5 \mu s \quad \Delta V = V_m = 300V \]

\[ I_T = \frac{I_m}{4} = \frac{SS}{4} \approx 14A \]

thus \[ C_s = 0.023 \mu F \]

The resistor \( R_s \) limits the peak transistor current during turn-on. Since the maximum voltage across the capacitor \( C_s \) is 300V and the maximum current of BUS14 is 50A, then

\[ R_s = \frac{V_c}{I_m} = \frac{300}{50} = 6 \Omega \]

However, the value of the resistor must be sufficiently low for the snubber capacitor to discharge completely during the turn-on period of the transistor, thus

\[ R_s C_s \leq \frac{t_{on(min)}}{5} = \frac{2 \mu s}{5} \]

\[ R_s \leq 16.7 \Omega \]

For the rating of \( D_s \)

\[ I_D = \frac{I_T t_{swf}}{T} = 0.28A \]
\[ I_{DM} = I_T = 14 \, A \]
\[ V_D = 300 \, V \]

The following snubber components were chosen:

- \( C_s \): 0.022 \mu F, 400V, polyester type
- \( R_s \): 0.022\Omega, 50W
- \( D_s \): Fast-recovery-diode BYV29-400 \( (V_D=400V, \, I_D=9A) \)

### 6.6.2 HIGH-SPEED CLAMPING DEVICES

The high-voltage spikes due to stray inductance may be clamped using a zener diode. However, such a device cannot continuously dissipate energy and consequently a varistor was used. For the low-voltage mosfet IRFZ42, a special ultra-fast transient suppressor IN6277 was used, for which:

- Stand-off voltage = 14.5V
- Maximum clamping voltage = 26.5V
- Maximum peak pulse current = 56.5A
- Transient pulse power = 1500 W (within 1ms)
- Clamping time = 1x10^{-12}s.

For the high-voltage devices BUS14 and IRFP450, the high-speed zeneric varistor Z15L391 was employed with an RMS working voltage of 230V, a peak transient current of 2000A, a DC working voltage of 310V, a varistor voltage at 1mA of 315V to 429V and a transient energy capability of 60J.

### 6.6.3 RINGING EFFECT

Internal capacitances exist in both mosfets and bipolar transistors, such as the drain-source capacitance \( C_{ds} \), the collect-emitter capacitance \( C_{ce} \), and the "Miller" capacitance
$C_{CD}$ as shown in Fig 6.21(a). These capacitances, together with the energy storage inductor and various stray induc-
tances, may cause oscillations or ringing in the circuit. The poor reverse recovery performance of the inherent source-drain diode of a mosfet also contributes to this effect.

Fig 6.21(b) shows the ringing on the voltage waveform across the switch $V_1$, which puts extra stress on the semi-
conductor devices and causes a deterioration in the overall converter performance. To minimise this effect, a fast
recovery diode $D$, was connected in series with each switch, as shown in Fig 6.21(a), to block the oscillation loop
between the inductor and the switch. The improved $V_1$ wave-
form is shown in Fig 6.21(c).

6.6.4 CIRCUIT LAYOUT

Both the power and drive circuits were carefully designed
to minimise stray inductance and ringing effects. To this end the switch drivers were located as close as possible to
their respective switches and the PCB layout was designed to
minimize the length of the connections as shown in Fig 6.22.

Any noise generated in the circuit earth connection will
seriously affect the performance of both the power and the
drive circuits. To avoid this, the impedance of the power
circuit earth is minimised and the earth of the drive signal
was directly connected to the mosfet source, so that the drive circuit is less affected.
Fig 6.1 4-Quadrant DC-DC Converter
Fig 6.2 Variation of Voltage Gain with Duty Cycle

(a) Ideal Condition
(b) Including Parasitic Resistance
Fig 6.3 MOS-BIMOS Switch

Fig 6.4 Base Drive Current Of Bipolar Transistor
Fig 6.5 Paralleling Transistors

Fig 6.6 BIMOS Switching Waveforms
Fig 6.7 Optimal Frequency Consideration
Fig 6.8 Inductor Current Waveform
(a) Continuous
(b) Discontinuous
(c) Transition
Fig 6.9 Dimensions Of EC Core FX3750
(Dimensions in mm)
Fig 6.10(a) EC Core (70/34/17) (Dimensions in mm)

Fig 6.10(b) Fringe Factor
Fig 6.11 Safe Operating Area

Fig 6.12 Thermal Resistance Between Junction And Mounting Base

Fig 6.13 Maximum DC Power Dissipation of Transistor
Fig 6.14 Switching Waveforms Of Transistors
(a) BUS14
(b) IRFZ42
(c) IRFP450
Fig 6.15 Heatsink Nomogram
Fig 6.16 Effect Of Diode Recovery Delay Time
Fig 6.17(a) Capacitor Model

Fig 6.17(b) Capacitor Waveforms
Fig 6.18 Dissipation Factor
Fig 6.19 Stray Inductance

Fig 6.20 Snubber Circuit
Fig 6.21 Ringing Effect Inside Power Switch
(a) Capacitances In Mosfets And Bipolar Transistor
(b) Ringing On The Voltage Across The Switch
(c) Improved Voltage Waveform
Fig 6.22 PCB Board
CHAPTER 7 DRIVE CIRCUIT DESIGN

The Mos-Gated bimos switch described in chapter 6 performs only as well as its gate drive permits. Consequently the drive circuit is extremely important, and a careful study of the gate requirements will result in the best device performance.

7.1 PWM SIGNAL GENERATOR

A PWM signal generator is used for open-loop operation. The saw-tooth carrier signal is obtained using a 555 timer, as shown in Fig 7.1(a). The small signal fet $Q_1$ provides a constant-current source to charge the capacitor $C$ and, as a result, the saw-tooth ramp of Fig 7.1(b) is almost linear. The values of resistance and capacitance in the circuit are determined using a standard design procedure. The capacitor must have a leakage current less than 10% of the threshold current $I_{th}(0.01\mu A)$ in order to ensure satisfactory performance, and suitable capacitor dielectrics are silvered mica, polycarbonate, and polystyrene.

The saw-tooth signal of Fig 7.1(b) is compared with a reference voltage using the circuit of Fig 7.2(a), and the resulting output pulse-width, as shown in Fig 7.2(b), may be varied by changing the reference voltage level.

7.2 ISOLATOR

The PWM control circuit may be isolated from the power circuit, since each switch has a different ground. Two common methods for separating control and power circuits are isolation transformers and opto-couplers.
7.2.1 ISOLATION TRANSFORMER

Fig 7.3(a) shows a drive circuit using a pulse transformer \( T \), with several secondary circuits, used to control several switches at different ground levels.

The advantage of using a pulse transformer is that only one power supply is required for the four drive signals. However, due to the voltage-time balance of the transformer (see Fig 7.3(b)) the amplitude of the drive signal for a large duty cycle \( D_{\text{max}} = 0.86 \) may fall below the value required to turn-on the mosfet.

The circuit shown in Fig 7.4 is usually used to drive gate-turn-off thyristors. The transformer \( T \), needs to be designed with a low leakage inductance and to saturate easily. Consequently, the output voltage waveform for a square-wave input voltage is as shown in Fig 7.5 and is unaffected by any variation in the duty cycle. The positive pulse locks the output high by positive feedback, and it remains high until the next negative pulse.

Unfortunately, the drive circuit of Fig 7.4 requires a separate power supply for each isolated drive circuit, which negates the main advantage of using a pulse transformer. Furthermore, a transformer with a low leakage inductance is difficult to construct and, in practice, the transformer may well not saturate.

7.2.2 OPTO-COUPLER

The considerations of section 7.2.1 led to the selection of the opto-coupler shown in Fig 7.6 as the isolator, since

a) It is more reliable than a pulse transformer.
b) The range of duty-cycle variation is almost 0-100%.

c) A very fast TTL/CMOS compatible opto-coupler IC is available.

d) The drive circuit is simple and straightforward.

The 6N317 opto-coupler is TTL compatible and has a typical response time of 45ns. Its output has an open collector, so that the output voltage level may be raised by means of a "pull-up" resistor.

7.2.3 MOSFET DRIVE REQUIREMENT

The gate/drain capacitance $C_{gd}$ of a mosfet is an important parameter in the design of the gate-drive circuit. It is non-linear and depends on both the drain/source and the gate/source voltages. Although the gate/drain capacitance $C_{gd}$ has a smaller static value than the gate/source capacitance $C_{gs}$, it requires more charge, due to the Miller effect [16]. The total dynamic input capacitance of the device is therefore greater than the sum of the static electrode capacitances [16].

Fig 7.7 shows the typical gate/source voltage waveform. Initially the gate voltage rises, and $C_{gs}$ is charged. During the plateau of the voltage waveform, the drain/source voltage begins to fall, and provides a path by which $C_{gd}$ is charged. When both $C_{gs}$ and $C_{gd}$ are fully charged the gate/source voltage again rises, indicating the minimum gate/source voltage needed for a given drain/source voltage and drain current. The gate/source voltage continues to rise to the value of the open-circuit gate drive voltage.
It is evident from Fig 7.8 and Fig 7.9 that the minimum charge for switch-on of IRFP450 is 50nC and for IRFZ42 it is 30nC. Based on these figures, and a defined switch-on time, the gate charge current may be determined and the gate-drive circuit designed.

Assuming a switch-on time of 120ns, the charging currents required for the two mosfets are

IRFP450:
\[ I_{g(\text{min})} = \frac{50}{120} = 0.42A \]

and

IRFZ42:
\[ I_{g(\text{min})} = \frac{30}{120} = 0.25A \]

The total gate current for one IRFP450 and two IRFZ42 is therefore

\[ I_g = 0.42 + 2 \times 0.25 = 0.92A \]

The push-pull circuit of Fig 7.6 is capable of providing 1.5A, which is adequate for the bimos switch. The mosfet gates shown in Fig.7.10 are all decoupled with individual resistors (R₁ to R₃). Without these the first device to turn-on, which is the device with the lowest threshold voltage, will tend to slow down the gate voltage rise of the other devices. This will further delay their turn-on and impair the current sharing balance within the paralleled devices.

The required value of the decoupling resistors are

\[ R₁ \leq \frac{V_{GS}}{I_{g(\text{min})}} = \frac{12}{0.42} = 28.6\Omega \]
\[ R_2 = R_3 \leq \frac{12}{0.25} = 48\Omega \]

In practice,

\[ R_1 = R_2 = R_3 = 25\Omega \]

was found satisfactory.

Fig 7.11 shows details of the circuit designed.
Fig 7.1 Saw-tooth Signal Generator
(a) Circuit Diagram
(b) Saw-tooth Signal Waveform
Fig 7.2 PWM Signal Generator

(a) Circuit Diagram
(b) Waveforms Of Saw-tooth, Reference And PWM Signals
Fig 7.3 Drive Circuit With Isolation Transformer
(a) Drive Circuit
(b) Voltage-Time Balance
Fig 7.4 Isolated Drive Circuit With Wide Range Of Duty Cycle

Fig 7.5 Output Voltage Waveform Of Saturated Transformer
Fig 7.6 Drive Circuit With Optocoupler
Fig 7.7 Typical Gate Charge Waveforms

Fig 7.8 Typical Gate Charge Of IRFP450

Fig 7.9 Typical Gate Charge Of IRFZ42
Fig 7.10 Decoupled Gate Drive
Fig 7.11 Drive Circuit For 4-Quadrant DC-DC Converter
A closed-loop control system can be implemented using either analogue or digital techniques. Recent advances in both digital electronics and microprocessor technology have led to their adoption in almost every field of electrical power engineering, and the microprocessor control of variable-speed drives, which appears to be a particularly interesting application, is described in this chapter.

Conventional digital closed-loop control systems for variable-speed drives usually contain an outer speed loop and an inner current loop, as shown in Fig 8.1. In certain special applications, where position control is required, the third loop shown in Fig 8.2 is added.

In general, control algorithms are classified as either linear or non-linear, with linear control algorithms being formed from one or more of the proportional, integral, and derivative operations. When combined, the three lead to the most general case of a Proportional-Integral-Derivative (PID) control algorithm.

Of the many methods which exist for the design of digital controllers, one of the most clear, straight-forward and easily understood is the Engineering Design Method, discussed later in detail in section 8.2.

8.1 DC MOTOR POSITION CONTROL SYSTEM

Fig 8.1 shows a typical speed-control system containing a speed and a current controller. The first of these maintains the motor speed at the demand level, while the second ensures that the motor starting current does not exceed the maximum allowable value. When the motor is started, the current controller allows the armature current to rise to its limit and maintains it constant at this value, so that the
motor reaches the demand speed in the shortest possible time. After that the speed controller becomes active and maintains the speed at or very near the demand value.

In order to eliminate steady-state error, both controllers normally include an integral operation, so that either a PI or a PID controller may be used.

The position-control system shown in Fig 8.2 contains an additional position controller, which ensures that the motor reaches the demand position. This controller need not contain an integral term, since one exists already in the change from speed to angular position control. Although a 3-loop position control system has good inherent stability and can be easily adjusted, it suffers from the drawback of a slow response due to the several integral operations existing within the system.

In medium and low power drives, the armature resistance is relatively high and, in some systems, a substantial overshoot of armature current for a short period is allowed. In order to reduce the response time an Interventionist System [17] may be used, in which the current loop is omitted and only a maximum current limit is employed. The system then becomes a 2-loop position-control system.

The Interventionist System has many advantages, particularly in the field of digital control. Its relative simplicity reduces cost and saves microprocessor computing time, while its enhanced reliability permits the designer to concentrate on the properties of position and speed-control without worrying about the current-loop. In addition, it is possible to realise direct digital control without the use of A/D or D/A converters.
8.2 THE ENGINEERING DESIGN METHODS IN AUTOMATIC CONTROL SYSTEM

Control systems are generally required to perform under both transient (dynamic) and steady-state conditions, with the control parameters being adjusted to provide the best behaviour in both situations. The system behaviour may be studied using either time or frequency response considerations. The former gives a general picture of the system behaviour, as shown in Fig 8.3, from which the speed of response, the frequency of any oscillations and the time to reach the final steady-state output can all be studied. However, for design purpose, time-response considerations are often too complicated and cumbersome. On the other hand, frequency-response methods investigate the stability of the system through considerations of the input/output characteristic as a function of frequency. This characteristic is explicit, straightforward and easy to analyse, and any design and parameter adjustments of the open-loop transfer function to meet a specified closed-loop performance are more easily carried out through frequency rather than time-response considerations.

Frequency-response techniques [18] are often used to design control systems, with the object being to find a controller by which the system can be adjusted to provide a specified open-loop frequency response. This response often means that (see Fig 8.4):

a) The log-magnitude of the frequency-response characteristic should cross the 0dB axis with a slope of -20dB/decade in the area of medium frequency. The band-width of the medium frequency $\omega_1$ to $\omega_2$ should be sufficient to ensure that the system is stable.

b) The cut-off frequency $\omega_c$ should be sufficiently high to
ensure a rapid system response.

c) The magnitude of the response in the low-frequency range, which depends mainly on the proportional gain of the systems, should be sufficiently high to ensure a good static accuracy.

d) Sufficient damping should be present in the high frequency range, to minimize the effects of noise and of any disturbance to the load.

In practice, it is often difficult to achieve a characteristic with all the features listed above and a compromise may be necessary. In different applications the emphasis may be different, and attention needs to be focussed on the most relevant features while maintaining the others at the best possible level.

8.2.1 STANDARD SYSTEM

For a linear control system the open-loop transfer function may be written as

$$W(s) = \frac{K(1+\tau_1 s)(1+\tau_2 s)}{s'(1+T_1 s)(1+T_2 s)}$$

(8.1)

where $\tau_1$, $\tau_2$, $T_1$ and $T_2$ are the system time constants and $r$ represents the number of pure integrations in the system. Systems are classified as type 0, type I, type II, type III, .... corresponding to $r=0, 1, 2, 3, ....$ respectively.

Figs 8.5 and 8.6 show typical type I and type II systems, together with their open-loop log-magnitude/frequency characteristics.
8.2.2 THE CHARACTERISTICS OF TYPICAL SYSTEM

Since type I system is used in the experimental controller considered later in the thesis, only the characteristics of this type of system are discussed here.

The transfer function of a type I system is:

\[ \omega(s) = \frac{K}{s(1+Ts)} \] (8.2)

it follows from Fig 8.5(b) that

\[ 20 \log K = 20 \log \frac{\omega_c}{1} \]

\[ K = \omega_c \]

The cut-off frequency \( \omega_c \) is therefore numerically equal to the proportional gain \( K \), provided that

\[ \omega_c < \frac{1}{T} \]

The higher the cut-off frequency, the faster is the system response. However the overshoot is also greater and the stability is correspondingly reduced.

Table 8.1 shows the dynamic response of a type I system for different values of the product KT.
8.2.3. THE CONTROLLER DESIGN

As stated in section 8.2.1, the design objective is to produce a system having the desired response. However, before designing the controller, it is necessary to determine what type of system is required.

A type I system has a simple structure and a low overshoot, but is easily disturbed. Although a type II system is relatively complicated, and often has a high overshoot, it is not easily disturbed. Type III systems and above have difficulties associated with stability and are often adjusted into lower-type system. Since a low overshoot is essential in the response of the position control scheme being considered, a type I system was adopted.

Table 8.2 lists the different controllers which are required to adjust different control systems into a type I system.
### Table 8.2 Controllers For The Type I Systems

<table>
<thead>
<tr>
<th>Control System</th>
<th>( \frac{K_s}{(1+T_1 s)(1+T_2 s)} )</th>
<th>( \frac{K_d}{1+T_1 s} )</th>
<th>( \frac{K_d}{(1+T_2 s)^2} )</th>
<th>( \frac{K_d}{(1+T_3 s)(1+T_2 s)(1+T_3 s)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_1 &gt; T_2 )</td>
<td>( T_3 ) is quite small, and ( T_1 ) and ( T_2 ) are relatively large</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Controller</th>
<th>( \frac{K_p}{\tau s} )</th>
<th>( \frac{K}{s} )</th>
<th>( K_p \frac{(1+\tau_1 s)(1+\tau_2 s)}{\tau_1 s} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(PI Controller)</td>
<td>(I Controller)</td>
<td>(P Controller)</td>
<td>(PID Controller)</td>
</tr>
</tbody>
</table>

| Coefficients | \( \tau = T_1 \) | \( \tau_1 = T_1 \), \( \tau_2 = T_2 \) |

**Note:** The table above represents controllers for Type I systems, with specific conditions and coefficients for each type of controller.
8.3 PID CONTROLLER DESIGN

The novel 4-quadrant DC-to-DC converter described in the thesis is used to drive a DC servo motor, with the following requirements:

a) The number of revolutions of the motor must be accurately controlled.

b) The speed is controlled such that, following a change in the demand position, the motor runs at maximum speed until the required position is approached. The speed then reduces, and the motor finally stops when it reaches the demand position.

c) The response-time of the system is minimised.

d) The overshoot is kept to a minimum.

e) The system is stable.

In order to achieve these requirements, several PI and/or PID controllers were investigated and the best option was chosen.

8.3.1 THE PID CONTROLLER

The Proportional-Integral-Derivative (PID) controller with the general form shown in Fig 8.7 is widely used in continuous-data control systems. The purpose of the proportional term $K_p$ is to achieve optimum acceleration of the system response, so as to achieve the demand value in the
minimum time. The integral term $K_1/s$ eliminates the steady-state error around the demand value, and the derivative term $sK_d$ provides an anticipatory action to reduce any overshoot in the response.

Although the 3-term combination is the general form of the controller, a 2-term combination may be obtained by setting the coefficient of the third term to zero. Any desired response may be obtained by adjustment of the three coefficient $K_p$, $K_i$, and $K_d$.

The time-domain relation between the output $E_a(t)$ and the input $E(t)$ of the 3-term controller is

$$E_a(t)=K_pE(t)+K_i\int_0^t E(t)dt + K_d\frac{dE(t)}{dt}$$  \hspace{1cm} (8.6)

with the associated $s$-domain transfer function being

$$D(s)=\frac{E_a(s)}{E(s)}=\frac{K_ds^2+K_ps+K_i}{s}$$  \hspace{1cm} (8.7)

Since the 3-term controller has proved very useful for continuous-time control system design, it is clearly desirable to develop a digital control algorithm which possesses similar characteristics.

8.3.2 TRANSFER FUNCTION

8.3.2.1. DC MOTOR TRANSFER FUNCTION AND BLOCK DIAGRAM

The separately-excited DC motor shown in Fig 8.8 has the dynamic armature voltage equation
\[ E_a = K_a \phi \omega + R_a I_a + L_a \frac{dI_a}{dt} \]  \hspace{1cm} (8.8)

and the torque balance equation

\[ M_a = F \omega + J \frac{d\omega}{dt} \]  \hspace{1cm} (8.9)

where the developed electromagnetic torque is

\[ M_a = k_a \phi I_a \]  \hspace{1cm} (8.10)

Re-writing equations (8.8) to (8.10) respectively in the Laplace domain gives

\[ E_a(s) = k_a \phi \omega(s) + R_a I_a(s) + L_a s I_a(s) \]  \hspace{1cm} (8.11)

\[ M_a(s) = F \omega(s) + J s \omega(s) \]  \hspace{1cm} (8.12)

and \[ M_a(s) = K_a \phi I_a(s) \]  \hspace{1cm} (8.13)

From equation (8.11)

\[ I_a(s) = \frac{E_a(s) - K_a \phi \omega(s)}{R_a + sL_a} = \frac{E_a(s) - K_a \phi \omega(s)}{R_a(1 + \tau_a s)} \]  \hspace{1cm} (8.14)

where \( \tau_a = L_a / R_a \) is the armature circuit time constant. From equations (8.12) and (8.13)

\[ \omega(s) = \frac{K_a \phi I_a(s)}{F(1 + \tau_m s)} \]  \hspace{1cm} (8.15)

where \( \tau_m = J / F \) is the motor mechanical time constant.
The two relationships expressed by equations (8.14) and (8.15) are detailed in block diagram form by Fig 8.9, from which the change in speed $\omega(s)$ due to variations in the applied voltage $E_a(s)$ may be obtained as

$$\frac{\omega(s)}{E_a(s)} = \frac{K_b/(K_b^2 + R_a K_f)}{J L_a/(K_b^2 + R_a K_f) s^2 + (J R_a + k f L_a)/(K_b^2 + R_a K_f) s + 1} \quad (8.16)$$

where $K_b = K_a \phi$. $K_f = F$

### 8.3.2.2 SYSTEM TRANSFER FUNCTION

It was shown in chapter 4 that the converter transfer function has the form

$$\frac{V_s}{d^2(s)} = \frac{V_s}{(1-D)^2(1+sL_s/R + s^2L_s C)} + \frac{V_s}{(1-D')^2(1+sL_s'/R + s^2L_s' C)} \quad (8.17)$$

where

$$I_s = \frac{L}{(1-D)^2} \quad I'_s = \frac{L}{(1-D')^2}$$

In the steady state,

$$K_b I_a = K_f \omega$$

so that

$$\omega = \frac{K_b I_a}{K_f}$$

and

$$E_a = I_a R_a + K_b \omega$$

$$= I_a R_a + \frac{K_b^2 I_a}{K_f}$$
so that 

\[ R = \frac{E_a}{I_a} = R_a + \frac{K_b^2}{k_f} \]

where \( R \) is the effective load resistance.

As explained in chapter 4, the system is increasingly unstable for large converter duty cycles. Considering the extreme situation with \( D = 86\% \), which is the duty cycle required to give an output of 180V,

\[
\frac{1}{D'^2} = \frac{1}{(1-D)^2} = 51 \quad \text{and} \quad \frac{1}{(1-D')^2} = \frac{1}{D^2} = 1.3
\]

Since \( \frac{1}{D'^2} \gg \frac{1}{D^2} \)

equation (8.17) can be re-written approximately as

\[
\frac{\dot{V}_o(s)}{\dot{a}} = \frac{V_o}{D'^2} \left( \frac{1 - sL/(RD'^2)}{1 + sL/(D'^2R) + s^2LC/D'^2} \right)
\]

In chapter 6, it was shown that for the 4-quadrant converter,

\( L = 25\mu H \quad \text{and} \quad C = 15\mu F \)

The measured parameters of the experimental DC motor are:

\( K_a = 1.06V/s/rad, \quad K_f = 0.95 \times 10^{-3} Nms/rad, \quad R_a = 26\Omega, \quad J = 5 \times 10^{-3} kgm^2 \)

Thus

\[
\frac{\dot{V}_o(s)}{\dot{a}} = 1428.6 \times \frac{1 - 1.06 \times 10^{-6}s}{1 + 1.06 \times 10^{-6}s + 0.019 \times 10^{-6}s^2} \quad (8.18)
\]

Since the output voltage of the converter is applied to the armature of the DC motor,
\[ \dot{V}_o(s) = E_a(s) \]

Substituting values in equation (8.16) gives

\[
\frac{\omega}{\dot{V}_o(s)} = \frac{0.92}{7.84 \times 10^{-4} s^2 + 0.11 s + 1} \tag{8.19}
\]

Since the motor mechanical time-constant is much greater than the electrical time constant of the converter from which it is supplied, the system transfer function is obtained approximately by multiplying the two transfer functions of equations (8.18) and (8.19). Then, ignoring higher-order terms,

\[
\frac{\omega}{d(s)} = \frac{1314.3(1 - 1.06 \times 10^{-6} s)}{1 + 0.11 s + 7.84 \times 10^{-4} s^2} \tag{8.20}
\]

### 8.3.3 CONTROLLER DESIGN

In the position-speed 2-loop control system the demand signal represents a position and the output from the position controller is the speed reference for the speed loop. Controller design conveniently begins with the inner loop, for which the speed controller design is based on the transfer function of the converter drive system. It follows that the position controller design for the outer position loop is based on the equivalent transfer function of the inner speed loop. Fig 8.10 shows the functional block diagram for the 2-loop control system.
8.3.3.1 SPEED CONTROLLER

Equation (8.20) may be re-written approximately as

$$ F_1(s) = \frac{\omega}{d(s)} = \frac{1314.3}{(1+0.104s)(1+7.65 \times 10^{-3}s)(1+1.06 \times 10^{-6}s)} $$

(8.21)

As shown in Table 8.2, to adjust the system to a standard type I system requires a controller of the form

$$ F_2(s) = \frac{\Delta \omega}{\Delta \omega} = K_s \frac{(1+0.104s)(1+7.65 \times 10^{-3}s)}{s} $$

(8.22)

Combining equations (8.21) and (8.22) leads to

$$ F(s) = \frac{\omega}{\Delta \omega} = \frac{K}{s(1+Ts)} $$

where \( K = K_s \times 1314.3 \) and \( T = 1.06 \times 10^{-6} \)

Theoretically, the optimum performance for a type I system occurs when \( K=1/(2T) \), from which a damping factor of 0.707, an overshoot of 4.3% and rise time of 4.72T are obtained. It follows from \( K=1/(2T) \), \( K_s = 201.3 \) that

$$ F_2(s) = 0.16s + \frac{201.3}{s} + 22.14 $$

(8.23)

and comparing equation (8.23) with the expression for a PID controller of equation (8.7) gives

$$ K_p = 22.14, \quad K_i = 201.3, \quad K_d = 0.16 $$
8.3.3.2 POSITION CONTROLLER

The equivalent transfer function of the inner speed loop of Fig 8.10 is

\[ G(s) = \frac{F(s)}{1 + F(s)} \]

and the open-loop transfer function of the position loop is

\[ G_p(s) = \frac{1}{s} \cdot G(s) = \frac{1}{s(1 + 1.06 \times 10^{-6}s)^2} \]

From Table 8.2, the position loop requires a controller for which

\[ F_3(s) = K_1(1 + \tau_2 s) = K_1(1 + 1.06 \times 10^{-6}s) \]  (8.24)

and with this controller the open-loop transfer function of the position loop becomes

\[ W_p(s) = F_3(s)G_p(s) = \frac{K}{s(1 + Ts)} \]

where \( K = K_1 \), \( T = 1.06 \times 10^{-6} \)

Since zero-overshoot is required, \( KT \) must be less than 0.25, as shown in Table 8.1, giving

\[ K_1 = K \leq 2.36 \times 10^5 \]

The term \( K_1 \) is determined according to the control strategy. Since the maximum motor speed is 1400 rpm, the maximum output of the position controller, which is the speed
reference for the speed-loop, is 1400 and the minimum countable position is one revolution. In order for the motor to run slowly and smoothly with a low demand position, the control strategy is designed such that the controller output does not reach 1400 unless the error between the demand and actual position exceeds 14. Therefore $K_1 = 100$, and from equation (8.24)

$$F_3(s) = 100(1 + 1.06 \times 10^{-6}s) = 100 + 1.06 \times 10^{-4}s$$

(8.25)

giving a PD controller with $K_p = 100$ and $K_d = 1.06 \times 10^{-4}$

8.3.3.3 CURRENT LIMIT PROTECTION

As stated in section 8.1, the best way to limit the current in a 2-loop control system is to use an interventionist system [17], in which the current limit is introduced only when the armature current exceeds a threshold value. Fig 8.11 shows such a system, with the armature current being sensed by the Hall-Effect Current Transducer. The output of the transducer $(K_I I_a)$ is applied to the threshold circuit TA, whose output is zero provided the current is less than the preset maximum armature current $I_{am}$, but which amplifies the excess by a gain $G_a$ if the current exceeds $I_{am}$.

Thus the output voltage of the transducer $V_I$ is

$$V_I = 0, \quad -I_{am} \leq I_a \leq I_{am}$$

$$V_I = G_a K_I (I_a - I_{am}), \quad I_a \geq I_{am}$$

$$V_I = G_a K_I (I_a + I_{am}), \quad I_a \leq -I_{am}$$

Where $G_a$ is the proportional gain.
8.3.3.4 DIGITAL CONTROL ALGORITHMS

Fig 8.12 shows a block diagram for the entire digital control system. When the principles of conventional PID control are applied to digital control, there are a number of ways by which the integral and derivative terms may be implemented. For position control, the function of the digital PD controller obtained in section (8.3.3.2) may be stated as [19]

\[ X_{dm} = e_n K_{p\theta} + K_d (e_n - e_{n-1}) \]

where \( K_d = K_d / T \), \( K_{p\theta} \) is the proportional gain, \( T \) the sampling period and \( e_n \) the position error at the nth sampling instant.

It follows from equation (8.25) that, with \( T = 12 \text{ms} \),

\[ K_{p\theta} = 100 \quad \text{and} \quad K_d = 8.8 \times 10^{-3} \]

For speed control, the separate functions of the digital PID controller may be written as

Integral: \( I_n = I_{n-1} + K_i \Delta \omega_n \)

Proportional: \( P_n = K_p \omega \Delta \omega_n \)

Derivative: \( D_n = K_d (\Delta \omega_n - \Delta \omega_{n-1}) \)

with the overall function being \( V_c = I_n + P_n + D_n \)

where \( K_i = K_i T \), \( K_d = K_d / T \), \( K_p \omega \) is the proportional gain and \( \Delta \omega_n \) the speed error at the nth sampling instant.

Using the coefficients of the PID speed controller given in equation (8.23) results in

\[ K_i = 2.4 \]

\[ K_p \omega = 22.14 \]
The microprocessor implements the digital current-limit protection described in section 8.3.3.3, by examining the status of the overcurrent flag set when the armature current exceeds the preset limit. If this occurs the value of \( V_c \), which determines the duty cycle, is changed, by varying \( I_n \) such that

\[
I_n = I_n + C_1
\]  
(8.26)

where the step size \( C_1 \) is set as 4% of the duty cycle by experience with the experimental system.

Selection of the appropriate sign in equation (8.26) depends on whether the output of the integrator \( I_n \) is positive or negative, i.e. whether the motor direction is forward or reverse. The sign adopted is opposite to that of \( I_n \).

After one sampling period, the processor again checks the current. If this still exceeds the preset limit the duty cycle changes by another 4%, by executing equation (8.26). This process is repeated until the current has fallen below the limit.

The output of the PID controller \( V_c \) is converted into the duty cycle through a control algorithm. In calculating the duty cycle, consideration is given to the non-linear relationship between the duty cycle and the steady-state output voltage of the converter shown in Fig 8.13(a) and obtained from

\[
\frac{V_o}{V_s} = \frac{1}{D'} - \frac{1}{D} = \frac{D-D'}{D D'}
\]

If the output of the speed controller \( V_c \) is converted into the duty cycle, through a proportional item, it is difficult
to maintain a high and stable output voltage, since any small change in the duty cycle leads to a large variation of the output voltage. A control algorithm of non-linear conversion similar to that shown in Fig 8.13(a), is used to keep the output voltage and thus the motor speed under control.

The relationship given in Fig 8.13(a) may be divided into regions I and II, corresponding respectively to $D \geq 0.5$ and $D < 0.5$

(I) In region I, where $D' \ll 1$

$M = \frac{V_c}{V_s} = \frac{1 - 2D'}{D'} = \frac{1}{D'} - 2$

and $D = \frac{M + 1}{M + 2}$

Since $V_c$ and $M$ are linearly related, $V_c = K_2 M$, which gives

$D = \frac{V_c + K_2}{V_c + 2K_2}$

(8.27)

With a duty cycle $D = 86\%$ required to give $V_c = 180V$, it follows from equation (8.27) that

$0.86 = \frac{V_c + K_2}{V_c + 2K_2}$

so that $V_c = 5K_2$

With a small $\Delta V_c$ ($\Delta V_c \ll V_c$)
To achieve an accuracy of duty cycle within 0.1%, $K_2 = 30$ is used, which makes $\Delta D = 0.06\%$ with each step change of $V_c$.

Hence:

$$D = \frac{V_c + 30}{v_c + 60}, \quad V_c \geq 0 \quad (8.28)$$

This conversion is shown in Fig 8.13(b).

(II) In region II, where $D \ll 1$

$$M = \frac{2D - 1}{D - D^2} \approx \frac{2D - 1}{D} = 2 - \frac{1}{D}$$

giving

$$V_c = -\frac{K_2}{D} + 2K_2$$

and

$$D = \frac{K_2}{2K_2 - V_c}$$

For $K_2 = 30$,

$$D = \frac{30}{60 - V_c}, \quad V_c \leq 0 \quad (8.29)$$

which is shown in Fig 8.13(c).

The difficulty of maintaining the drive stable at the high-speed region has been solved, but the problem still persists in the low-speed region. This is because, when the duty cycle is around 50%, $dD/dV_c$ is relatively large, which
leads to a large variation in output voltage with only a small change in $V_c$. Because of this problem, regions I and II are further subdivided into the low-speed and high-speed sub-regions shown in Fig 8.13(d). For a low output voltage, the new linear formula of equation (8.30) is employed to reduce the variation in $dD/dV_c$.

$$D = 0.5 + \frac{V_c}{256}$$  \hspace{1cm} (8.30)

To summarize,

$$D = \frac{30 + V_c}{60 + V_c} \hspace{1cm} V_c \geq 67$$

$$D = 0.5 + \frac{V_c}{256} \hspace{1cm} -67 \leq V_c \leq 67$$

$$D = \frac{30}{60 - V_c} \hspace{1cm} V_c \leq -67$$

8.4 POSITION AND SPEED MONITORING

Modern encoders offer higher resolution, greater reliability and greater accuracy than the alternative arrangement of a tachometer coupled to an analogue/digital converter, and in addition they are readily interfaced with a digital control system. In a practical unit, the rotary displacement is encoded as a number by the encoder disc and a logic circuit. One type, in which the number of encoder output pulses is counted over a fixed time period, is designated a constant-time resolver. In the alternative constant-displacement resolver, the angular velocity is determined by measuring the time required for a fixed angle of rotation.
Both types of encoder include a digital counter, made of cascaded flip-flops, which accumulates and stores the input pulses as a binary or BCD number. Such counters are the cornerstone of many designs of digital circuit.

The experimental speed measurement circuit used to interface the motor and the system controller, is illustrated by the block diagram of Fig 8.14. The main elements of this circuit are:

a) A shaft encoder and its output interfacing circuit

b) The envelope shaping circuit

c) Binary and BCD counter circuits, together with their related latching devices

d) A direction of rotation detection circuit and

e) A speed demand interfacing circuit.

The position monitoring system can use the same encoder as the speed monitoring system, with a bidirectional counter circuit determining the number of output pulses from the encoder to establish the actual position. A block diagram of the system is shown in Fig 8.15.

8.4.1 SHAFT ENCODER INTERFACING CIRCUIT

An incremental shaft encoder produces a single output pulse for each incremental change in the shaft position, by either optical or mechanical means. A known number of pulses is generated for each complete rotation of the shaft, so
that the accuracy of measurement depends largely on the accuracy with which the encoder is manufactured and the accuracy of its assembly on the motor shaft.

The specification of the encoder used in this research gives the encoder constant $A$ (i.e. the number of pulses per rotation) as 1250. If $N$ is the shaft speed in rpm, the corresponding output frequency in Hz is

$$f = \frac{NA}{60}$$

The minimum encoder output pulse frequency occurs at the minimum motor speed, and vice versa.

Thus, for $N_{\text{min}} = 1 \text{ rpm}$, $T_{\text{max}} = 48 \text{ ms}$
and for $N_{\text{max}} = 1500 \text{ rpm}$, $T_{\text{min}} = 32 \mu s$

A gating signal duration of at least 48 ms is therefore necessary to ensure coverage of the full speed range. This is undoubtedly large for a digital speed control application, since it is comparable with the mechanical time constant of the drive and could introduce unexpected problems and possibly instability if a sudden speed change occurred during a sampling interval [20].

The only way to decrease the duration of the gating signal is to use frequency multiplication to increase the number of encoder output pulses. In the experimental system the frequency is multiplied by 4, using the circuit of Fig 8.16(a), to reduce the gating duration to 12 ms. If multiplication by a greater factor is desired, this is only possible at the expense of increased circuit complexity and cost.
There are four outputs for the A quad B type encoder; 1 relative to A and 2 relative to B and their respective complements $\tilde{1}$ and $\tilde{2}$. Further reference to Fig 8.16(a) shows that the encoder output frequency $f$ is first multiplied by 2, using an exclusive-OR gate ($1/4 \times 74LS86$). Following this, single pulses are generated at each change of logic state of the $2f$ signal using two monostables, one triggering on the rising edge of the pulse and the other on the falling edge. The pulse duration must obviously be less than one-half the minimum pulse duration, to avoid pulse overlap and possible miscounting at high speed. In practice, the pulse duration is set at about $1\mu s$.

Fig 8.16(b) illustrates the pulse sequence throughout the interfacing circuit, and demonstrates how frequency quadrupling is achieved.

8.4.2 DIRECTION OF ROTATION DETECTION CIRCUIT

The direction of rotation of the motor shaft may be determined from the encoder output, since channel 1 output leads that of channel 2 by $90^\circ$ for one direction of rotation and lags it by the same amount for reverse rotation.

Implementing this facility using the logic circuit of Fig 8.17, provides a visual indication on the relevant LED, together with a 1-bit signal to the controller circuit to indicate the actual direction of rotation to be compared with the demand direction.

Fig 8.18 illustrates the pulse sequence at each point in the circuit, for each direction of shaft rotation.
8.4.3 CLOCK CIRCUIT AND GATING SIGNAL GENERATION

In a digital control system, it is necessary to provide a common time base for all the circuits involved and to synchronise the overall operation.

In the experimental unit, the synchronising signals G1 and G2 shown in Fig 8.19 originate from the microprocessor controller discussed fully in section 8.5. The signal G1 is used as a gating signal with a duration of 12 ms, for use in the binary counter described in section 8.4.4. The signal G2 is used to gate the BCD counter with the same duration of 12 ms, but at a lower frequency of about 1 Hz. This low frequency provides a comparatively long holding time for the counter, to ensure visual stability of the display.

8.4.4 BINARY COUNTER CIRCUIT

The rotational speed of the motor is measured by a technique in which the output pulse train generated within a prescribed time (i.e. the active period of the gating signal) is digitized, using the counter circuit of Fig 8.20(a). Together with the direction signal, the 12-bit output number which represents the motor speed is fed to the controller for comparison with the demand speed.

The main components of the counter are the 4-bit binary counters (3x74HCT161), which count the number of pulses within the 12 ms duration of the gating signal. At the end of this period the output of the counter is transferred to a pair of OCTAL D-type latches (74LS273), when a positive gating signal is received at the clock pin of the latches. This gating signal is generated by monostable M1, triggered on the negative edge of the counter gating signal G1. At the end of the store pulse, monostable M2 generates a pulse.
which resets the counter. This enables a new counting process to begin at the next sampling period. It is important that the sum of the store and the reset times (i.e., the durations of the output pulses of M1 and M2) should not exceed the holding time of the gating signal, to ensure that the system is ready at the commencement of the next counting period. The individual durations of M1 and M2 are 1 \mu s and 0.5 \mu s respectively. The pulse sequence for the counter circuit is illustrated in Fig 8.20(b).

The shaft position is measured by counting the pulses from the index output of the incremental encoder. This index output Z, which has one pulse per revolution, is applied to the bidirectional binary counter circuit shown in Fig 8.21. The main components of this are the 4-bit Binary up/down counters (4x74LS193). If the motor runs in the forward direction, a low-to-high transition on the input advances the count by one. Conversely, if the motor runs in the reverse direction a pulse on the input decreases the count by one. The total count number, which can be 16-bits long, represents the actual position relative to the start point.

The counter can be reset either manually or automatically, when the whole microprocessor-controlled system is started.

8.4.5 BCD COUNTER CIRCUIT AND DISPLAY

The BCD counter circuit of Fig 8.22 is used to provide a visual display of the motor speed.

The heart of this circuit is the (7224) 4-decade counter driver (RSdata3970) which drives directly the 7-segment common-anode LCD displays. The device count is controlled using a pair of commands (STORE and RESET) generated in a manner similar to that of the binary counter. Using an AND
gate, the input pulse train is gated with the BCD counter gating signal G2, which is generated from the microprocessor controller (section 8.5.3.5). The counter active time is again 12 ms, although the hold time is relatively long at about one second. Fig 8.22 shows both the BCD counter and its related circuits, including the display components and the control command (STORE, RESET) generator. The on-board oscillator of the 4-decade counter driver is designed to run freely at approximately 16 kHz. The oscillator frequency is divided by 128 to provide the backspace frequency of about 125 Hz with the oscillator running freely.

8.4.6 DEMAND POSITION SPEED INTERFACING CIRCUITS

The previous sections concentrated on the measurement of speed and rotor position in a form suitable for the controller. However, interfacing the demand speed and position into the system is of equal importance, and it is vital for the demand signals and the actual speed and position signals to be of the same form, so that they can be compared easily within the control system. The demand speed is commonly set by using either a thumb wheel or a binary coded rotary switch. These are each available as hexadecimal or decade (decimal) switches to provide a 4-digit output.

In the experimental unit, 4-decade switches were used to convert a demand speed range up to 9999 rpm to a 16-bit BCD number, and this requires the use of the simple interfacing circuit of Fig 8.23. The 16-bit BCD number is sampled by the microprocessor and converted into a 14-bit binary number in the software.
8.4.7 MOSFET GATE DRIVE PULSE GENERATOR

The mosfet gate drive signal is derived from the value of $D_n$ which is output by the microprocessor. This 8-bit number is applied to one of the two inputs of an 8-bit comparison circuit, consisting of two cascaded comparators (7485). The other input is obtained from an 8-bit count circuit, comprising two cascaded counters (74HCT161), which index from 0 to 255 and are then reset by the TC pin of the second counter, as in Fig 8.24(a). The input to the counter is a 7.5 MHz pulse train. The TC output of the second counter is also connected to the S-input of an R-S flip-flop, to trigger the positive-going edge of the generated pulse $T_s$ in Fig 8.24(b). When the counter output equals $D_n$, the comparator circuit output assumes a logic state 1. This is applied to the R-input of the R-S flip-flop to trigger the negative edge of $T_s$ which appears at the Q-output of the flip-flop.

8.5 MICROPROCESSOR-CONTROLLED CLOSED-LOOP CONTROL SYSTEM

The microprocessor field is one of the fastest developing industrial activities. Many powerful microprocessors exist and are utilised in variable-speed-drives to perform complicated tasks by executing digital control algorithms stored in their memory. Due to recent developments in semiconductor manufacturing technology, many of the sophisticated control techniques now available have become economic with the application of microprocessors [21]. Both 8-bit and 16-bit microprocessors are widely used in industry. In the work described in the thesis a 16-bit device was used in order to achieve the required high accuracy. Considerations of the capability, hardware structure, software compatibility, and equipment availability led to the use of an Intel 8086 for the present project.
8.5.1 INTRODUCTION OF 8086

The 8086 family was first made available by INTEL in 1978. It rapidly became popular, not only because it was the first 16-bit microprocessor but also because it contains features which made it attractive for many applications. It has 16-bit internal and external data paths, one megabyte of memory address space $2^{20}$ and a separate 64k byte $2^{16}$ I/O address space.

Many features of the 8086 are derived from its predecessor (the 8080), and the 8086 maintains software compatibility with the 8080. It is not difficult to translate an 8080 assembly language program into an equivalent 8086 program. The 8086 is easy to use in multiprocessor systems because of its bus-locking capabilities. It is also well suited for operation with a co-processor.

The architecture of the 8086 has new elements not found in 8-bit processors. The processor can be divided into two concurrent working parts—the execution unit and the bus interface unit—with communication to external devices being fully organized by the bus interface unit.

The 8086 addresses the one megabyte memory in a rather unusual way; the CPU itself operates on "logical" address in a 64k range but the bus interface unit translates these "logical" addresses into 20-bit "physical" addresses which appear on the external bus.

The 8086 device may be used in two configurations, called respectively minimum mode and maximum mode. The minimum mode 8086 is for small to medium single CPU systems. Its system architecture is directed at satisfying the requirements of the lower to middle segment of high performance
16-bit applications. The maximum mode extends the system architecture to support multiprocessor configurations, and local instruction set extension processors (co-processors).

8.5.2 IMPLEMENTATION OF THE 8086 MICROCONTROLLER

The hardware configuration for the closed-loop DC drive system is shown in Fig 8.25, where the box with intermittent lines represent the software functions of the microcomputer.

The demand speed/position is set by the interface circuit discussed in section 8.4.6. A speed/position switch indicates either position and speed control or speed control alone, and the forward/reverse switch shows the required direction of motor rotation. The start/stop switch enables the operator to stop the motor at any time.

The speed and position feedback signals, which are obtained from the measurement circuit of section 8.4, are interfaced with the microcomputer via the input port. The sign bit produced by the speed monitor, which indicates the direction of rotation, is also applied to the microcomputer via the input port.

The output port carries a 16-bit binary number which indicates the pulse width of the PWM signal. This signal is applied to the PWM generator, which generates the PWM signal of the required pulse width.

8.5.2.1 SYSTEM CLOCK

The 8086 microprocessor requires an external clock signal with a frequency of 5 MHz. An optimum 33% duty cycle clock, with the required voltage levels and transition times, can be obtained using the 8284 clock generator of Fig 8.26.
Either an external frequency source or a series resonant crystal may drive the 8284. A 15MHz crystal is used in the project.

There are three frequency outputs from the 8284 clock generator; the system clock CLK which runs at one-third of the crystal frequency and is used to drive the CPU; the oscillator frequency OSC which equals the crystal frequency and a peripheral clock that runs at one half the CPU clock frequency.

8.5.2.2 ADDRESS LATCH CIRCUIT

Since the 8086 uses a multiplexed data/address bus, address latches must be used to memorize the address when the processor sends data out through the same shared address/data bus. The 8282 latch is an ideal chip to separate the address from the shared address/data bus (Fig 8.27).

To achieve this, the processor sends a signal on the ALE (Address-Latch-Enable) pin, as a notification that it is outputing an address on the shared address/data bus. This signal is then placed on one of the 8282 pins, called the STB pin, to enable the chip and thereby to memorise the address.

8.5.2.3 DATA AMPLIFICATION

Although there is normally no need to latch the data, the processor is limited in the number of peripherals that it can drive. This limitation may be overcome using a data amplifier, which receives the data and after amplification
transmits it to the required peripherals. The amplifier must be bidirectional, to enable data to flow from the processor to the rest of the system and vice versa.

The 8086 family includes the 8286 chip, which is a transceiver, with eight pins that serve for data input and another eight for data output. The transceiver can however interchange the roles of the two sets of pins, so that data can pass in either direction. The chip has two control pins OE and T, the former being used to indicate data flow through, while the T pin controls the direction in which data is transmitted.

Fig 8.28 shows the connection between the 8086 processor, the 8282 address latches and the 8286 transceivers.

8.5.2.4 MEMORY UNITS

The microprocessor controller uses EPROM memory to store the program and RAM memory to store the data generated by operation of the microprocessor.

Based on the size and nature of the program, a 4k ROM, 1k RAM should be adequate. However, since the cost of high-memory capacity is almost the same as that of a low-memory unit there is a tendency to build large memory units. At the time the controller was built, there was a shortage of 4k(or below) EPROM and RAM, so that the 8k x 8-bit EPROM 27C64 and 8k x 8-bit RAM 6264 were used.

When the microprocessor selects a memory chip, the read or write operation must be completed before the read or write signal disappears from the microprocessor and, in this respect, the chip access time is very important. Both EPROM and RAM were chosen with 150ns access time.
Care is also necessary when enabling the memory chips. If several logic gates are connected in series, there will be considerable extra delay, which might make the memory access time much longer than 150ns and cause a failure of the system timing.

Since a 16-bit memory is required, two 2764 chips are combined to form a 8Kx16bit ROM, and two 6264 chips are combined to form a 8Kx16bit RAM, as shown in Fig 8.29.

8.5.2.5 PROGRAMMABLE INTERVAL TIMER

The 8253 timer used with the Intel microcomputer system has three independent programmable counters. Each counter has 6 modes to select from, which can also be cascaded to enable counting up to $2^{18}$.

As shown in Fig 8.30, counters 0 and 1 are cascaded to create a pulse repetition rate of 12 ms duration. The counters are loaded with a corresponding 16-bit number, which is decremented at a rate controlled by the clock frequency of the counter. When the count reaches zero, the output of counter 1 is raised to a high level (mode 0). This generates an interrupt signal to inform the processor that a new speed/position sample is ready and is appropriately called the sampling clock. The high level is maintained for 35μs, as set by software, before the counters are loaded again and a new count started.

A logically inverted version of the sampling clock G1 is used as a gating signal in the speed monitor circuit described previously in section 8.4.
Counter 2 is programmed as a square-wave generator. The output signal G2 is used as a gating signal for the DISPLAY discussed in section 8.4.5.

The maximum frequency that can be applied to the CLK pins of the 8253 counters is 2 MHz, so the 15MHz clock signal from the clock generator 8284 is divided by 8 using counter (74HCT160) to provide a 1.875 MHz clock frequency to CLK 0 of the 8253 timer.

8.5.2.6 PROGRAMMABLE PERIPHERAL INTERFACE

Input/output interface circuits are required to enable the control system to communicate externally. The Intel 8255 can be used as a programmable I/O component to interface equipment to the microcomputer system bus. The functional configuration of the 8255A is programmable by the system software, so that no external logic is normally necessary to interface peripheral devices or structures.

The 8255A chip has 24 I/O pins, which can be individually programmed in 3 groups of 8 and used in 3 major modes of operation. The three groups of 8 pins form three 8-bit Input or Output ports. In the case of the 16-bit microcomputer, two chips are combined to form three 16-bit Input/Output ports. As shown in Fig 8.31(a), ports A and B are programmed as Input ports, using port A for the demand speed and port B for the feedback speed. Port C is an Output port, which provides a 16-bit number representing the pulse width to the PWM signal generator.

Another set of 8-bit I/O ports (8212 chips) are used to provide a further 16-bit Input port for position feedback.
Since the 8212 chip contains an 8-bit latch as well as a 3-state output buffer no extra latches are needed, and the data from the position counter can be applied directly to the chips and latched. The latched data will not appear at the data bus until a signal is output by the microprocessor to enable it.

The actual connection of the chips is shown in Fig 8.31(b).

8.5.2.7 PROGRAMMABLE INTERRUPT CONTROLLER

Microcomputer system design requires that I/O devices, displays, sensors and commands such as emergency stop receive service in an efficient way, in order that a large proportion of the total system tasks can be undertaken by the microcomputer with little or no effect on the throughput. Any desirable method of servicing such devices will allow the microprocessor to execute its main program, and only stop to service peripheral devices when it is instructed to do so by the device itself. In effect, the method provides an external asynchronous input that informs the processor that it should complete whatever instructions are currently being executed, and calls a new routine that will service the requesting device. Once this servicing is complete the processor will resume its previous tasks exactly where it left off. This method is called interrupt, in which a programmable interrupt controller (PIC) is used to function as an overall manager in an Interrupt-Driven system environment, as shown in Fig 8.32.

In this thesis, a PIC 8259 is programmed to operate in the fully nested mode, in which the interrupt requests are ordered in priorities from 0 to 7. It will be seen from Fig 8.33 that the highest priority of interrupt request IRO is the emergency stop. If there is a stop signal, the PIC
immediately sends an interrupt signal to the microprocessor. The microprocessor then stops its main program and executes the stop subroutine, which in turn stops the motor drive. The next interrupt request priority goes to the overcurrent protection. When an overcurrent interrupt request is received, the microprocessor forwards an inhibit signal to all the PWM drive signals, so as to cause the motor to stop. The sampling request is connected to IR2, with a priority next to that of overcurrent protection. On receipt of this request, the PIC sends a interrupt signal to the microprocessor, with an address which indicates the location of the sampling subroutine in the program. The microprocessor then begins to execute the sampling procedure.

8.5.2.8 INTERFACING THE 8086 CPU WITH MEMORY AND I/O DEVICES

The 8086 microprocessor can communicate with both standard semiconductor memory components and Input/Output devices. The latter may be addressed by isolated I/O architecture, which separates the memory address space from the I/O address space and uses a conceptually simple transfer technique to or from the accumulator. Such an architecture is easy to understand, since I/O devices communicate only with the accumulator using the IN or OUT instructions. In addition, the full memory address space of 64K is unaffected by the I/O devices addressing due to their separation. The I/O ports may therefore be addressed from 0-256, which can be specified directly in the IN/OUT instructions, despite the same addresses being used in memory. For these reasons, an isolated I/O architecture is used in this 8086 system. An alternative form of I/O addressing is the Memory Mapped Input/Output. By assigning an area of memory address space,
the Input/Output can be manipulated with the same instruction used to manipulate memory locations. The advantage of this method is that it can achieve a significant increase in the overall speed of execution.

Fig 8.34 shows the memory and I/O maps and the chip selecting circuit. The 74139 is a high speed 3-to-8 binary decoder which accepts 3-bit binary code and, by gating this input, creates an exclusive output that represents the value of the input code. The \( T\bar{O}/M \) pin indicates whether or not it is to address either the memory or the I/O devices. The \( \bar{BHE} \) indicates whether 16-bit or 8-bit data is required. \( A_0 \) and \( \bar{BHE} \) are combined to ensure the even address of RAM.

8.5.3 SOFTWARE DESIGN

The software consists of several routines, and is responsible for the following tasks:

a) Reserving memory space for initial values and constants.

b) Programming the microcomputer peripheral chips.

c) Loading the interrupt vector table.

d) Sampling the actual and the demand position/speed.

e) Calculating the converter duty cycle.

f) BCD-to-Binary conversion.

g) Over-current protection.

h) Emergency stop.
The overall aim of the software is to bring the actual position of the motor to the demand value as rapidly as possible, with both speed and maximum current being kept under control.

Tasks(a) to (c) can clearly be included in an initialisation process, as part of the main routine executed at the beginning of the program. Task(d) has a periodic nature and occurs only when a position/speed sample is ready. It can thus be kept under the control of an external timer acting as a sampling clock, which informs the CPU via an interrupt that a new position/speed sampling is ready. The microprocessor is predominantly occupied in performing task(e), which acts as the PID controller.

Since the demand position/speed is in the form of BCD code, task(f) converts the BCD code into the Binary form in order to simplify the calculation.

Task(g) prevents the armature current from exceeding a pre-determined limit, by controlling the converter duty cycle and thus reducing the output voltage should this be necessary. It is also appropriate to control the maximum current to a level that the converter semiconductor switches can withstand. If the current attempts to exceed this limit, the CPU is informed through its interrupt and executes an emergency stop by inhibiting the gate drive signal.

The purpose of task(h) is to stop the motor when required. To achieve this, a drive signal with a 50% duty cycle is output to provide zero output voltage to the armature.

The simplified block diagram of Fig 8.35 shows that the main tasks considered above are performed by four routines, namely POWER-UP, OVERCURRENT, STOP and CONTROL-ALGM, each
of which has its own structural nature and includes specially designed subroutines. The routine POWER-UP establishes the initial conditions for the control system and ensures that the motor remains stationary, before setting the demand position/speed and programming the peripheral chips. The routine OVERCURRENT is initiated by interrupting the microprocessor via the IR1 of the 8259 interrupt controller. It serves to prevent overcurrent, as required by task(g) above.

Tasks(d), (e) and (f) are performed jointly by CONTROL-ALGM, which is started by the sampling clock interrupting the processor via IR2 of 8259. In addition to sampling the position and speed, CONTROL-ALGM converts these to binary code through a BCD-to-Binary conversion subroutine and determines the converter duty cycle by comparing the demand value with the actual value and processing the result by the PID algorithm. The STOP routine is executed by sending an interrupt request through IR0 to the CPU to set the duty cycle to 50%.

8.5.3.1 POWER-UP ROUTINE

When the power supply activates the microcomputer the processor is reset and automatically loaded with addresses FFFFFH, where a JUMP instruction causes the CPU to go to the start address of the POWER-UP routine. The flow chart for this routine shown in Fig 8.36 starts with an initialization process, which includes reserving memory space for initial values and constants, loading the vector table which stores the start addresses of the interrupt subroutines, programming the PPI 8255 chip (to assign Port A and Port B as Input ports, and Port C as an Output port) and the Timer 8253 chip (to assign Timer 0 and Timer 2 to operate in mode 3, with Timer 1 in mode 0). The program then clears the interrupt flag to halt any interrupt request before receiving a START
command. To keep the motor at stand-still, a 50% duty cycle signal is output from the controller. After this, the processor checks the START/STOP flag. If it is START, the sampling period is loaded into Timer 1 to start counting down. The interrupt flag is enabled and the processor enters a WAIT state until it receives any interrupt requests. If it is STOP, the program keeps the motor at stand-still and re-checks the START/STOP status.

8.5.3.2 OVERCURRENT ROUTINE

This routine is executed when the armature current exceeds the preset maximum value. As can be seen from Fig 8.37, the routine begins by inhibiting any interrupt request, before resetting the $PC_{15}$ pin of Port C. This logic 0 of $PC_{15}$ together with the converter gate drive signals are applied to AND gates so that all gate signals are inhibited. The motor is then stopped and remains stationary until the processor is reset.

8.5.3.3 STOP ROUTINE

Fig 8.38 shows the flowchart for the STOP routine, which is the highest priority interrupt subroutine and consequently allows the operator to stop the motor immediately. As with the OVERCURRENT routine, it first disables the interrupt request before sending a 50% duty cycle signal through Port C to stop the motor. The processor continues to check the START/STOP status and, upon receiving a START command, the program returns to the main program and waits for the next sample.
8.5.3.4 CONTROL-ALGM ROUTINE

CONTROL-ALGM is the IR2 interrupt service routine which performs the tasks of sampling the position/speed and calculating the converter duty cycle. It also limits the armature current to below the rated value.

The flowchart for the CONTROL-ALGM routine in Fig 8.39 shows that the routine first calls the DELAY subroutine, which gives a 35μs delay before restarting the sample period counting. This delay causes the output of Timer 1 to remain high for approximately 50μs (35μs plus 15μs consumed in calling the CONTROL-ALGM interrupt subroutine). Inversion of this output (defined as G1 in Section 8.4.3) is used as the gating signal for speed sampling. The 50μs duration used for storing and resetting related chips was discussed in detail in Section 8.4.4. The processor then loads Timer1 with the sampling period and automatically starts to count again. After the feedback speed has been input, the processor checks its D14 bit, which is used as an overcurrent flag. If D14=1 the armature current exceeds the rated value. In this case the current control loop is closed, as shown in Fig 8.12 (details of the current limit protection were discussed in Sections 8.3.3.3 and 8.3.3.4). After this, the processor checks the POSITION/SPEED flag D13. If D13=0, the reference data from Port B is the demand speed and the processor is in the speed control mode. Conversely, if D13=1 the reference data at Port B is the demand position and the processor is in the position control mode. It initially executes position control by inputing both demand and feedback positions. Since the demand position is in the form of a BCD code, it is first converted into binary code by calling the BCD-to-Binary Conversion Subroutine. The error between demand and feedback positions is sent to the PD controller discussed in detail in the next section. The resultant output of the position controller is used as a
speed reference in the speed controller where, in order to ensure a soft-start, the processor first checks that the motor is stationary. If so the maximum speed reference is set at 50 rpm, and the error between the reference and the actual speed is applied to the PID controller described below. The output of the PID controller is converted into the correct duty cycle by Control Algorithm 3, described previously in Section 8.3.3.4. The result is output through Port C to the PWM gate pulse generator shown in Fig 8.24. Finally the processor enables all interrupt flags and returns to the main program to wait for next sampling period.

8.5.3.5 CONTROL ALGORITHMS

The control algorithms described in section 8.3.3.4 are employed in the CONTROL-ALGM subroutine. Fig 8.40(a) shows the flowchart of control algorithm 1 (PD controller). The processor first sets the position error limit at 10 revolutions. If this is exceeded, the PD controller saturates and the motor runs at the preset maximum speed. From the current error $e$, and the previous error $e_{n-1}$, the speed reference $X_{dm}$ is calculated through the PD controller, as discussed in Section 8.3.3.4.

Fig 8.40(b) shows the flowchart of Control Algorithm 2. The error between $X_{dm}$ and the actual speed $X_n$ is applied to the integrator and the processor then considers the current limit. If there is overcurrent (Cl is set), the absolute value of the integrator $I_n$ is reduced by one step Cl. The error between $X_{dm}$ and $X_n$ is amplified by the proportional gain $K_p$, with the result being added to that of the Integrator $I_n$. There is a upper and lower limit for the output of the PID Controller $V_c$ which will determine the maximum and minimum duty cycle in control algorithm 3.
The flowchart for control algorithm 3 is shown in Fig 8.40(c). As described in Section 8.3.3.4, four different formulae are used to calculate the duty cycle, depending on which region \( V_n \) is in. The final result, which represents duty cycle will be output to a pulse generator to generate the required converter duty cycle.
Fig 8.1 Conventional Control For DC Drive System

Fig 8.2 Position-Speed-Current Three-Loop Control For DC Drive System
Fig 8.3 Typical Time Response Of Second-Order System

Fig 8.4 Log-Magnitude Plot of Open-Loop Frequency Response
**Fig 8.5(a) Type I System**

**Fig 8.5(b) Open Loop Magnitude-Frequency Characteristics Of Type I System**

**Fig 8.6(a) Type II System**

**Fig 8.6(b) Open Loop Magnitude-Frequency Characteristics Of Type II System**
Fig 8.7 PID Controller
Fig 8.8 Separately-Excited DC Motor

Fig 8.9 Functional Block Diagram of Motor Transfer Function
Fig 8.10 Functional Block Diagram of Position-Speed Control System

Fig 8.11 Speed Control With Interventionist Current Limited
Fig 8.12 Block Diagram Of Digital Control System
Fig 8.13 Relationship Between $V_c$ And $D$

a) Converter Output Voltage  b) Region I

Against Duty Cycle

c) Region II  d) Speed Sub-Region
Fig 8.14 Block Diagram Of Speed Measurement Circuit
Fig 8.15 Block Diagram Of Position Measurement Circuit
Fig 8.16 Encoder Pulse Frequency Multiplication
(a) Circuit Diagram
(b) Pulse Sequence
**Fig 8.17 Direction Detection Circuit**
Fig 8.18 Direction Detection Pulse Sequence
(a) Forward Direction
(b) Reverse Direction
Fig 8.19 Counter Gating Signal Generation
Fig 8.20(a) Binary Counting Circuit For Motor Speed
GATING SIGNAL C

STORE LATCH SIGNAL

COUNTER RESET SIGNAL

ENCODER CIRCUIT OUTPUT

GATE PULSES FOR COUNTER

\[ a = \text{COUNTER HOLD TIME} \]
\[ b = \text{STORE TIME} \]
\[ c = \text{RESET TIME} \]
\[ d = \text{COUNTER ACTIVE TIME} \]

Fig 8.20(b) Pulse Sequence
Fig 8.21 Binary Counting Circuit For Motor Position
Fig 8.22 Circuit Diagram For BCD Counter And Display Of Motor Speed
Fig 8.23 Demand Speed/Position Interfacing With 4-Decade Switches
From Port C

PWM SIGNAL

(TO DRIVE CIRCUIT)

Fig 8.24(a) PWM Signal Generation Circuit
Fig 8.24(b) Pulse Sequence Of PWM Pulse Generator
Fig 8.25 Hardware Configuration Of Closed-Loop Controlled DC Drive System
Fig 8.26 8284 Clock Generator

Fig 8.27 Separating Address From Shared Address/Data Bus
Fig 8.28 Using Transceivers To Boost Data Bus
Fig 8.29 8k X 16-bit EPROM And 8k X 16-bit RAM
Fig 8.30 8253 Timer
Fig 8.31(a) Programmable Peripheral Interface Circuit
Fig. 8.31(b) 16-bit Input Port Using 8212
Fig 8.32 Interrupt Method

Fig 8.33 8259 Interface to Standard System Bus
Fig 8.34 Memory And I/O Address Map And Chip Selecting Circuit
Fig 8.35 Software Tasks
Fig 8.36 Flowchart Of Power-Up Routine
DISABLE INTERRUPT

RESET OVERCURRENT SIGN (PC45)

OUTPUT 50% DUTY CYCLE

RETURN

START

DISABLE INTERRUPT

OUTPUT 50% DUTY CYCLE

NO

START

YES

ENABLE INTERRUPT

RETURN

Fig 8.37 Overcurrent Routine

Fig 8.38 Flowchart Of STOP Routine
Fig 8.39 Flowchart of CONTROL-ALGM
\[ e_n = \theta_{dm} - \theta_n \]

\[ \text{LIMIT} |e_n|_{\text{max}} \leq 100 \]

\[ \text{PD CONTROLLER} \]

\[ X_{dm} = e_n K_p + (e_n - e_{n-1}) K_d \]

\[ X_{dm} \text{ (SPEED REFERENCE)} \]

Fig 8.40(a) Control Algorithm 1
\[ \Delta \omega_n = X_{ds} - X_n \]

\[ I_n = I_{n-1} + \Delta \omega_n K_f \]

\[ I_n \geq 0 ? \]

\[ I_n = I_n - C_1 \]

\[ I_n = I_n + C_1 \]

\[ V_n = I_n + K_p \Delta \omega_n \]

\[ V_n \geq 0 ? \]

\[ \text{LIMIT } V_n \leq V_{\text{max}} \]

\[ \text{LIMIT } V_n \geq V_{\text{min}} \]

Fig 8.40(b) Control Algorithm 2
Fig 8.40(c) Control Algorithm 3
CHAPTER 9 EXPERIMENTAL STUDIES

This chapter discusses the experimental performance of the DC-to-DC converter, the microcontroller and the closed-loop DC drive system. Comparisons are made between practical and theoretically predicted results.

9.1 DC-to-DC CONVERTER PERFORMANCE

A photograph of the prototype 4-quadrant converter is given in Fig 9.1(a), and a circuit diagram showing the power components in Fig 9.1(b). The converter output is loaded by a directly-coupled motor-generator set.

Figs 9.2(a) and (b) show waveforms of the gate-drive voltages for the four switches $S_1$-$S_4$ under forward and reverse operation respectively. It is seen that $S_1$ and $S_3$ are switched complementarily with $S_2$ and $S_4$.

Fig 9.3(a) and (b) illustrate the performance of the two bimos switches $S_1$ and $S_2$, at maximum output voltage of +180V and -180V respectively. The voltage waveforms across the two switches show that a rapid switching speed is achieved, with switch-on and switch-off times of less than 1 $\mu$s. If the on-time of $S_1$($t_1$) exceeds that of $S_2$($t_2$), as in Fig 9.3(a), the peak voltage across $S_1$, which is equal to the output voltage of the upper converter $V_{c1}$, exceeds that across $S_2$, which is equal to the lower converter output voltage $V_{c2}$. On the other hand, if $t_2$ exceeds $t_1$, the peak voltage across $S_2$ exceeds that across $S_1$, as shown in Fig 9.3(b).

Fig 9.4 shows the effect of the switching duty cycle on the output voltage of the converter. When the duty cycle $D$ (based on $S_1$) exceeds 50% $V_{c1}$ exceeds $V_{c2}$ and the overall output voltage ($V_o=V_{c1}-V_{c2}$) is positive. Conversely, if $D$
is less than 50\%, \( V_{c1} \) is less than \( V_{c2} \) and \( V_o \) is negative. When \( D = 50\% \) \( V_{c1} \) equals \( V_{c2} \) and \( V_o = 0 \). These results show good agreement with the theoretical predictions obtained by computer simulation in chapter 5.

The converter output voltage ripple is shown in Fig 9.5, for an output voltage of about 180V. The ripple voltage \( \Delta V_o = 5V \) is less than the design maximum of 10\% of the output voltage.

Fig 9.6 shows the inductor current waveform \( I_{li} \), the drive signal and the voltage across the switch \( S_1 \) and the output voltage \( V_o \). It can be seen that when the drive signal goes high, the switch closes and the inductor current, which passes through the switch as discussed in chapter 3, ramps up. When the switch opens, the inductor current is diverted to charge the output capacitor and it ramps down until the switch is again turned on.

9.2 CLOSED-LOOP OPERATION

In the following sections various circuit waveforms are presented for the closed-loop system described in chapter 8.

9.2.1 CLOSED-LOOP CIRCUIT WAVEFORMS

A photograph of the experimental closed-loop system appears in Fig 9.7. The system comprises the microcontroller board and the measuring and interface board.

Fig 9.8 illustrates the operation of the direction detection circuit described in section 8.4.2. Fig 9.8(a) shows the shaft encoder outputs A and B for forward rotation, with A lagging B by 90°. Signal Q, provided by the direction detection circuit, is similar to B for forward operation.
and, since it results in logic 0 at the output of the direction detection circuit, it confirms the pulse sequence of Fig 8.18(a). Fig 9.8(b) shows corresponding waveforms for reverse rotation, with output A now leading output B by 90°. Signal Q is similar to $\bar{A}$, which results in a logic 1 output from the direction detection circuit and again confirms the pulse sequence of Fig.8.18(b).

Fig 9.9 shows waveforms for the encoder output interface circuit discussed in section 8.4.1, in which the shaft encoder output frequency is quadrupled. The two upper traces show the encoder outputs A and B, from which the double-frequency signal of the third trace is obtained as the output signal X from the exclusive-OR gate of the circuit of Fig 8.16. The frequency is again doubled within this circuit to provide the signal shown in the lowest trace.

The gating signals for the binary counters of the speed measurement circuit and the BCD counter of the display driver are shown in Fig 9.10. These are generated using the clock circuit formed by the Programmable Timer 8253 of Fig 8.19. The signal G1 for the binary counter has a count-duration of 12 ms and a hold-duration of about 50μs, with G2 providing the BCD counter with a similar count-duration of 12 ms but a longer hold-duration of about 1 s.

The high-to-low transition of G1 generates a sampling request signal to the microprocessor through the interrupter controller every 12 ms. This sampling request signal should last sufficiently long to be acknowledged by the microprocessor, and this is set at 50μs by the software.

The binary counter waveforms for the motor speed detection circuit are presented in Figs 9.11 and 9.12. As explained in Section 8.4.4, the store pulse used to update the
D-latches of Fig 8.20(a) is generated at the end of the gating signal, as shown in trace 2 of Fig 9.11. The counter reset pulse is generated at the end of the store pulse duration, in accordance with the pulse sequence shown in Fig 8.20(b). The interfaced encoder output pulses and the binary gating signal are shown in Fig 9.12. These two signals provide the gated input to the counter circuit, as discussed in Section 8.4.4.

Fig 9.13 shows the binary counter waveforms for the motor position detection circuit. If the motor is rotating in the forward direction, the direction detection signal D is low and a count-up input pulse is obtained which increments the position counter. If the rotor direction is reversed, the direction detection signal D becomes high, and the count-down pulse then obtained decrements the position counter.

9.2.2 DRIVE SYSTEM RESPONSE WITH CLOSED-LOOP CONTROL

This section is concerned with the dynamic performance of the closed-loop drive system.

The experimental DC motor is coupled to a DC generator which acts as a load. The field windings of the two machines are supplied at 240V DC, and a 100Ω variable resistor is connected to the generator armature terminals.

Two D/A converters are used to provide analogue speed and position information and the motor armature current is measured using a Hall-effect current sensor.

9.2.2.1 SYSTEM RESPONSE TO SPEED DEMAND

Figs 9.14(a) and (b) show respectively the experimental drive response from standstill to a forward speed of 1000 rpm and also regenerative braking of the motor from this
speed to standstill. Predicted results for the same two conditions are given in Fig 9.15. It can be seen in Fig 9.14(a) that, when the motor is energised, there is an initial surge of armature current. The motor accelerates towards the demand speed, which it reaches without any overshoot, and the armature current drops to the value needed to maintain the demand speed.

To stop the motor, the switch duty cycle is reduced to 50%, causing the armature voltage to fall to zero. The armature current reverses as shown in Fig 9.14(b), providing a braking torque which, together with the load torque, rapidly decelerates the rotor to standstill. During this period, power is returned via the converter to the supply and regenerative operation is achieved. The predicted results in Figs 9.15(a) and (b) are in general agreement with the experimental results.

The drive response for reverse operation in Figs 9.16(a) and (b) provides results corresponding to those of Fig 9.14. Fig 9.16(a) shows the response from stand-still to a reverse speed of 1000rpm and Fig 9.16(b) that from a reverse speed of 1000rpm to stand-still.

Fig 9.17 shows the motor response to a change in direction. With the duty cycle changing between 80% and 20%, the armature voltage changes from positive to negative and back to positive, as does the armature current and speed. A fast, stable and accurate response is thus once again demonstrated. Predicted result of the drive response from forward to reverse operation given in Fig 9.18 are in generally good agreement with the experiment results.
9.2.2.2 SYSTEM RESPONSE TO POSITION DEMAND

Fig 9.19 illustrate the drive response to a position demand in terms of the number of revolutions, which is set at 100. As described in section 8.5.3.5, the initial position error $\Delta \theta (=100)$ is sent to the position PD controller. Since it exceeds the error limit, which is preset at 10 revolutions, the controller saturates and a maximum speed reference is applied to the speed controller. The motor runs at maximum speed until the position error becomes less than 10 revolutions, when the PD controller becomes active. The motor speed gradually reduces, following the decrease in the position error, and eventually stops when the demand position is reached.

9.2.2.3 SYSTEM RESPONSE TO LOAD VARIATION

If a change occurs in the load, the dynamic properties of fast response and good stability are required. To illustrate these for the experimental drive, Fig 9.20(a) shows the response following an increase in the load current produced by a sudden increase of the load on the generator. The initial speed drop is followed by a rise in armature current, to increase the motor torque and return the motor to the demand speed. As can be seen, the dynamic variation of speed is quite small and the recovery time is short. This very desirable property is also evident in Fig 9.20(b), which illustrates the case when the generator load is suddenly reduced. The initial rise in speed is followed by a fall in armature current to reduce the motor torque as the motor decelerates to the demand speed. The predicted results for the system response in Fig 9.21 are again very similar to the corresponding practical results.
Fig 9.1(a) The Prototype 4-Quadrant DC/DC Converter
Fig 9.1(b) Circuit Diagram Of 4-Quadrant DC-DC Converter
Fig 9.2 Gate Drive Pulse Sequence
(a) Forward Direction
(b) Reverse Direction
Fig 9.3 Performance Of The Bimos Switches
(a) $t_1 > t_2$
(b) $t_1 < t_2$
Fig 9.4 The Effect Of Duty Cycle On Output Voltage
Fig 9.4 Effect of Duty Cycle On Output Voltage

(a) D=86%
(b) D=14%
(c) D=50%
Fig 9.5 Output Voltage Ripple

Fig 9.6 Drive Signal And Converter Voltage And Current
**Fig 9.8 Direction Detection Circuit Operation**

(a) Forward Operation  
(b) Reverse Operation
Fig 9.9 Shaft Encoder Pulse Frequency Multiplication

Fig 9.10 Gating Signal For Speed And Position Counter
Fig 9.11 Control Pulse Generation For Binary Counter Circuit

Fig 9.12 Binary Counter Circuit Gating Principle
Fig. 9.13 Pulse Generation For Position Counter
(a) Forward Operation
(b) Reverse Operation
**Fig 9.14(a) Drive Performance From Stand-still To Forward Speed Of 1000rpm (No Load)**

**Fig 9.14(b) Regenerative Braking From Forward Speed Of 1000rpm To Stand-still (No Load)**
Fig 9.15(a) Predicted Results Of Drive Performance From Stand-Still To Forward Speed Of 1000rpm (No Load)
Fig 9.15(b) Predicted Results Of Drive Performance From Forward Speed Of 1000rpm To Stand-still (No Load)
Fig 9.16(a) Drive Performance From Stand-Still To Reverse Speed Of 1000rpm (No Load)

Fig 9.16(b) Regenerative Braking From Reverse Speed Of 1000rpm To Stand-Still (No Load)
Fig 9.17 Drive Response To Speed Reversal (No Load)
Fig 9.18 Predicted Drive Response To Speed Reversal (No Load)
Fig 9.19 Drive Response To A Demand Position Of 100 revolutions
Fig 9.20(a) Drive Response To Load Increase From No-Load To Full Load

Fig 9.20(b) Drive Response To Load Decrease From Full Load To No-Load
Fig 9.21(a) Predicted Drive Response To Load Increase
From No-Load To Full Load
Fig 9.21(b) Predicted Drive Response To Load Decrease From Full Load To No-Load
CHAPTER 10 CONCLUSIONS

This thesis has described a new topology of 4-quadrant switched-mode DC-to-DC converter and its successful application to a 1.2kW microprocessor-controlled DC servo drive.

To meet the demand of high-power battery-operated DC variable-speed drives and switched-mode power supplies, this novel converter has been designed to be capable of providing a substantial step up of voltage and of varying its output continuously between maximum voltage in both forward and reverse directions.

Since the development is based on the existing boost converter, through the complementary operation of two symmetrically arranged units, it is cost-effective and possesses all the major advantages of the basic DC-to-DC converters, including an excellent dynamic performance and a high efficiency. Both features arise since the power translation is accomplished through ideally non-dissipative inductive and capacitive components, leaving only parasitic resistance and non-ideal switches contributing to the total power loss.

The steady-state and dynamic performance of the new converter was examined extensively using mathematical modelling. A complete linearised mathematical model has been developed, and input-to-output and duty cycle-to-output transfer functions were derived using the State-space Average Method.

In the practical implementation of the converter, efforts were made to maximise the efficiency and minimise the overall size, on which the switching frequency has a major effect. Computer simulation revealed that, for the 1.2kW converter considered in the thesis the optimal frequency is between 30 to 40kHz.
Both theoretical and practical investigations have shown that the switching speed and the rating of the power semiconductor devices are the main factors limiting the output power of switched-mode power converters. To make full use of existing devices, hybrid arrangements, which combine beneficial characteristics and overcome undesirable features, are an effective and economic way of increasing both the switching frequency and the power rating. In this thesis, power mosfets and power bipolar transistors are cascaded to form switching devices (Mos-Gated-Bimos), in which the high switching speed of mosfets and the high power rating of bipolar transistors are combined. It is believed that this merging of the different existing transistor technologies represents an important trend in the development of power semiconductors.

The microprocessor-controlled DC servo system implemented using the new converter is completely digital and does not involve either analogue-to-digital or digital-to-analogue conversion, thereby eliminating any inaccuracies associated with analogue circuits. This advantage is enhanced by the use of a 8086 microprocessor-based microcontroller, which has a capacity of 8K of 16 bits ROM, 8K of 16 bits RAM, 4 of 16 bits I/O ports and 8 interrupt requests, together with PD and PID control algorithms, a current limit algorithm and a duty cycle control algorithm. It increases the system versatility and also realizes with great flexibility a number of control functions that are otherwise difficult to achieve.

The closed-loop control system described in the thesis enables the motor shaft position and speed to be precisely controlled, and the motor armature current of the controlled motor to be limited to a maximum value without the need for a separate current feedback loop.
Since the duty cycle-to-output voltage transfer function obtained for the converter contains a right half-plane zero, it possesses a potential instability in closed-loop operation. The control gain coefficients of the PD and PID control algorithms within the microcontroller were tuned, such that the offending zero was cancelled and the system achieved high accuracy, fast response and good stability. Due to the rapid operation of the microprocessor, the current-limit algorithm effectively prevented the armature current from exceeding its rated value. The duty cycle control algorithm ensured that the duty cycle accurately tracked changes in the motor speed, in both the high-speed and low-speed regions.

The experimental and theoretical studies presented in the thesis indicate that the new converter is potentially a low cost and high efficiency drive unit, with full digital control and a superior 4-quadrant buck/boost operation. The theoretical and practical results presented respectively in Chapter 5 and Chapter 9 show generally good agreement for all the cases where the motor runs within the different quadrants and under different load conditions.

SUGGESTIONS FOR FURTHER WORK

Further research needs to be directed towards increasing the output power of the converter and this may be achieved by using more advanced semiconductor switches and/or by changing the structure of the converter circuit.

The Mos-Gated Bimos switch which was used is the result of combining two mosfets with one bipolar transistor. When high currents are switched with a high rate-of-change a high-voltage spike is often generated due to the stray inductance of the connection lead between the transistors. This gives rise to a difficulty in the protection circuit
design and limits the switched current level to below the rated value for the switch. The recently developed IGBT (Isolated-Gate Bipolar Transistor) however integrates the three transistors and protection circuit into one package such that internal inductance is eliminated and no voltage spike appears across the switch. As a result, the switched current may be increased up to the rated value of the devices and, with further development, the IGBT could replace the discrete bimos switch and lead to a converter with higher output power.

The development of SIT (Static Induction Transistor) devices also makes it possible to increase the converter power to tens of kilowatts, with switching frequencies up to about 100kHz without substantial increase in switching loss.

The main drawback of the present converter is that the switches have to withstand high peak currents and voltage. The structure of the converter circuit could be modified to reduce the currents and voltages handled by the switches, with the inductors in the converter circuit being replaced by transformers to isolate the input and output circuits. The switches would then need to handle either low-current and high-voltage or vice versa, and the output power of the converter could be increased without increasing the power rating of the semiconductor switches.
REFERENCE


18. Cheng, B. S., "Automatic Control System", Qing-Hua University, Peking, China, 1980


BIBLIOGRAPHY


APPENDIX I SWITCH POWER LOSSES

The current and voltage waveforms for mosfet IRFP450 under full load condition are shown in Fig 6.14(c), in which,

\[ V_D = 200V \quad t_{sun} = 62ns \quad t_{swf} = 110ns \]

\[ D = 0.94, \quad I_{D(ave)} = 8.6A \]

\[ I_A = 31A, \quad I_B = 11A. \]

\[ P_{sun} = \frac{V_D I_A t_{sun}}{2} f = 7.68W \sqrt{\text{}} \]

\[ P_{swf} = \frac{I_B V_D t_{swf}}{2} f = 4.84W \sqrt{\text{}} \]

\[ P_{con} = \frac{V_{sat} I_{D(ave)} T_{on}}{T} \]

\[ = DV_{sat} I_{D(sav)} \]

\[ = 24.3W \]

\[ P_{tot} = P_{swf} + P_{sun} + P_{con} = 24.33 + 7.68 + 4.84 = 36.85W \]

The current and voltage waveforms for the IRFZ42 are shown in fig 6.14(b), in which

\[ V'_{D} = 30V \quad t_{swf} = 195ns \quad t_{sun} = 85ns \]

\[ I_A' = 31A \]

\[ I_B' = 55A \]

\[ I'_{D(ave)} = \frac{I_A' + I_B'}{2} = 43A \]

Since two IRFZ42 are connected in parallel,

\[ R_{DS(on)} = 0.035/2 = 0.0175\Omega \]

\[ P_{sun} = \frac{I_A' V'_D t_{sun}}{2} f = 1.26W \sqrt{\text{}} \]
\[ P_{\text{swf}} = \frac{I_B V_D t_{\text{swf}}}{2} f = 2.51\, \text{W} \]
\[ P_{\text{con}} = I_D^2 R_{DS(on)} D = 19.5\, \text{W} \]
\[ P_{\text{tot}} = P_{\text{swf}} + P_{\text{swn}} + P_{\text{con}} = 23.24\, \text{W} \]

For BUS14, as shown in Fig 6.14(a),

\[ I_A'' = 24.8\, \text{A} \quad I_B'' = 44\, \text{A} \]
\[ I_{c(\text{ave})} = 34.4\, \text{A}, \quad V_{\text{sat}} = 1.5\, \text{V} \]
\[ V_c = 200\, \text{V} \quad t_{\text{swn}} = 100\, \text{ns} \quad t_{\text{swf}} = 0.5\, \mu\text{s} \]
\[ P_{\text{swn}} = \frac{I_A'' V_c t_{\text{swn}}}{2} f = 10\, \text{W} \]
\[ P_{\text{swf}} = \frac{I_B'' V_c t_{\text{swf}}}{6} f = 29.3\, \text{W} \]
\[ P_{\text{con}} = V_{\text{sat}} I_{c(\text{ave})} D = 47.25\, \text{W} \]
\[ P_{\text{tot}} = P_{\text{swf}} + P_{\text{swn}} + P_{\text{con}} = 86.25\, \text{W} \]
As discussed in chapter 6, the effective airgap cross-sectional area of a gapped ferrite core is greater than the physical dimensions, due to the fringe flux. For the core chosen, the additional pole face areas labelled E and F in Fig 6.7(a), can be calculated according to the curves shown in Fig 6.7(b), in which

\[ X = H + W/2 = 69 \text{ mm} \]

\[ g = \frac{\text{Airgap length}}{2} = 2.5 \text{ mm} \]

\[ \frac{X}{g} = 27.6 \]

From curve (a)
\[ \lambda = 2.6 \]

area \( E = 17 \times 2.6 = 44.2 \text{ mm}^2 \)

and \( C = 13, \ C/g = 5.2 \)

so that from curve (b)
\[ \lambda = 1.1 \]

area \( F = 68.5 \text{ mm}^2 \)

the effective cross-sectional area is therefore
\[ A_i' = 2E + F + A_i = 372.5 \text{ mm}^2 \]
APPENDIX III CALCULATION OF VOLTAGE GAIN
IN THE DISCONTINUOUS MODE

1. BUCK CONVERTER

Fig 3.4 shows the buck converter waveforms for discontinuous mode of operation. Consideration of the balance of the voltage-time integral of the inductor voltage \( V_L \) gives

\[
(V_s - V_o)t_1 = V_o t_2
\]

\[
t_2 = \frac{(V_s - V_o)t_1}{V_o}
\]

(11.1)

Since \( I_{L(au)} = I_o + I_c \)

where \( I_{L(au)} \) is the average inductor current

\( I_o \) is average load current

\( I_c \) is average capacitor current

Thus \( I_{L(au)} \) may be calculated as

\[
I_{L(au)} = \frac{1}{T_s} \left( \int_{t_1}^{t_1 + t_2} I_b dt + \int_{t_1}^{t_1 + t_2} I_b \left( 1 - \frac{t}{t_2} \right) dt \right)
\]

\[
= \frac{I_b (t_1 + t_2)}{2T_s}
\]

and the average load current

\[
I_o = \frac{V_o}{R}
\]

The average capacitor current \( I_c \) at steady state is zero, so,
or
\[
\frac{t_2}{2T_s} = \frac{V_o}{I_bR} - t_1
\]  
(11.2)

It follows from equations (11.1) and (11.2),
\[
\frac{V_s t_1}{l_v} = \frac{2T_s V_o}{l_b R}
\]

since

\[
I_b = \frac{V_s - V_o}{L} t_1, \quad D = \frac{t_1}{T_s}
\]

\[
\tau = \frac{L}{R T_s}, \quad M = \frac{V_o}{V_s}
\]

so,
\[
M^2 + \frac{D^2}{2\tau} M - \frac{D^2}{2\tau} = 0
\]

\[
M = \frac{D^2 (\sqrt{1 + 8\tau D^2} - 1)}{4\tau}
\]

or
\[
M = \frac{2}{1 + \sqrt{1 + 8\tau D^2}}
\]

2 BOOST CONVERTER

Fig 3.7 shows the discontinuous mode waveforms of the boost converter. Consideration of the balance of the voltage-time integral of the inductor voltage \( V_l \) gives

\[
V_s t_1 = (V_o - V_s) t_2
\]
Since \( I_{D(\text{av})} = I_o + I_c \)

where \( I_{D(\text{av})} \) is average diode current

\( I_{D(\text{av})} \) may be calculated as

\[
I_{D(\text{av})} = \frac{1}{T_s} \int_{t_1}^{t_1 + t_2} I_b \left( 1 - \frac{t - t_1}{t_2} \right) dt
\]

\[
= \frac{I_b t_2}{2T_s}
\]

and the average load current

\[
I_o = \frac{V_o}{R}
\]

the average capacitor current \( I_c \) at steady state is zero.

so,

\[
I_b t_2 = \frac{V_o}{2T_s \cdot R}
\]

or

\[
t_2 = \frac{2T_s V_o}{I_b R}
\]

(11.4)

It follows from equations (11.3) and (11.4) that

\[
\frac{V_s t_1}{V_o - V_s} = \frac{2T_s V_o}{I_R}
\]

since

\[
I_b = \frac{V_s t_1}{L}, \quad D = \frac{t_1}{T_s}
\]
\[ \tau = \frac{L}{RT_s}, \quad M = \frac{V_o}{V_s} \]

so,

\[ M^2 - M - \frac{D^2}{2\tau} = 0 \]

\[ M = \frac{1 + \sqrt{1 + \frac{2D^2}{\tau}}}{2} \]
APPENDIX IV PUBLISHED WORK
ABSTRACT

The paper describes theoretical and experimental considerations of a novel 4-quadrant PWM switched-mode dc/dc power converter. Computer simulations lead to an optimum switching frequency, which minimises the size of the circuit inductors while maintaining a high unit efficiency. From this basis, a 40 kHz 1.7 kW 28 V battery-supplied converter was designed and constructed, using MOS-gated BIMOS switches to achieve high power, high frequency operation.

1. INTRODUCTION

In the era of modern power electronics, it is essential that bulky dissipative methods of power processing need to be replaced by more efficient and space saving techniques. Switched-mode dc/dc converters provide a highly efficient means of transforming power from one voltage level to another, with the most basic of the many circuit configurations which can produce this conversion at an adjustable voltage ratio, being the buck, boost and buck/boost configurations shown in Fig.1. Other arrangements, such as the flyback and forward converters, are derived from these [1].

To date, dc/dc converters have been widely used in switched-mode power supplies, with low output voltage and power levels and single-quadrant operation. High power (greater than 1 kW) single quadrant boost converters are however now being used in satellite power systems and similar applications. Although a 4-quadrant H-bridge chopper may be used for multi-quadrant operation, this provides only step-down conversion while suffering from low efficiency and harmonic tolerance.

The paper describes a 4-quadrant buck/boost switched-mode converter with a single battery powered supply, which has many advantages over the existing forms of converter.

2. THE NEW CONVERTER

The output voltage $V_0$ of the conventional boost converter of Fig.1 may be adjusted by variation of the switching-duty cycle. Thus, if $V_1$ is the input voltage, the output voltage is

$$V_0 = \frac{V_1}{1 - D}$$

where the duty cycle

$$D = \frac{t_{on}}{T}$$

and switching period

$$T = t_{on} + t_{off}$$

If two 2-quadrant boost converters (Fig.2(a)) are paralleled symmetrically, as shown in Fig.2(b), a novel 4-quadrant converter capable of bi-directional voltage output is obtained. The main power switches $S_{W1}$ and $S_{W2}$ operate in a complementary mode. During time $T_1$ switch $S_{W1}$ is open, and the build-up of the current $I_1$ stores energy in the inductor $L_1$. During period $T_2=(T-T_1)$, $S_{W1}$ is open and $S_{W2}$ closed, and the energy stored previously in $L_1$ is released through the diode $D_1$ to charge the capacitor $C_1$ to a voltage $V_{C1}$. Similarly, the build-up of the current $I_2$ stores energy in the inductor $L_2$ which, at the commencement of the next duty cycle, is released through the diode $D_2$ to charge the capacitor $C_2$ to a voltage $V_{C2}$. If, now $D_1 = \frac{T_1}{T}$ and $D_2 = 1 - D_1 = \frac{T_2}{T}$, it follows that the capacitor voltages are given by

$$V_{C1} = \frac{V_1}{1 - D} \quad \text{and} \quad V_{C2} = \frac{V_1}{1 - D_1}$$

The voltage gain of the converter is

$$K = \frac{V_0}{V_1} = \frac{V_{C1} - V_{C2}}{V_1} = \frac{2D}{1 - D} \quad (1)$$

from which it can be deduced that variation of $D$ between 0 and 1 enables the output voltage to be either less than or greater than the input voltage and for the polarity of the output voltage to be reversed, as is clear from both Table 1 and the theoretical and experimental variations of voltage gain with duty cycle shown in Fig.3.

Four-quadrant operation of the new converter requires that the load current can be reversed, and this may be achieved by the introduction of the two extra switches $S_{W3}$ and $S_{W4}$ shown in Fig.2. When $V_{C2}$ is raised so that it exceeds $V_{C1}$, but the direction of the load current remains unchanged, more energy is returned to the sources via $S_{W3}$ than is removed via $S_{W4}$ and regeneration is obtained. Fig.4 shows typical
3. DESIGN CONSIDERATIONS

A prototype converter has been designed and constructed to provide an output of 6.6 A at 180 V from a 28 V supply.

Initially, a computer simulation [4] was undertaken on the circuit of Fig.2(b) to determine the optimum switching frequency, which minimises both the physical size of the inductors and the total power loss in the circuit. At a low frequency a large inductance is required and the inductor loss is high. On the other hand, the switching loss is low at low frequency but increases with the frequency. The results of the simulation, recorded in Fig.5, establish that the most suitable switching frequency is around 40 kHz.

The peak voltages and currents handled by the power switches are 43 A and 250 V, and many transistors capable of handling this power level at the switching rates of 40 kHz are now available. However, in order to obtain an output at 180 V considerations of equations (1) show that

\[ \frac{V_o}{V_i} = \frac{2D-1}{D(D-1)} = \frac{180}{28} \]

or

\[ D = 0.87 \]

So that \( T_1 = 21.75 \mu s \), \( T_2 = 3.25 \mu s \) and SW2 has only about 3\( \mu s \) to switch on and off in an ideal converter. In practice it is necessary to consider parasitic resistance in the circuit, in which case \( D \) may need to be increased to 0.95 to provide an output of 180 V, as shown in Fig.3(b), and SW2 must switch on and off within about 1.25 \( \mu s \). This speed is conveniently achieved using two power MOSFETs and one bipolar transistor connected to form the MOS-gated BIMOS switch shown in Fig.6. In this circuit, Q2 is a high-power (400 V 50 A) switching bipolar transistor, Q2 a high-voltage low-current MOSFET used to aid turn on of Q2 and Q3 a low-voltage high-current MOSFET used to turn off Q2 by opening its emitter lead. The advantages of this switch are that it can be turned on and off at MOSFET speeds, while its efficiency is high and its power handling capacity can be as great as that of a bipolar transistor. The drive circuit is also very simple, since only a conventional MOSFET drive is required.

To minimise skin effect and eddy current losses, the inductors \( L_1 \) and \( L_2 \) of Fig.2 were formed from copper strip wound on a ferrite core. The magnetic circuit was gapped to allow the inductance to remain at its required unsaturated value of 25 \( \mu H \), when peak current was flowing. Polypropylene capacitors were used to keep the equivalent series resistance to a minimum.

4. CONCLUSION

Both theoretical and experimental evidence has established that the novel dc/dc converter described in the paper may be employed when 4-quadrant operation is necessary. Bipolar transistors and MOSFETs have been used in an effective combination of power devices which enables high frequency, high power operation to be achieved. With the rapid advance taking place in semiconductor technology the limitations on the rating of the converter are continually being raised, and very powerful units may be envisaged in the relatively near future.

5. REFERENCES

Fig. 1. THREE BASIC DC/DC CONVERTER

a) BOOST CONVERTER

b) BUCK CONVERTER

c) BUCK-BOOST CONVERTER

Fig. 2a. 2-QUADRANT CONVERTER  Fig. 2b. 4-QUADRANT DC/DC CONVERTER
Fig. 3. Variation of voltage gain with duty cycle

Fig. 4. Circuit Waveforms (time scale 40μs/Div)

(a) Inductor current (20A/Div)
(b) Output voltage (50V/Div)
(c) Duty Cycle D (10V/Div)

Fig. 5. Optimal Frequency

Fig. 6. MOS-BIMOS Switch