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AN EXPERIMENTAL AND THEORETICAL
STUDY OF THE HOT-CARRIER ENERGY
DISTRIBUTION IN VLSI MOSFETs

by

TALAL S. AL-HARBI

A Doctoral Thesis Submitted in Partial Fulfilment of the Requirements for the
Award of a Doctor of Philosophy at Loughborough University of Technology

January 1996

© by Talal S. Al-Harbi
This thesis is dedicated to my parents,
my wife and children for their love,
support and understanding.
ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to my supervisors Professor Adel E. El-Hennawy and Dr. D. Visser for their guidance, inspiration and help throughout the course of this study. Thanks are also due to Professor R. P. Howson for his assistance and I would also like to thank Professor K.R. Ziebeck, director of research and head of the Department of Physics at Loughborough University of Technology for his encouragement and the interest he has shown in this work.

I am grateful to the Government of Saudi Arabia (King Abdulaziz University) for giving me this opportunity to continue my higher studies.

I would also like to thank Dr. Ali M. Al-Sanoosi head of the Department of Physics at King Abdulaziz University for all his help during my course.

My thanks are to the technical staff of K.A.A.U. for their help in writing the simulation software.

I would like to thank Thomson Microelectronics of Grenoble and Nottingham University for supplying us with MOSFETs and thin film samples.

Finally, I am grateful to all my colleagues and specially to Dr. Farag Al-Hazmi for his assistance throughout this work.
Abstract

MOSFET devices have, recently, been considered the basic building element in any electronic IC circuit or system. The great advances achieved by modern technologies has made it possible to scale-down considerably the MOSFET device (channel length L smaller than 0.5μm and oxide thickness smaller than 400 Å) which appreciably influences the device performance and its operating parameters.

This thesis presents novel theoretical and experimental contributions with respect to carrier heating phenomenon and their effects on device operation and reliability. It also develops new models for the simulation and predication of the behaviour and evolution of MOSFET characteristic parameters (the channel mobility μ, threshold voltage V_T, channel depth d_0, the noise level e_n, etc). In addition, the reliability is studied and formulated using the results of related measurements (percentage evolution or shift in the parameter values as a function of the stressing time t_{st} and the means of stressing: x-ray, or UV-radiation).

These models and formulations take into account the effects of scaling-down, the biasing conditions, the technology of fabrication and the environmental conditions.

High-precision measurement techniques and automatic parameter acquisition procedures have been applied. A cancellation of the leakage and drift in the device itself, the printed circuit board and the measuring instruments, have been seen to be the most serious problem. New types of precaution measurements have been introduced to overcome this problem successfully.

The research presented in this thesis has recently become very important since it provides new tools for the early discovery of any degradation in device performance or spreading of its characteristics. This helps to monitor the device, circuit and system operation and keep them functioning safety. It also enables one to establish the optimal conditions of operation which guarantees the most efficient performance.
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<td>Critical field of carrier heating (~1.5V/μm for for electrons and 2V/μm for holes).</td>
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<td>$e_{CLM}$</td>
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<td>$E_x$</td>
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<td>$E_y$</td>
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<tr>
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<td>$E_{yo}$</td>
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<td>$f_H$</td>
<td>High threshold frequency of the hot carrier gate current noise.</td>
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<td>Low threshold frequency of the hot carrier gate current noise.</td>
</tr>
<tr>
<td>$f_t$</td>
<td>Noise power fluctuation frequency (Hz).</td>
</tr>
</tbody>
</table>
G  Generation rate (cm³·sec) or op.Amp open loop gain elsewhere.

$g_m$  Transconductance of MOSFET (A/V).

$g_{mR}$  Transconductance of the RG-MOSFET.

$g_{mT}$  Transconductance of the TG-MOSFET.

H  Magnetic field intensity (A.Turn).

$H(v)$  Volume power density dissipated in the channel (W/m³).

$h\nu$  Photon energy (eV).

$H_i$  Internal magnetic field intensity (A.Turn).

$h_0$  Oxide thickness (Å).

$I_r$  Radiation flux (W/cm²).

$I_B$  Hot carrier substrate current (μA).

$I_{DS}$  Drain current (mA).

$I_{GS}$  Hot electron gate current (pA).

$I_{GP}$  Hot hole gate current (pA).

$I_L$  Channel leakage-current (~pA).

$I_m$  Magnetic current (A) (used to generate the magnetic field $B_z$).

$I_e$  Irradiation intensities (W/cm²).

$I_x$  Channel current at position $x$ (mA).

$J_{sy}$  The electron current density in the Y-direction (mA/cm²).

$J_{sz}$  Electron photogenerated current in the Z-direction (mA/cm²).

$J_{py}$  The hole current density in the Y-direction (mA/m²).

$J_{pz}$  Hole photogenerated current in the Z-direction (mA/cm²).

$J_{zo}$  Total photogenerated current in the Z-direction at front surface $z = 0$ (mA/cm²).

$J_{zt}$  Total photogenerated current in the Z-direction at rear surface $z = 6$ (mA/cm²).

$k$  Boltzmann constant.

$k(\lambda)$  Light absorption coefficient (1/cm).

$L$  Channel length (µm).
Electron and hole diffusion lengths (μm).

$m$ Electron rest mass ($0.11 \times 10^{-31}$ kg).

$M$ Magnetization (A.Turn).

$m^*$ Effective mass (kg).

$m_g$ Magnetic quantum number.

$N$ Number of broken bonds.

$n$ Principal quantum number.

$n(e,T_e)$ Carrier density at any energy and temperature $T$ (1/cm$^3$).

$n(y)$ Electron density (1/cm$^3$).

$N_A$ Acceptor density (1/cm$^3$).

$N_a$ Number per unit volume of the antiparallel magnetic dipole (T).

$N_{A,D}$ Acceptor and Donor atoms density (1/cm$^3$).

$n_c$ Number of stressing cycles.

$N_c$ State density at the conduction band edge (1/cm$^3$).

$N_D$ Donor density (1/cm$^3$).

$n_i$ Electron and hole densities at thermal equilibrium (1/cm$^3$).

$n_{o,p}$ Electron and hole densities in absence of illumination (1/cm$^3$).

$N_p$ Number per cent volume of the parallel magnetic dipole (T).

$n_{ph}$ Photogenerated electron density (1/cm$^3$).

$n_{p0,p0}$ Electron and hole bulk density (1/cm$^3$).

$N_s$ Density of surface state (1/cm$^3$).

$N_v$ State density at the valence band edge (1/cm$^3$).

$P_{esc}$ Escape probability.

$P_{inj}$ Injection probability.

$P_{ph}$ Photogenerated hole density (1/cm$^3$).

$P_V$ Volume power density (W/m$^3$).

$q$ Electron charge ($1.6 \times 10^{-19}$ C).

$Q_{B}$ Surface immobile charge density in the depletion layer (C/cm$^2$).

$Q_{fs}$ Fast state charge density (1/cm$^3$).
$Q_G$ Gate-electrode charge (C/cm$^2$).

$Q_m$ Mobile electron-charge density inside the channel (C/cm$^2$).

$Q_{ox}$ Oxide charge density (C/m$^3$).

$Q_S$ Surface charge density (C/cm$^2$).

$Q_{SS}$ Interface charge density (C/cm$^3$).

$Q_{SSS}$ Slow state charge density (1/cm$^3$).

$R$ Channel resistance ($\Omega$).

$R_B$ Substrate resistant ($\Omega$).

$S$ Surface recombination velocity (cm/sec).

$S_{SL}$ Channel length fluctuation spectrum ($\mu$m$^2$).

$S_{ch}$ Channel mobile charge density (C/cm$^3$).

$S_{DS}$ Channel current spectral density (A$^2$/Hz).

$S_{g}$ Gate current noise spectrum (A$^2$/Hz).

$S_{N}$ Spectral density of carrier trapping (cm$^{-3}$)$^2$.

$S_{n(e,T_e)}$ Perturbations of $n(e,T_e)$ (1/cm$^3$).

$S_{ox}$ Oxide mobile charge density (C/cm$^3$).

$S_{V_x}$ Spectral density (V$^2$/Hz).

$t$ Sample thickness ($\mu$m).

$T$ Temperature (K).

$T(x,y)$ Substrate temperature at position $x,y$ (K).

$T_e$ Electron temperature (K).

$T_{ev}$ Evaporation temperature (K).

$t_i$ Irradiation time (mn).

$T_m$ Melting point (K).

$T_o$ Ambient temperature (300K).

$T_s$ Substrate temperature.

$t_n$ Stressing time (sec).

$u$ Ultra violet.

$v$ Electron drift velocity.
$V_{DS}$  
Drain to source voltage (V).

$V_{DSS}$  
Drain to source saturation voltage (V).

$V_{DS}$,$V_{GS}$  
Stressing voltages (V).

$V_{FB}$  
Flat band voltage (V).

$V_{FG}$  
Floating gate potential (V).

$V_s$  
Reduced gate voltage - (V).

$V_{GS}$  
Gate source voltage (V).

$V_H$  
Hall voltage (mV).

$V_{ox}$  
Oxide voltage (V).

$V_{SB}$  
Substrate bias voltage (V).

$V_T$  
Thermal voltage that carrier gain from the environmental medium (mV) (used to denote the threshold voltage elsewhere (V).

$V_{To}$  
Large-geometry MOSFET threshold (-0.5V).

$V_x$  
Channel potential at position x (V).

$w$  
Depletion layer depth (µm). (Sample width elsewhere).

$W_D$  
Depletion layer width (µm).

$x$  
Constant depending on the sample geometry.

$\chi$  
Transconductance reduction-factor.

$x_{1},x_2$  
Positions of Hall sample contacts (mm).

$\gamma$  
Trap separation from the Si-SiO$_2$ interface.

$Z$  
Channel width (µm).

$\ell_{ox}$  
Electron mean free path in oxide (~16Å).

$\varepsilon_{si}$  
Silicon dielectric constant (12).

$\ell_{e}$  
Electron mean free path in silicon (~40Å).

$\varepsilon_{ox}$  
Oxide dielectric constant (4).

$<\delta I_y>^2$  
Mean square fluctuation of the hot carrier gate current.

$<\delta N>^2$  
Mean square fluctuation of carrier trapping.

$\alpha,\beta$  
Constants relating the threshold voltage to the device geometry (cm$^{-1}$).

$\beta$  
Channel sides steepness.

$\gamma$  
Constant accounting for surface recombination.
\( \delta \)  
Duty cycle.

\( \delta \eta \)  
Incremental variation due to variations in oxide field.

\( \Delta \phi \)  
Reduction in \( \phi_a \) (eV).

\( \Delta I_d \)  
Incremental current along the channel (mA).

\( \Delta I_{DS} \)  
Channel current variation caused due to lorentz force (\( \mu A \)).

\( \delta I_{DS} \)  
Fluctuation in the channel current (A^2).

\( \delta I_{\text{gs}} \)  
Fluctuation in the gate current spectral density (A^2).

\( \Delta n, \Delta p \)  
Excess electron and hole densities (1/cm^2).

\( \Delta N_{ox} \)  
Oxide state (slow) density (1/cm^3).

\( \Delta N_{SS} \)  
Surface state (fast and slow) density (1/cm^3).

\( \Delta N_i \)  
Number of electrons trapped in the volume element.

\( \Delta R \)  
Incremental variation of the channel resistance (\( \Omega \)).

\( \Delta S \)  
Small surface element (cm^2).

\( \Delta V_b \)  
Back biase voltage (V).

\( \Delta V_{\text{FB}} \)  
Flat band voltage (V).

\( \delta V_g \)  
Fluctuation in the gate voltage (V^2).

\( \Delta V_T \)  
Threshold voltage shift (V).

\( \Delta V_x \)  
Voltage drop at position x across incremental length \( \Delta x \) along the channel (V).

\( \Delta x \)  
Relative displacement of the Hall contacts (mm).

\( \Delta y \)  
Height of the surface element (cm).

\( \Delta \ell \)  
Pinch-off region length (\( \mu m \)).

\( \eta \)  
Trap activation energy (eV).

\( \eta_b \)  
Efficiency at which the bonds receive and absorb the photon energy.

\( \theta_A, \theta_p \)  
Electron and hole Hall angles (\( \theta_{A,p} = \mu_{A,p} B_2 \)).

\( \theta_G \)  
Constant accounting for the gate-electrode effect (1/V).

\( \epsilon_{\text{fi}} \)  
Intrinsic Fermi level (eV).

\( \epsilon_{\text{fp}} \)  
Quasi Fermi level (eV).
\( \varepsilon_g \)  
Energy gap (eV).

\( \varepsilon_m \)  
Mean energy of hot carriers (eV).

\( \varepsilon_0 \)  
Free space permitivity \((8.85 \times 10^{-12} \text{F/m})\).

\( \lambda \)  
Wavelength (nm).

\( \lambda_0 \)  
Displacement of the peak of the Si/SiO\(_2\) potential caused by the oxide field and the image force \((\sim 10 \text{ Å})\).

\( \mu \)  
Mobility \((\text{cm}^2/\text{V.sec})\).

\( \mu_a \)  
Angular momentum.

\( \mu_b \)  
Bulk mobility \((\text{cm}^2/\text{V.sec})\).

\( \mu_{\text{eff}} \)  
Effective channel mobility \((\text{cm}^2/\text{V.sec})\).

\( \mu_m \)  
Quantum magnetic dipole moment.

\( \mu_{\text{ma}} \)  
Antiparallel magnetic dipole moment.

\( \mu_{\text{mp}} \)  
Parallel magnetic dipole moment.

\( \mu_n, \mu_p \)  
Electron and hole mobilities \((\text{cm}^2/\text{V.sec})\).

\( \mu_o \)  
Free space permeability \((\text{wb/cm}^2 \cdot \text{A.Tum})\).

\( \mu_{\text{ox}} \)  
Oxide mobility \((\text{cm}^2/\text{V.sec})\).

\( \mu_{\text{oxn}} \)  
Electron oxide mobility \((\sim 40 \text{ cm}^2/\text{V.sec})\).

\( \mu_{\text{oxp}} \)  
Hole oxide mobility \((\sim 3.9 \text{ cm}^2/\text{V.sec})\).

\( \mu_r \)  
Relative permeability \((\text{wb/cm}^2 \cdot \text{A.Tum})\).

\( \mu_{\text{st}} \)  
Stressed channel mobility \((\text{cm}^2/\text{V.sec})\).

\( \xi \)  
Constant depending on the physical properties of silicon and the device geometries.

\( \rho \)  
Resistivity \((\Omega \cdot \text{cm})\) or volume charge density of electrons in MOSFET surface \((1/\text{cm}^3)\).

\( \rho_m \)  
Magnetoresistivity.

\( \rho_v \)  
Specific mass \((\text{kg/m}^3)\).

\( \rho_x \)  
Longitudinal sample resistivity \((\Omega)\).

\( \rho_y \)  
Transverse sample resistivity \((\Omega)\).

\( \sigma \)  
Capture cross-section \((\text{cm}^2)\).

\( \sigma_m \)  
magnoconductivity \((\Omega)\).
\( \sigma_{ph} \) Radiation capture cross-section (cm\(^2\)).

\( \sigma_c \) Capture cross-section (cm).

\( \sigma_x \) Longitudinal sample conductivity (\( \Omega \)).

\( \sigma_y \) Transverse sample conductivity (\( \Omega \)).

\( \tau \) Trap time constant (sec).

\( \tau_{an} \) Annealing time constant (hr).

\( \tau_{bo} \) Time constant for breaking of bonds (mn).

\( \tau_{co} \) Capture time constant of electrons by oxide defects (mn).

\( \tau_{cs} \) Capture time constant of electrons by surface defects (mn).

\( \tau_{fo} \) Formation time constant of defects at the oxide (-sec to hr).

\( \tau_{fs} \) Formation time constant of defects at the Si-SiO\(_2\) interface (-sec to hr).

\( \tau_{en} \tau_{ep} \) Electron and hole lifetimes lengths (\( \mu \)sec).

\( \tau_o \) Time constant for a trap at MoSFET surface (sec).

\( \tau_{ph} \) Annealing time constant.

\( \tau_i \) Traping time constant.

\( \phi_B \) Silicon to oxide potential carrier (eV).

\( \phi_{Ba} \) Silicon to oxide potential for electrons (-3.2 eV).

\( \phi_{Bp} \) Silicon to oxide potential for holes (-3.6 eV).

\( \phi_{Mo} \) Metal to-SiO\(_2\) barrier height (eV).

\( \phi_{Mi} \) Metal work function (eV).

\( \phi_{MS} \) Metal to silicon work function difference.

\( \phi_{Np} \) Donor and Acceptor potential energy (eV).

\( \phi_S \) Surface potential (eV).

\( \phi_{so} \) Si/SiO\(_2\) potential difference (3.25 eV).

\( \omega \) Fluctuation frequency (rad/sec).
CHAPTER 1
GENERAL INTRODUCTION
Over the years the size of IC devices has decreased dramatically. In this way it has been possible, by means of hot carrier phenomena, to operate devices more efficiently in several new areas of applications and at lower bias voltages. Therefore, it has become necessary to study the effects of hot carrier heating in more detail. The search for faster electronic devices that are noise and leakage free has resulted in the realisation of a new type of gate form (trapezoidal) for the MOSFET (Metal Oxide Semi-conductor Field Effect Transistor) device. The reduction of the physical size of MOSFETs has led to the great advantage of being able to put large numbers of components onto a very small area and, as such, save energy and space. However, a major drawback which has been encountered in the scaling down process is the increase of noise generated.

This thesis concerns the study of the hot-carrier energy distribution and its dependence on electric and magnetic fields and also noise reduction in VLSI MOSFET devices.

Traditional rectangular-gate MOSFET devices have been described in the literature [1,2,3,4]. Although the rectangular MOSFET has been known for a long time and its behaviour studied in detail, there are still significant discrepancies between theoretical models and experimental measurements of the device parameters. These discrepancies seem to increase when scaling down the device dimensions (channel length and width) and when using higher biasing voltages. Knowledge of the carrier energy distribution helps to evaluate the hot carrier gate and substrate currents and to characterise all related parameters. A new hot energy distribution has been adapted in this thesis from which values of the hot carrier currents and related parameters can be correctly predicted.

The trapezoidal-gate MOSFET device is introduced for the first time with complete modeling and analysis in this thesis. This type of MOSFET gate allows applications that require low noise levels and reduced leakage current and which are to be realised using simple and cheap technology [5,6,7]. The operation characteristics
of the trapezoidal-gate MOSFET have been modelled and are compared with experimental characterisation.

In a similar way, inconsistencies concerning the channel depth determination, \( d_0 \), the pinch-off region \( \Delta l \), etc., have been removed by introducing new models based on channel and oxide activities, by which it was found possible to determine \( d_0 \) and \( \Delta l \), and to simulate and describe the related experimental data [8, 9].

Scaling down has resulted in increased device noise and tends to decrease reliability [8,10,11,12]. In the past, noise reduction has been attempted by large and complicated filter circuitries, which often have many limitations [13,14]. In this thesis a novel type of noise cancellation is proposed. This uses a topological methodology making use of the trapezoidal-gate form. This new technique helped to achieve a much improved noise performance

As scaling down MOSFET sizes has proceeded over the last two decades, great attention has been given to device reliability and performance. Accelerated stressing by high-voltage operation was the simplest tool to be used [12,15,16,17,18]. It has been noticed that the device parameters and the performance change relatively slowly; therefore, it requires a very long time to obtain a clear picture of the evolution of the device reliability (~300 hours). Device degradation is caused by hot carrier action which takes place at the Si-SiO\(_2\) interface. In order to speed up the stressing and to widen the interaction area to the SiO\(_2\) layer above the interface, X-ray irradiation (20keV) has been used to degrade the Si-SiO\(_2\) interface region. In this case, defect creation has been obtained in the SiO\(_2\) as well as in the Si-SiO\(_2\) interface. The strain caused by the X-rays during a certain stressing time (20 seconds) is equivalent to the effect of high voltage applied for a much longer time (~100 hours).

Degradation of the Si-SiO\(_2\) and the SiO\(_2\) areas of MOSFET devices causes a shift in their device parameters. The degradation of the interface Si-SiO\(_2\) can be monitored by the mobility \( \mu \) and the 1/f noise while the degradation of the SiO\(_2\) is
related to a shift of the threshold voltage shift $V_T$. Different types of broken bonds, as well as dangling bonds, which are related to different types of trap levels inside the band gap, are responsible for device parameter modification. The work of the thesis classify these traps into two types: fast and slow.

It is well known that for SiO$_2$ thin films traps can be removed by irradiation with UV light [19-21]. Occupied trap can be emptied via luminescence and radiation loss processes and be returned to the ground state. Therefore, UV radiation (254 nm) has been applied to the MOSFET device in order to try to reverse the high-voltage or X-ray induced damage. The UV light at 254 nm (10eV), through the photo-electron induction effect which takes place at the Al-SiO$_2$ and the Si-SiO$_2$ interfaces, allows the device to be re-generated by direct UV radiation. It has been realised from the experimental results that the MOSFET operational parameters can be controlled and optimised for different applications by subsequently giving them X-ray and UV treatment.

The degradation due to X-ray and high-voltage stressing is similar. The change in mobility behaviour due to the stressing has been explained qualitatively via a slow-state and a fast-state process. The UV behaviour has also been modeled via a two-state model. The results of the X-ray and UV irradiation are finally discussed within a physiochemical framework of the Si-SiO$_2$ network and interface.

The effect of magnetic fields on MOSFET devices and their parameters has not been well documented in the literature. Hall effect measurements on MOSFET devices indicate indirectly that the channel carriers deviate laterally by a normal magnetic field applied normally. The MOSFET channel and the thin film are both in effect sheets of mobile carriers accelerated by a longitudinal electric field and deviated up or down by a normally applied magnetic field. The effect of the Lorentz force has been studied in a specially designed RG MOSFET which has a split drain. It has been demonstrated that this device can be used as a very sensitive magneto detector of magnetic fields.

In the following sections a brief outline of the thesis is given.
Chapter 2 presents the necessary theoretical and technological background to the subject of the thesis. It presents the different types and structures of MOSFET VLSI. A brief summary is also given of the physics concerned with the X-ray and the UV stressing as well as a short discussion of the material properties of the Si-SiO₂ interface and the SiO₂ layer and the corresponding technologies of fabrication.

Chapter 3 presents the new modeling techniques used for MOSFET devices. It is divided into five main parts. In part 1, the accurate modeling of the channel and carrier heating phenomena are presented. In part 2, a description of the development of the new noise-reduction technique is presented. In part 3, the effects of stressing on the MOSFET are studied. Part 4 presents the theoretical investigation of the magnetic properties of the MOSFET devices. Finally, part 5 summarises the results of preceding theoretical approaches.

Chapters 4&5 show the experimental results and simulation results of the model simulation developed in Chapter 3. Experimental verification of most models are presented.

Finally, Chapter 6 presents a the general conclusions and the achievements of this research work. It also indicates short outline of future research.

Most of the research presented in this thesis has been published in specialized international periodicals and presented at international conferences. Also the practical applications have been submitted for patent.
CHAPTER 2

PHYSICS AND FUNDAMENTALS
OF MOSFETs
2.1 INTRODUCTION

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) structure has recently received much attention from both physicists and industrial scientists since it now represents a basic building block for many electronic circuits or systems. Precision detectors, huge computer memories, laser drivers, aerial and submarine navigation systems are only few examples of MOSFET VLSI applications.

From the research point of view, the MOSFET structure provides a simple and reliable tool to study and characterize the carrier heating phenomenon, the related effects on the hot carrier energy distribution and its dependence on the electric and magnetic fields.

The MOSFET is simply constructed of two $N^+$ doped regions (the source and drain) diffused into a p-type substrate. Between them a voltage controlled conducting channel exists. According to the biasing voltages and the MOSFET geometry, carrier heating takes place.

The mobile carriers in the MOSFET surface may be injected into the $SiO_2$ insulating layer when these carriers are given energies sufficient to enable them to jump over the $Si-SiO_2$ interface energy barrier. These carriers can propagate continuously through the $SiO_2$ layer towards the gate electrode, as long as the oxide field is high enough to overcome the trapping effects. Under these conditions, a hot carrier gate current may be obtained ($10^{-14}$ to $10^{-9}$ A) [22,23,24,25].

When the biasing voltages are increased and/or the device geometrical dimensions are decreased so that impact ionization and consequent carrier multiplication occurs in the MOSFET channel, secondary electrons and holes are generated. The electrons are attracted towards the drain where they contribute to the channel current. Some of these electrons are injected into the $SiO_2$ layer which may
enhance the hot carrier gate current. The secondary holes are accelerated towards the bulk where they are accumulated and give rise to the hot carrier substrate current [10,11,23]. When the device is switched into saturation, the surface normal field close to the drain reverses its direction and some of the secondary holes are accelerated to the Si-SiO₂ interface where they jump over the energy barrier, and penetrate into the oxide layer and constitute a hot hole gate current, which subtracts from the hot carrier gate current (given due to the injection of the hot electrons).

The hot-carrier injection represents a major drawback concerning the MOSFET reliability and parameter stability [11,12,23]. However, this phenomenon is now principally used as a means of programming and erasing the modern EEPROMs (Electrically Erasable Programmable Read Only Memories) [24].

Precise modelling and evaluation of these phenomena became very important during the last decade especially for the characterization and the prediction of performance of the VLSI; very large scale integration MOSFET devices and systems. Therefore it is necessary to have a proper understanding of the behaviour of the hot carrier and its energy distribution to enhance our knowledge about the device operation in the presence of hot carriers.

The principal objective of this chapter is to present an overview of all principles and consequences relating to the carrier heating phenomenon and to provide the background for the formulation of new or modified theories describing the hot carrier phenomenon. The production process of MOSFET devices and the structural and physical properties of the Si-SiO₂ interface and SiO₂ layer are also discussed.

2.2 BASIC STRUCTURE

A cross sectional view of an N-Channel MOSFET is shown in Fig.(2-1). The device consists of an n-type source and drain regions (~ 10¹⁸ /cm²) diffused into p-type silicon substrate (~ 10¹⁴ /cm²). A very thin layer of insulating SiO₂ (of thickness h₀ ranging from 400 Å to 1200 Å) is grown on the substrate surface between the source
A cross sectional view of an N-channel MOSFET.
and drain regions. This insulating layer is called the gate oxide. A metal layer (Al) is deposited over the gate oxide which is referred to as the gate. The energy band structure of MOSFET is shown in Fig.(2-2). In modern technology p or n polysilicon gates are used instead of aluminum [1].

When a positive voltage (smaller than the threshold voltage) is applied to the gate (with respect to the source) the positive holes are pushed away into the substrate. Each leaves behind a negative ion (ionized acceptor impurity atom) which creates a negative immobile charge at the surface of the silicon between the source and the drain. If the positive gate voltage is large enough (greater than the threshold value \( V_T \)), mobile electrons are introduced into the MOSFET surface and a conducting channel between the source and drain will be established. In other words the MOSFET surface is said to be inverted into n-type (or populated by electrons).

Under these conditions, electrical conduction will take place between the source and the drain when a potential difference is applied between them.

In the absence of surface inversion (when the gate voltage is smaller than \( V_T \)) no channel is established and no conduction takes place between the source and the drain.

The device is bilaterally symmetric, i.e. the source and drain regions can be electrically interchanged.

The inversion layer which forms the conducting bridge between the source and drain is the seat of electrical activities exhibited by the device. The thickness of this layer, which we call the channel depth, \( d_0 \), is varied from 10 to 200 Å [12,23,26].

Sometimes when the device biasing voltages (drain to source voltage \( V_{DS} \) and gate to source voltage \( V_{GS} \)) are extremely high and/or the MOSFET geometry (channel length \( L \), width \( W \) and oxide thickness \( h_o \)) are appreciably reduced, new
Fig. (2-2)

Energy band structure of MOSFET
phenomena related to the carrier heating take place to make the gate insulating layer the seat of new and important activities [27,28].

2.3 PRINCIPAL TYPES OF MOSFETs

There are two principal types of MOSFETs: the first is the enhancement mode MOSFET named E-MOSFET, which has been dealt with in section (2-2), where the drain current $I_{DS}$ remains zero as long as $V_{GS}$ is smaller than $V_T$. As Fig.(2-3) shows, $I_{DS}$ increases proportionally with $V_{GS}$ as $V_{GS}$ exceeds $V_T$. When $V_{GS}$ is very high, the channel electrons are accelerated towards the Si-SiO$_2$ interface during their longitudinal motion towards the drain. This degrades their mobility of propagation through the channel. $I_{DS}$, acquires a smaller rate of increase with $V_{GS}$ and ceases afterwards to increase further with $V_{GS}$ [23].

The second type is the depletion mode MOSFET which is termed D-MOSFET illustrated in Fig.(2-4), the energy band structure is shown in Fig.(2-5). It is normally conducting (a channel exists between the source and drain) even when the gate voltage $V_{GS}$ is zero. It can be turned off (see Fig.(2-3)) when $V_{GS}$ is made sufficiently negative ($|V_{GS}| > |V_T|$). That is because an implanted N$^+$ channel normally exists and when a sufficiently high and negative $V_{GS}$ is applied the channel is pinched-off and no drain current flows. The typical I-V characteristics of both E and D-MOSFETs are shown in Fig.(2-6).

The MOSFET current for a D-type MOSFET occurring by increasing $V_{GS}$ does not saturate due to the attraction of electrons by the gate electrode $V_{GS}$. In this case, it pushes the electrons far from the Si-SiO$_2$ interface (see Fig.(2-6-b)). However, the interaction between these electrons and the surface defects and states is strongly reduced, and the channel mobility is expected to be greater than that which we have observed with the E-MOSFET [1,12]. However, the mobility degradation in the D-MOSFETs may be observed when $V_{GS}$ is positive.
Fig (2-3)
Variation of the channel current $I_{DS}$ with the gate voltage $V_{GS}$.

Fig (2-4)
Depletion mode MOSFET (D-MOSFET)
**Fig (2-5)**
MOSFET energy band structure [22]

**Fig (2-6)**
Typical I-V Characteristics of the E and D MOSFET
2.4 MODERN TECHNOLOGIES OF FABRICATION

In this section, the most widely used technologies of MOSFET fabrication are presented.

2.4.1 H-MOSFET Technology

In this technology the steps of fabrication, using monolithic IC technique, are shown in Fig.(2-7). It starts with p-type epitaxial silicon wafer and comprises [1]:

- a) Thick oxide growth (step No.1)
- b) Opening of the source and drain windows (steps 2 up to 4).
- c) Drain and source diffusion. (step 5).
- d) Opening the gate window (steps 6 up to 9)
- e) Deposition of a thin oxide (400Å) layer; the gate oxide (step 10).
- f) Opening the drain and source contact windows (steps 11 up to 13).
- g) Evaporation of interconnections metal under high vacuum (step 14).
- h) Selective etching of the undesired metallization (steps 15,16).

The thick oxide is used to prevent any penetration out or into the silicon wafer, the selective masks are made of chromium glass photoplates and are used to allow certain areas of SiO$_2$ or aluminum to be illuminated by ultraviolet light which facilitates the removal of these areas by chemical etching and deionized-water washing.

2.4.2 Interconnections in IC Devices

The global interconnections in an IC device are used to supply power and ground connections to the transistors of the device, as well as to provide the pathways across which signals can be sent. The global interconnect communicates to the diffusion area and the polysilicon gate through contacts, while the connection between the global interconnects at adjacent levels in the device is made by vias, see Fig.(2-8). These contacts are vital to the operation of the device and, as such, partly determine the properties [29].
Fig. (2-7-a)

Steps of MOSFET fabrication, using monolithic IC technique
9) Etching the gate window

10) Gate oxide growth

11) Masking no 3
12) UV Exposure

Fig. (2-7-b)

Steps of MOSFET fabrication, using monolithic IC technique.
13) Etching the drain and source windows

14) Metal evaporation

15) Selective etching
16) Metal connections

Fig (2-7-c)
Steps of MOSFET fabrication, using monolithic IC technique
Fig. (2-8)
Schematic cross section of a double-metal COMS circuit showing the key components of a multilevel metal circuit [29]
On a microscopic level many problems are encountered which are directly related to the materials involved and the thin film nature of the device, such as mechanical stress at the boundary (lattice mismatch), solubility of the elements, or composites at the interface, etc.

For process simplicity one would like to use one single material for the connections. Aluminium fullfills most of the requirements which are set for the interconnects [29]. In order to improve reliability of the metallization, layering with Ti, TiN or TiW is used. This is because pure Al contacted on n and p-Si is not stable at temperatures between 350-500°C and the device will be subject to these temperatures in the post-contact steps of the fabrication. Si is soluble in Al at high temperatures. It also diffuses rapidly into polycrystalline Al films. The dissolution of Si in the contact is localized due to the presence of an Al₂O₃ layer at the interface. Where the interface is weak the Si can still diffuse in and form spikes, which can short out shallow junctions. These problems can be prevented by adding 1% Si to Al as a gate material. Al - 1% Si is used for MOS circuits below 5 μm. At high temperatures, Si and Al go into solution but on cooling, Si is precipitated out as an epitaxial layer at the interface. This can lead to a high contact resistance and be a real concern for devices <1 μm.

The presence of a small oxide layer, < 10 Å, at the contact interface can prevent the formation of an epitaxial layer on the Si substrate. The contact resistance variation can also be prevented by interposing a metallic layer between Al and Si, such as MoSi₂, TaSi₂, Ti, TiN, TiW. In the case where Si precipitates out as particles in this underlying metal, the current is shunted into the contact around these precipitates. The properties of the Al interconnects are strongly dependent on the microstructure of the Al film. The growth process is given in Fig.(2-9). Depending - on the presence/absence of an intermetallic layer on the Si, the growth process results in wetting the surface (Si-Al) or the formation of conglomerates (TiN, TiW) (see Fig. (2-10)). For a good current conducting contact, the Al islands have to grow together to make the interconnections, finally resulting in an Al-film which consists of many holes. The process is not necessarily carried through till a continuous film is formed. The devices used in this thesis are covered with an non-continuous Al-film. The islands need to have a thickness between 1-3 μm in order to make a good electrical contact.
Stages of formation of Al films during deposition. (a) Formation of nuclei. The size and spacing depend on the underlayer and deposition temperature. (b) Island formation from the growth and coalescence of neighboring nuclei. Secondary nuclei are also formed between the islands. (c) Coalescence of islands to form a semicontinuous film with interpersed voids. (d) Formation of continuous film consisting of small grains. (e) Grain growth [29]
Islands formed during the formation of Al films on two different substrates: (a) on single-crystal Si and (b) on TiW deposited in the same pump down as Al. On Si the Al film wets the surface and tends to agglomerate. The average thickness at which the film becomes continuous is lower on Si than it is on TiW [29].
This fact will allow UV irradiation to penetrate the $\text{SiO}_2$ layer and reach $\text{SiO}_2/\text{Si}$ interface. As such, the active parts of the device can be stressed by UV light.

2.4.3 SOI Technology

Many silicon-on insulator (SOI) devices have been proposed, including silicon-on-sapphire (SOS), silicon-on-spinel, silicon-on-nitride, and silicon-on-oxide. Fig. (2-11) shows a schematic diagram of an SOI device, where single-crystal silicon is epitaxially grown on an insulator substrate (e.g., $\text{Al}_2\text{O}_3$ in the case of SOS) [30]. The devices are made using the standard MOS process (Sec.2.4.1). The substrate provides the isolation between devices. Because of the reduced parasitic capacitances, the device has a faster response. The value of the threshold voltage $V_T$ depends strongly on the substrate doping; higher doping results in a larger $V_T$ value.

Laser annealing techniques [31] have recently been applied to amorphous silicon films deposited on insulator substrate, such as $\text{Si}_3\text{N}_4$ and $\text{SiO}_2$ to facilitate their structural performance. At present the devices show inferior performances which are not better than those of the devices made on bulk single crystal substrates, owing to the high defect density in the Si film and the high interface trap density at the Si-insulator interface. With improvements in film quality, SOI devices will have the potential for ultra-high speed operation and three-dimensional device configurations, (since the basic SOI layers can be staked one over other to form a multiple-layer integrated circuit) [32].

2.4.4 V-MOSFET Technology

Fig. (2-12) shows the V-MOSFET (V-shaped groove MOSFET) structure [33]. It also shows a modified version, the U-MOSFET (U-shaped groove MOSFET) structure [34]. These structures are made on <100>-oriented silicon substrates (see section (2.5)), using a nonisotropic etching to form the notch sloping from the horizontal at 54.7 Å. The doping distribution shown is equivalent to a D-MOSFET structure. The channel length is $2L$ since the two channels are parallel, one on each side of the etched groove. The device has a common drain contact at the bottom. Because many devices can be connected in parallel these structures can handle high
Fig (2-11)
Schematic diagram of an SIO device [1].

Fig (2-12-a)
V-MOS Structure [1].

Fig (2-12-b)
U-MOS Structure [1].
current and high power [33]. In this technology very short channel lengths (≤ 0.1 μm) can be realized.

2.4.5 HEXFET

Fig.(2-13) shows the HEXFET (hexagonal MOSFET) structure. The operation of the HEXFET is similar to the D-MOSFET (see section 2.3). Each cell has an N⁺ source region and a hexagonal polysilicon gate. The current flows from the source through the inverted narrow channel around the periphery of the cell and then vertically downward to the bottom drain N⁺ contact. The HEXFET offers very high packing density (e.g., ~ 10⁵ hexagonal cells per cm²). Because of the large aspect ratio, 6NZ/L where N (see Fig.(2-13-b)) is the total number of cells per device and Z is the length of the hexagonal side, the on-resistance can be made very low [35].

2.5 EFFECT OF SURFACE ORIENTATION ON MOSFET PERFORMANCE

The silicon bulk is the body of the silicon which is very far from the surface, i.e. where the silicon surface has no influence on the bulk properties (mobility $\mu$, resistivity $\rho$, etc.). The bulk refers to the single crystal substrate.

The silicon crystalline structure is characterized by a periodic repetition in the three directions x, y and z of the silicon atoms. It could be thought of as a simple cubic crystal [1,2,36].

In MOS technology it is necessary to specify the various planes of the silicon crystal, and to evaluate the surface density of defects (probable number of broken bonds) in each plane and thereafter select the plane having the minimum defect density. Miller indices are employed for this purpose. Referring to Fig.(2-14), these indices are specified as follows [1,22,23,36]:

1) Determine the intercepts $a$, $b$ and $c$ of the plane with the three axes x, y and z respectively.
2) Form the reciprocals of these intercepts, $\frac{1}{a}$, $\frac{1}{b}$ and $\frac{1}{c}$. 

12
Fig. (2-13-a,b)
HEXFET (hexagonal MOSFET) Structure [1]
Fig (2-14)
Miller Indices

\[ a = 1, b = 1, c = \infty \]

\[ \{110\} \]

\[ 4/\sqrt{2}a^2 \]

\[ a = b = c = 1 \]

\[ \{111\} \]

\[ 6/\sqrt{2}a^2 \]

\[ a = 1, b = \infty, c = \infty \]

\[ \{100\} \]

\[ 4/a^2 \]
3) Express the reciprocal terms with the smallest set of integers that can be obtained by multiplying each of the fraction by the same number, for example $\frac{a}{a}$, $\frac{a}{b}$, and $\frac{a}{c}$.

4) We can therefore distinguish three principal planes $<111>$, $<110>$ and $<100>$ respectively for $a=b=c$, $a=b$ and $c=\infty$ and $b=\infty=c$.

5) Straight forward calculations showed that the plane $<100>$ is the best since it corresponds to the minimum number of broken bonds and it therefore has the minimum defect density $N_s = \frac{3}{a^2}$.

2.6 THRESHOLD VOLTAGE INSTABILITY AND SHIFT

We have seen that MOSFET can be turned on by applying a gate voltage $V_{gs}$ of proper polarity (positive in the case of n-channel and negative in the case of p-channel) between the metal gate and the silicon substrate. As Fig.(2-15-a) shows, when applying a positive voltage $V_{gs}$ on the MOSFET gate a normal electric field is built-up in the substrate surface which bends the energy bands downwards. When the value of $V_{gs}$ is greater than a certain threshold value termed $V_T$, the intrinsic Fermi level, $e_{Fi}$, crosses the quasi fermi level, $e_{Fp}$, and the surface region converts from p-type to n-type (surface inversion occurs). The n-channel inversion layer electrically connects the n+ source and drain regions to each other as shown in Fig.(2-15-b). This inversion layer is considered to be present effectively when the silicon surface becomes as heavily n-type as the bulk is p-type.

Mathematical investigation of this condition (referring to Fig.(2-15)) can be stated as [1]:

$$\phi_s = 2\phi_N \quad (2-1)$$

where $\phi_s$ is the surface potential which is defined as:

$$\phi_s = \frac{(e_{Fi \text{ bulk}} - e_{Fi \text{ surf}})}{q} \quad (2-2)$$

and $\phi_N$ is the Fermi Potential given by

$$\phi_N = \frac{(e_{Fi \text{ bulk}} - e_{Fp})}{q} \quad (2-3)$$

where $q$ is the charge of the electron.
Fig (2-15-a)
Surface Inversion in MOSFET [22]

Fig (2-15-b)
Creation of MOSFET Channel [22]
As SiO$_2$ is a good insulator, no current will flow in the y direction. It thus follows that $e_{Fp}$ remains constant in the y direction. When $V_{GS}$ is reduced (less positive) and the energy band edges go up such that $e_{Fi}$ and $e_{Fp}$ coincide at the Si-SiO$_2$ interface, the substrate surface becomes intrinsic, i.e. contains free electrons and free holes with equal numbers (see fig(2-16)).

When $V_{GS}$ is further reduced, such that $e_{Fi}$ goes far above $e_{Fp}$, the surface electrons can not be accommodated further in the channel well and holes are not yet collected. In this case the substrate surface is said to be depleted.

When $V_{GS}$ becomes negative the energy bands are bent in the opposite direction and the normal surface field reverses its polarity, attracting the free holes to the Si-SiO$_2$ interface. Hence accumulation of free holes occurs at the substrate surface.

In any one of the above three cases, the applied gate voltage $V_{GS}$ is distributed between the gate oxide and the silicon surface region as follows:

$$V_{GS} = V_{ox} + \phi_s$$

(2-4)

with

- $V_{ox}$ the voltage across the gate oxide.
- $\phi_s$ the voltage across the silicon surface region [1,12].

The continuity of electric displacement vector $D$ across the Si-SiO$_2$ interface requires that [1,2]:

$$\varepsilon_{ox} E_{ox} = \varepsilon_{st} E_{st}$$

(2-5)

The electric field directed into the silicon surface at the interface is given by Gauss's theory as:

$$E_{st} = -\frac{Q_s}{\varepsilon_{st} \varepsilon_0}$$

(2-6)
**Fig (2-16-c)**
Hole accumulation in MOSFET ($V_{gs}=-ve$).

**Fig (2-16-b)**
Depletion in MOSFET ($V_{gs}<V_T$).

**Fig (2-16-a)**
Inversion in MOSFET ($V_{gs}=V_T$).
with $Q_s$ being the density of charge per unit surface area, introduced by the band-bending. The electric field is constant in the gate oxide and given in terms of the oxide voltage $V_{ox}$ and oxide thickness $h_o$ by:

$$E_{ox} = \frac{V_{ox}}{h_o} \tag{2-7}$$

Thus combining Eqs. (2-5),(2-6) and (2-7) yields:

$$V_{ox} = h_o E_{ox} = h_o E_{st} \frac{\varepsilon_{st}}{\varepsilon_{ox}} = \frac{-h_o Q_s}{\varepsilon_o \varepsilon_{ox}}$$

Since the oxide layer capacitance $C_{ox}$ is given by:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{h_o} \text{ F/cm}^2 \tag{2-8}$$

Thus Eqs. (2-8) and (2-4) develop to:

$$V_{ox} = \frac{Q_s}{C_{ax}} \tag{2-9}$$

$$V_{GS} = \frac{Q_s}{C_{ax}} + \phi_s \tag{2-10}$$

but

$$Q_s = Q_B + Q_n \tag{2-11}$$

where $Q_B$ is the surface immobile charge density in the depletion layer and $Q_n$ is the mobile electron-charge density inside the channel.
The surface potential $\phi_s$ creates a surface depletion layer with depth $w$ which is given by [1,2,26]

$$w = \sqrt{\frac{2\varepsilon_{si} \varepsilon_0 |\phi_s|}{qN_A}}$$ 

(2-12)

$w$ attains its maximum value when $|\phi_s| \geq 2|\phi_p|$, since all further charge induced by the applied gate voltage assists the surface inversion layer with no addition to the depletion layer:

$$w_{\text{max}} = \sqrt{\frac{4\varepsilon_{si} \varepsilon_0 \phi_p}{qN_A}}$$ 

(2-13)

At the onset of inversion we have:

$$\phi_s = 2\phi_p$$

$$Q_B = qN_A w_{\text{max}} = \sqrt{4\varepsilon_{si} \varepsilon_0 qN_A \phi_p}$$ 

(2-14)

Referring to Eq. (2-10), the gate voltage attains, in this case, its threshold value $V_T$ which is given by:

$$V_T = -\frac{Q_B}{C_{ox}} + 2\phi_p$$

$$= -\frac{\sqrt{4\varepsilon_{si} \varepsilon_0 qN_A \phi_p}}{C_{ox}} + 2\phi_p$$ 

(2-15)

Further increase of the gate voltage $V_{GS}$ over its threshold value $V_T$ results in the creation of mobile electrons and an enhancement of the inversion layer charge density $Q_s$. In this case
\[ V_{GS} = -\frac{Q_B}{C_{ox}} - \frac{Q_n}{C_{ox}} + 2\phi_p \] (2-16)

If the interface charge \( Q_{SS} \) is considered, Eq. (2-15) develops to:

\[ V_T = -\frac{1}{C_{ox}} \left( Q_{SS} + \sqrt{4\varepsilon_s \varepsilon_0 \eta N_A \phi_p} \right) + 2\phi_p \] (2-17)

2.6.1 Dependence of \( V_T \) On The Surface Orientation

According to Eq. (2-17) we conclude that \( V_T \) is very sensitive to the interface charge density \( Q_{SS} \) [12], and the surface charge density \( Q_{SS} \) depends on the crystalline orientation (see table (2-1)) [1,36]. It is positive for both n and p type of the thermally oxidized silicon. \( Q_{SS} \) increases as the number of broken bonds is increased. Referring to section (2.5), it was seen that \( Q_{SS}(111) > Q_{SS}(110) > Q_{SS}(100) \). It depends also on the process quality.

Because of the presence of the positive \( Q_{SS} \) at the Si–SiO\(_2\) interface (see Fig.(2-17)), it is necessary to employ a positive gate voltage to bring about the flat band condition. This voltage is sometimes termed \( \Delta V_{FB} \) and is given by:

\[ \Delta V_{FB} = \frac{Q_{SS}}{C_{ox}} \] (2-18)

2.6.2 Back Bias Effect

Equation (2-17) shows that \( V_T \) varies proportionally with the surface immobile charge density \( Q_B \) which is given by Eq.(2-14) [1,2], from which it is clear that \( V_T \) is sensitive to variation of \( w \) which varies in turn with the back bias voltage \( V_{SB} \) (appearing on the substrate) and cause \( w \) to obey the following formulation,
Fig (2-17)
Flat Band Voltage $V_{FB}$

<table>
<thead>
<tr>
<th>Crystal orientation</th>
<th>$Q_{SS}$ (C/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(111)</td>
<td>$8 \times 10^{-8}$</td>
</tr>
<tr>
<td>(110)</td>
<td>$3.2 \times 10^{-8}$</td>
</tr>
<tr>
<td>(100)</td>
<td>$1.4 \times 10^{-8}$</td>
</tr>
</tbody>
</table>

Table (2-1): Values of the surface state density $Q_{SS}$ as function of the crystal face orientation
\[ W = \sqrt{\frac{2 \varepsilon_E \epsilon_0 (V_{sb} + 2 \phi_p)}{qN_A}} \] (2-19)

From this it is clear that \( W \) and consequently \( Q_B \) increase as the substrate back bias \( V_{sb} \) increases. Referring to Eq. (2-17), we declare that \( V_T \) increases as \( V_{sb} \) increases and vice versa.

2.6.3 Dependence of \( V_T \) on the Device Scaling-Down

The reduction of the MOSFET geometry affects the threshold \( V_T \) voltage as explained below [3,4].

a) Short channel effect

As shown in Fig.(2-18-a,b), the gate electrode normally controls a surface charge \( Q_{BC} \) (defined by the shaded area), while the source junction controls the charge \( Q_{BS} \) existing within the source to substrate depletion region. The drain controls the charge \( Q_{BD} \) existing within the drain to substrate depletion region. Since the width of this depletion layer increases as the drain voltage \( V_{DS} \) increases, then \( Q_{BD} \) is expected to increase as \( V_{DS} \) increases. Indeed the source junction controls, besides \( Q_{BS} \), additional charge \( \Delta Q_{BS} \) which is defined by the cross shaded area. Also the drain controls, besides \( Q_{BD} \), additional charge \( \Delta Q_{BD} \) (cross shaded area). \( \Delta Q_{BS} \) and \( \Delta Q_{BD} \) have to be subtracted from \( Q_{BC} \). In long channel MOSFETs, \( \Delta Q_{BS} \) and \( \Delta Q_{BD} \) represent a negligibly small fraction of \( Q_{BC} \). Then referring to Eq. (2-17), it is clear that the value of \( V_T \) remains almost unaffected by the subtraction of \( \Delta Q_{BS} \) and \( \Delta Q_{BD} \) [1,37].

In short channel MOSFETs where \( L \) becomes smaller than 2 \( \mu m \) (see Fig.(2-18-b)), \( \Delta Q_{BS} \) and \( \Delta Q_{BD} \) no longer become negligibly small with respect to \( Q_{BC} \). Therefore subtraction of \( \Delta Q_{BS} \) and \( \Delta Q_{BD} \) from \( Q_{BC} \) causes it to be appreciably decreased, which appreciably reduces the value \( V_T \) below its large geometry value \( V_{to} \). In this case \( V_T \) can be formulated as [1,37,38,39]
Fig (2-18)
Short Channel Effect.
When $\alpha$ is a constant depending on the technology of fabrication. Measurements performed on HMOS I and HMOS II generations showed that $\alpha \equiv 0.2$.

b) Narrow Channel Effect

As shown from Fig.(2-19-a,b), the gate electrode controls the lateral charges $\Delta Q_{BC}$ (defined by the cross shaded zones) in addition to the surface charge $Q_{BC}$ existing in the channel to substrate depletion region as defined by the shaded area. In large MOSFETs $\Delta Q_{BC}$ is negligibly small compared to $Q_{BC}$. It does not, therefore, affect the value of $V_T$. On the other hand when the channel width $Z$ is decreased below 3 $\mu$m (see Fig.(2-19-b)) $\Delta Q_{BC}$ becomes comparable to $Q_{BC}$ and shows an important increase in the value of $V_T$. In this case $V_T$ is formulated, in terms of $V_{T0}$ (the large MOSFET value) as [37,40]

$$V_T(Z) = V_{T0} + \frac{\beta}{Z} \tag{2-21}$$

where $\beta$ is a constant depending on the technology of fabrication. Measurements performed on HMOS I and HMOS II generations showed that $\beta \equiv 0.3$.

Combining Eqs. (2-20) and (2-21), the global effect of scaling down on $V_T$ can be evaluated by:

$$V_T(L,Z) = V_{T0} - \frac{\alpha}{L} + \frac{\beta}{Z} \tag{2-22}$$
Fig (2-19)
Narrow Channel Effect
2.6.4 Injection Of Hot-Carriers Into The Oxide

When the carrier heating phenomenon becomes appreciable due to scaling down of the device geometry \((L,Z,h_0)\) and/or elevating the MOSFET biasing voltages \((V_{GS}, V_{DS})\) hot carriers are generated in important numbers and injected into the oxide layer. When the gate voltage \(V_{GS}\) is not sufficiently high to overcome the oxide trapping and/or the oxide quality is poor \([12,16,23,41]\), an important fraction of the injected carriers will be trapped inside the oxide and cause it to have a charge \(Q_{ox}\), which will be negative or positive according to whether the channel is n or p respectively. It tends to shift the value of \(V_T\) in the positive direction or the negative direction according to its polarity: and Eq. (2-17) develops to

\[
V_T = \phi_s + \frac{Q^*_S + Q_{SS}^* + Q_{ox}^*}{C_{ox}}
\]  

(2-23)

From this we see that \(V_T\) is very sensitive to \(Q_{ox}\) owing to the very small value of \(C_{ox} \) \(\left(10^{-4}\, \text{pF/\mu m}^2\right)\). A detailed study and analysis of the hot carrier injection into the MOSFET oxide is presented in Chapter 3.

2.6.5 Injection Of Hot Carriers Into The Substrate

In scaled-down MOSFETs, where the drain to source separation is reduced, the surface fields are increased and carrier heating takes place [1]. The energetic electrons (case of n-Channel MOSFET) cause impact ionizations and lead, therefore, to surface carrier multiplication [10,11]. The generated electrons are accelerated by the longitudinal-field component \(E_x\) towards the drain and contribute to the MOSFET drain current \(I_{DS}\). The generated holes are accelerated by the transversal field component \(E_y\) towards the substrate where they are collected and constitute the substrate current \(I_B\).

The flow of the substrate current \(I_B\) through the substrate \(R_S\) causes an \(I_B R_S\) voltage drop \(\Delta V_B\) which we call the back-bias voltage. It elevates the bottom potential of the depletion layer to a value which is greater than that which is expected
to be maintained in the absence of the substrate current, which shifts up the value of $V_T$ and makes it unstable [42]. Equation (2-23) develops, therefore, to:

$$V_T = \phi_S + \frac{Q_S \sqrt{1 + \frac{\Delta V_B}{V_{SB} + 2\phi_p} + Q_S^+ + Q_{ox}^+}}{C_{ox}}$$

(2-24)

If $I_B$ is so large that the $I_B R_B$ product exceeds a certain critical limit (~0.6V), the source-substrate junction will be forward biased and inject more electrons into the depletion region which enhances the carrier multiplication. This latter process causes $I_B$ and $\Delta V_B$ to be, regeneratively, increased through a positive feedback loop and may lead to a source to substrate breakdown [10,11].

The back-bias voltage $\Delta V_B$ tends also to decrease the surface potential $\phi_S$ and increases the channel depth $d_o$ by modifying the surface carrier distribution [24,26].

2.6.6 Effect Of The Gate Material On The Threshold Voltage

The threshold voltage is very sensitive to the gate material. This problem begins with the appearance of the n-Channel MOSFET generations [2,38], where metal gates are employed and where a channel is created even if the gate voltage is not yet applied (i.e. $V_T$ drops to zero or has a negative value). This is referred to as the work function difference $\phi_{ms}$ existing between the substrate silicon and the gate electrode. This difference bends the conduction band edge $e_c$ as shown in Fig.(2-20-a) in such a manner that electron accumulation occurs in the MOSFET surface. This means that surface inversion occurs and a channel is established which makes the device normally conducting even if the gate voltage is not yet applied (as in the case of the D-MOS explained in sec.(2.3)). This behaviour is not desired in the case of n-channel E-MOS (see sec.(2.3)). To treat this problem, polysilicon is used instead of the aluminum to fabricate the MOSFET gate. The potential of this solution can be explained as follows:
Fig (2-20)
Effect of the gate material on the threshold voltage.
When the work function between the semiconductor bulk and the gate field plate has a finite value then, as shown in Fig.(2-20 a,b,c) $\Phi_\text{M}=\Phi_\text{MO}$ is the metal to $\text{SiO}_2$ barrier height which is equal to the difference between the conduction band edge of $\text{SiO}_2$ and the Fermi level of the metal gate region. For the Al-$\text{SiO}_2$ system, $\Phi_\text{MO}=3.2$ eV, and for the Si-$\text{SiO}_2$ system the potential energy difference between the conduction band edge of $\text{SiO}_2$ and the conduction band edge of silicon $\Phi_\text{SO}=3.25$ eV. $\Phi_\text{S}$ is the potential energy difference between the conduction band edge of $\text{SiO}_2$ and the Fermi level in silicon. Thus, referring to Fig.(2-20-a), where the Si-P/Al $\text{SiO}_2$ System is illustrated

$$\Phi_{MS} = \Phi_M - \Phi_S$$

$$= 3.2 - \left[ \Phi_{SO} + \frac{\varepsilon_F}{2} + \Phi_P \right]$$

$$= 3.2 - [3.25 + 0.55 + 0.29]$$

$$= 3.2 - 4.09 \approx -0.9 \text{ eV} \quad (2-25)$$

In order to retain the flat band condition (removing the surface accumulation of electrons), a negative gate voltage (-0.9V) should be applied. Otherwise the value of the threshold voltage ($\text{V}_{\text{To}}$) will be negative,

$$\text{V}_T = \text{V}_{\text{To}} + \Phi_{MS}$$

$$= \text{V}_{\text{To}} - 0.9 \quad (2-26-a)$$

Since $\text{V}_{\text{To}}$ is small (-0.5V) then $\text{V}_T$ may drop to zero or negative values. The second example illustrated in Fig.(2-20-b) concerns the threshold voltage of the p-Si/ $\text{SiO}_2$/n-Si system where

$$\Phi_{MS} = \Phi_M - \Phi_S$$

$$= \left[ \Phi_{SO} + \left( \frac{\varepsilon_F}{2} + \Phi_N \right) \right] - \left[ \Phi_{SO} + \left( \frac{\varepsilon_F}{2} - \Phi_P \right) \right]$$

$$= -\Phi_N + \Phi_P = -0.58 \text{ eV}$$

Similar treatment showed that the value of $\text{V}_T$ may be zero or negative which is opposite to what is desired to satisfy the proper operation of the device,
\[ V_T = V_{T_0} + \phi_{MS} \]
\[ = V_{T_0} - 0.58 \quad (2-26-b) \]

The third case concerning the p-Si/ SiO\textsubscript{2}/p-Si is shown in Fig.(2-20-c). Here we have

\[ \phi_{MS} = \phi_M - \phi_S \]
\[ = \left[ \phi_{s0} + \left( \frac{e \kappa}{2} + \phi_p' \right) \right] - \left[ \phi_{s0} + \left( \frac{e \kappa}{2} + \phi_p \right) \right] \]
\[ = \phi_p' - \phi_p = +0.2 \text{ eV} \]

which leads to a value of \( V_T \) which is always positive and greater than \( V_{T_0} \) and maintains, therefore, the proper operation of the n-type E-MOSFET,

\[ V_T = V_{T_0} + 0.2 \text{ eV} > V_{T_0} \quad (2-26-c) \]

From this analysis we see that the employment of the polysilicon to fabricate the gate electrode tends to increase or decrease the value of \( V_T \) according to the type and/or level of the polysilicon doping [2,38].

2.7 MOBILITY DEGRADATION MECHANISMS

This effect is strongly related to the effective mobility \( \mu_{\text{eff}} \) of the channel carriers (electrons in our case of n-Channel MOSFET) which represents a very important parameter affecting, noticeably, both device operation and performance. The value of \( \mu_{\text{eff}} \) is appreciably reduced below that of the \( \mu_o \); the mobility of carriers existing deep in the substrate [23,26,40]. This reduced value no longer remains constant all over the channel depth.

Several studies have been devoted to the different mechanisms of degradation which reduce \( \mu_{\text{eff}} \) and make its value smaller than that of \( \mu_o \) [26,40,43,44].
2.7.1 Interaction With The Si-SiO\textsubscript{2} Interface States

In this mechanism, the mobile electrons are deviated up, during their propagation from the source to the drain, towards the Si-SiO\textsubscript{2} interface by the dragging force exerted by the charges localized in the surface states. This process tends to reduce the mobility [26,45]. The resulting mobility degradation becomes more important the greater the density of the surface states $N_t$ and/or the smaller the electrons drift velocity [46]. In this case the channel mobility $\mu(N_t)$ is given in terms of the bulk one $\mu_B$ by [1,23]:

$$\frac{\mu(N_t)}{\mu_B} = \frac{N_B \ln \left[ 1 + \frac{B}{N_t^{2/3}} \right]}{\left[ 1 + \frac{B}{N_t^{2/3}} \right]}$$  \hspace{1cm} (2-27)

with

$B$ is constant given by:

$$B = 5 \times 10^6 \left( \frac{e}{e_0} \right) T^2$$

$N_B$ = bulk density of ionized atoms.

The capture cross section $\sigma(y)$ of a surface state decreases exponentially with the distance $y$ separating the mobile electron from it [1,49], then $\sigma$ can be formulated in terms of $\sigma(o)$, the capture cross section of the surface state for an electron existing at the Si-SiO\textsubscript{2} interface as:

$$\sigma(y) = \sigma(o) \exp(-ay)$$  \hspace{1cm} (2-28)
Combining Eqs. (2-27) and (2-28), the variation of mobility with \( N \) and \( y \) is given by:

\[
\frac{\mu(N, y)}{\mu_B} = \frac{\mu(N, 0)}{\mu_B} + \left[ 1 - \frac{\mu(N, 0)}{\mu_B} \right] \left[ 1 - \exp \left( -\frac{y}{y_0} \right) \right]
\]  

(2-29)

with \( y_0 \) being a degradation parameter (~ 28 Å).

### 2.7.2 Carrier-Carrier Collision Effect

The mobile electrons can be classified, as shown in Fig. (2-21), into two groups: cold electrons, existing at the low energy states of the lower conduction band \( e_{C1} \) with high mobility, and hot electrons, existing at the low energy states of the upper conduction band \( e_{C2} \) with low mobility [29,47,48]. This classification is valid for the semiconductor whose conduction (or valence) bands consist of more than one valley (or hum), each characterised by a certain energy.

The carrier-carrier collisions exercise exchange of carrier energy. This process tends to increase the number of hot electrons having smaller mobility and to decrease the number of cold electrons which have higher mobility. This also tends to decrease globally the value of the effective mobility. This mechanism of degradation is expected to increase with the mobile carrier density, \( n \). Since \( n \) decreases when going deeper into the substrate but becomes bigger (at a certain position \( y \)) by increasing \( V_{GS} \), then the degradation mechanism becomes more important when approaching the Si-SiO₂ interface and/or by increasing \( V_{GS} \). In this case the mobility is formulated in terms of the bulk mobility \( \mu_o \) by [42,49].
Fig (2-21)
Electron distribution in multivalley conduction band semiconductors.
\[ \frac{\mu(n,y)}{\mu_o} = \frac{1}{\sqrt{1 + \left( \frac{n(y)}{n_e} \right)^2}} \]  

(2-30)

with

\[ n_e = 10^{19}/\text{cm}^3 \]

2.7.3 Crystal Heating

As the device biasing \((V_{GS}, V_{DS})\) is increased, more power is dissipated in the channel which elevates its temperature \(T\) (even if carrier heating does not occur). Crystal heating may also be caused by elevating the ambient temperature. Thermal heating of the crystal results in mechanical vibrations (of atoms about their equilibrium positions) whose number and amplitude increase as \(V_{GS}\) and/or \(V_{DS}\) is increased. These vibrations correspond to acoustic and optic phonons. The collisions of electrons with these phonons absorb energy from electrons and tend, therefore, to decrease their mobility \(\mu(T)\) \([12,50,51]\). In this case \(\mu(T)\) is formulated by \([1]\):

\[ \frac{\mu(T,Y)}{\mu_o} = \left( \frac{T}{T_o} \right)^{-3/2} \]  

(2-31-a)

with \(T = \xi H(y)\)  

(2-31-b)

\(H(y)\) is the volume power density dissipated in the channel and \(\xi\) is constant depending on the physical properties of silicon and the device geometries \([1]\).

2.7.4 Carrier Heating

When the device biasing voltages \((V_{DS}, V_{GS})\) are increased and/or the geometrical dimensions \((L, Z, h_o)\) are decreased, carriers are heated up \([12,16,27,41]\). Hot carriers emit some of their energy into the crystal which heats it up and causes generation of acoustic and optic phonons (see sec.(2.7.3)). Collision of hot electrons with these phonons degrade their mobility. The amount of mobility degradation
increases as crystal heating increases [12,26]. In this case the mobility is given in terms of the longitudinal channel field $E_x$ and the critical field of heating $E_c$ ($\sim 1.3$ to $1.6$ V/\(\mu\)m) as:

$$\frac{\mu(E_x,y)}{\mu_o} = \frac{1}{\sqrt{1 + \left(\frac{E_x}{E_c}\right)^2}}$$  \hspace{1cm} (2-32-a)

with

$$E_x = \frac{J_x(y)}{\sigma} y$$ \hspace{1cm} (2-32-b)

From which it is clear that $E_x$ is position dependent.

2.7.5 Gate, Electrode Macroscopic Defects

The normal surface field $E_y$ induced by the gate electrode, deviates the electrons during their propagation from the source to the drain towards the Si-SiO$_2$ interface, where they collide with the fixed surface charges and the surface macroscopic defects (see Fig.(2-22)) [52-58]. The mobility degradation caused by this mechanism increases as $V_{gs}$ increases and/or $V_{ds}$ decreases, because the barrier height of a surface defect increases with $V_{gs}$ increases, while the time length during which a carrier is acted upon by the field of defect increases with decreasing $V_{ds}$. This effect becomes bigger when the geometrical dimensions of the device are reduced. In this case $\mu(E_y)$ is given by [23]:

$$\frac{\mu(E_y,y)}{\mu_o} = \frac{1}{\sqrt{1 + \left(\frac{E_y}{E_x}\right)^2}}$$ \hspace{1cm} (2-33-a)

with

$$E_y(y) = \frac{\partial \phi_s(y)}{\partial y}$$ \hspace{1cm} (2-33-b)
Surface macro defects and mobility degradation
For simplicity, it can be modified to:

\[
\frac{\mu(E_p y)}{\mu_o} = \frac{1}{1 + \theta_g \left[ V_{GS} - V_T - \frac{V_{DS}}{2} \right]}
\]

with \( \theta_g \) being a constant which is reciprocally proportional to the channel length [23,26].

2.7.6 Surface Recombination And Trapping Effects

The high energy hot carriers exercise random collisions with the Si-SiO$_2$ interface and create defects in it. These defects act either as recombination centres or traps. Both of them provoke the disappearance of electrons through recombination and/or trapping. This process tends to degrade the mobility [23,26].

In this case the mobility is formulated by:

\[
\frac{\mu(S,\tau)}{\mu_o} = \left[ 1 - \frac{S\tau_n}{S\tau_n + L_n} \right]
\]

(2-34)

with \( S \) as the surface recombination velocity, \( \tau_n \), \( L_n \) the electron lifetime and diffusion length, respectively.

2.8 CHANNEL DEPTH

As the MOSFET gate voltage exceeds the threshold value \( V_T \), the device surface is depleted from holes and begins to be populated by electrons. When the surface density of electrons becomes equal to that of the holes which were existing before surface depletion, the surface is said to be inverted from \( p \) to \( n \) and a thin inversion layer is created below the gate between the source and the drain which represents the conducting channel between them. The thickness of this layer \( d_o \), see Fig.(2-23) is called the channel depth and it is defined as the distance \( y \) at which free electron density \( n(y) \) decreases to 10% of its maximum value \( n_s \) which occurs at the
Channel depth criterion (old one).

Fig.(2-23)
Si-SiO₂ interface. This approach assumes that the electron mobility \( \mu \) is constant all over the surface region and substrate thickness which is not correct [23,26].

Referring to section (2.7) we can observe that \( \mu \) acquires its undegraded value \( \mu_0 \) deep in the substrate and begins to decrease owing to several mechanisms of degradation when approaching the Si-SiO₂ interface. This approach gives channel depth values of the order of 10 to 20 Å. However, as will be seen in chapter 5, experimental work based on hot carrier injection indicated that \( d_o \) should be greater than 100 Å and is dependent on the device geometry \((Z,L)\) and biasing conditions \((V_{GS}, V_{DS}, V_{SB})\) [12,23,26].

2.9 EFFECTS OF DEVICE GEOMETRY ON NOISE PERFORMANCE

2.9.1 Effects on Carrier Heating

From the above description it becomes clear that \( \mu_{eff} \) is sensitive to the device geometry and biasing conditions. In fact the scaling down process of MOSFET devices provides conditions for increased carrier heating under which the energetic carriers bombard the Si-SiO₂ interface and create defects on it. These defects, as explained before (see sec (2.7)), lead to greater surface recombination, trapping and consequently in a more steeply decreasing mobility with distance \( y \) from the interface. This behaviour strongly affects the channel depth \( d_o \) and all related MOSFET performance and parameters \((V_{DS}, \Delta l, V_x(X), E_x(X), I_s \text{ and } I_b)\), as will be shown in chapter 3.

2.9.2 Effects on Noise Performance

The thermal and \( 1/f \) noise are seen to be appreciably increased in the short channel MOSFETs in comparison to those observed in large geometry devices. This may be referred to several reasons:

Firstly, the high field operation of the short channel devices elevates both the carrier and the crystal temperatures. This results in a thermal noise corresponding to an effective temperature which is greater than that of the large geometry devices [25,40].
Secondly the MOSFET is a surface activity device in which the fluctuating occupancy of traps existing in the oxide in and/or at the Si-SiO₂ interface can modulate the device surface-conductivity and affect the surface activities playing part along all the channel length [23,25,40]. The density and distribution of the interface and oxide traps seem, therefore, strongly to affect the level and behaviour of the device 1/f noise [40,59]. However, in short channel devices these two latter parameters are not stable either with time or with the device operating conditions [40,60,61] since the random bombardment of the Si-SiO₂ interface by energetic hot carriers causes the Si-SiO₂ interface and the oxide trap densities to increase continually with time and to be sensitive to the device operating voltages [40]. These densities will not be uniform either along the channel length nor over the oxide layer thickness [40]. Although these variations are very small, appreciable related evolution of the thermal and 1/f noise have been noticed. The 1/f and thermal noise manifest themselves as fluctuations in the gate voltage $\delta V_g$, in the channel current $\delta I_{DS}$ and in the gate current $\delta I_g$. The corresponding spectral densities $S_{V_g}$, $S_{I_{DS}}$ and $S_{I_g}$ were analysed and formulated before [40,46,59,61,62].

Several complicated methods and sophisticated techniques have been proposed [63-65] to achieve such a reduction of these fluctuations. All proposed techniques are complicated, delicate, expensive and not reliable. Also perfect noise cancellation is impossible.

2.10 EFFECT OF MAGNETIC FIELD

References [12,45,66,67,68] studied different aspects of the effect of magnetic fields on the MOSFETs. The conclusions can be summarised as follows:

When the MOSFET is acted upon by a relatively low magnetic field (~0.1 to 0.3 T), lateral deflection of electrons occurs in the channel by the resulting magnetic force and a transversal Hall voltage is created, but no serious effects on the energy band structure is observed. This effect causes, as will be shown in chapter 3, more mobility degradation.
Stronger magnetic field ( > 0.3 T) causes conduction and balance band edge splitting and leads, therefore, to the creation of heavy and light electrons and holes. However, the energy band gap width remains unaffected.

2.11 CONCLUSIONS

In this chapter we have reviewed all the principal effects and consequences related to the hot carrier heating phenomenon and its dependence on the MOSFET biasing and geometry. Attention has been given to the different mechanisms of channel mobility degradation, and to the consequent evolution of the channel depth since both of them strongly affect the MOSFET operation and performance and may be used as a measure of the device reliability and stability. Also the possible property fluctuations caused by the application of low-level and high-level magnetic fields have been investigated.

The basic concepts of this chapter are used and further developed in the subsequent chapters.
CHAPTER 3

NEW THEORETICAL DEVELOPMENT IN THE CARRIER HEATING, NOISE GENERATION, STRESSING AND MAGNETIC PROPERTIES

PART 1: CARRIER HEATING PHENOMENA
PART 2: NOISE REDUCTION
PART 3: STRESSING
PART 4: MAGNETIC PROPERTIES
PART 5: CONCLUSIONS
3.1 GENERAL INTRODUCTION

As the trend towards progressively smaller semiconductor devices continues, the carrier and crystal heating effect becomes noticeable and unavoidable. Such devices may be operated at power levels as high as 400 μW/μm² of the gate area which corresponds to a volume power density in the active region as high as $10^9$ W/cm³. This is sufficient to disturb the device operation and performance, for instance, mobility degradation, noise and leakage current enhancement, threshold voltage shift and instability. For the sake of accurate modelling of the VLSI MOSFET devices, circuits and systems, it is important to model and measure the channel temperature and to evaluate its effects on the hot carrier gate and substrate currents as well as the device threshold voltage and mobility [4,8,10,11,15,18,69].

The prediction of the gate and substrate currents and the threshold voltage instability in MOSFETs have become extremely useful for VLSI design and for the evaluation of the device and circuit performances. Both gate and substrate currents are the result of the hot carrier effects and are much more sensitive than drain current, to the device electric fields and oxide processing. Several drain current models have been established and used to predict the MOSFET parameters related to the channel current [4,6,7,8,9,10,23,69,89].

In this chapter we present simple but adequate modelling for the hot carrier gate and substrate current in rectangular-gate (traditional) and trapezoidal-gate (novel) MOSFETs which have been published [6,8,89,116]. Electrons are heated up by the channel fields; consequently a small fraction of these electrons attains enough energy to overcome the energy barrier existing at the Si-SiO₂ interface and are therefore capable of penetrating into the gate insulator. Some of these energetic electrons lose their energy in bombardment with the Si-SiO₂ interface and create defects in it.

The rest of the chapter is divided into five main parts. Part 1 reviews E and D-type MOSFET and presents new theoretical developments of RG and TG MOSFETs. In part 2 new techniques for noise cancellation are developed. Part 3 presents new approach to the carrier mobility degradation for X-ray stressing and UV stressing of MOSFET devices. Part 4 discusses the magnetic properties of MOSFET and its relation to semiconductor thin films like a-GaAs. Finally, an overview of the results of the above parts are presented.
PART 1: CARRIER HEATING PHENOMENA
3.2 CURRENT-VOLTAGE CHARACTERISTICS OF MOSFET

This section comprises the current voltage characterisation of the enhancement rectangular and trapezoidal gate MOSFETs.

3.2.1 Enhancement Mode MOSFET (E-MOSFET)

The work of this thesis deals with the traditional rectangular formed gate MOSFET. For reasons concerning the enhancement of carrier heating phenomena without the need for reducing the device geometry, a trapezoidal formed gate MOSFET (TG-MOSFET) has been introduced and analyzed. The same procedure of analysis on modelling generally used by others [1,2] was adopted. However, the novelty in this work is the manipulation of short channel devices ($L = 0.5$ to $2 \mu m$) while formal work dealt with long channel devices ($L = 2$ to $10 \mu m$) [3,10]. Also the majority of the studies were focused on p-channel while the work presented in this thesis based on n-channel. The short n-channel devices are much more susceptible to carrier heating and related phenomena.

a) Rectangular Gate (RG-MOSFET)

The derivation of the RG-MOSFET I-V characteristics proceeds as follows: it is assumed that the inversion layer is established, the source is biased to the same substrate voltage and the device is operating in its linear region, where the drain voltage $V_{DS}$ is kept smaller than the saturation value $V_{DSS}$ ($V_{DSS} V_{GS} = V_T$ as will be shown later) with the channel current $I_{DS}$ flowing from the source to the drain. Fig. (3-1) shows a cross section in an n-channel MOSFET and illustrates the charge distribution in its surface, from which we have [1,2,22]

$$Q_G^* + Q_B^- + Q_n^- + Q_{DS}^* = 0 \quad (3-1)$$

$$Q_G^* = C_{ox} (V_{GS} - V_s) \quad (3-2)$$

where

$Q_G$ is the gate electrode charge density (should be positive to compensate for other charges).
Fig. (3-1)

A cross section in N-channel MOSFET.
**Q_B** is the depletion layer immobile charge density (it is negative in this case).

**Q_n** is the mobile electron charge density inside the channel.

**Q_SS** is the surface charge density (it is always positive).

**C_{ox}** is the gate oxide capacitance per unit area \( \left( \frac{e_{ox}\epsilon_o}{h_o} \right) \)

**\epsilon_{ox}** is the dielectric constant of SiO\(_2\) (\( \epsilon_{ox}=4 \)).

**h_o** is the oxide thickness (450 Å).

**V_x** is the potential at point \( x \) in the MOSFET channel.

The channel current \( I_x(y) \) passing through a channel sheet of thickness \( dy \) can be formulated by:

\[
I_x(y) = \rho \, \nu \, Z \, dy
\]  

(3-3)

with \( \rho \) is the volume charge density of electrons in the MOSFET surface, \( \nu \) is the electron velocity along the channel. They are given, respectively, by:

\[
\rho = q \, n(y)
\]  

(3-4)

\[
\nu = \mu(y) \frac{dV_x}{dx}
\]  

(3-5)

where

\( n(y) \) is the electron concentration in the MOSFET surface.

\( \mu(y) \) is the electron mobility at position \( y \).

\( \frac{dV_x}{dx} \) is the channel longitudinal field at position \( x \) from the source.

Substituting from Eqs. (3-4) and (3-5) into Eq. (3-3) yields

\[
I_x = q \, n(y) \, \mu(y) \frac{dV_x}{dx} \, Z \, dy
\]  

(3-6)

The mobile charge density \( Q_n \) in the MOSFET channel is given by
\[ Q_n = \int_0^\gamma q \, n(y) \, dy \quad (3-7) \]

and the most probable value of the channel mobility \( \mu \) which may be considered constant throughout the channel depth is given by:

\[ \mu = \frac{\int_0^\gamma q \, \mu(y) \, n(y) \, dy}{\int_0^\gamma q \, n(y) \, dy} \quad (3-8) \]

combining Eqs. (3-6) and (3-8) gives:

\[ I_x(y) \, dx = \mu \, Z \, Q_n \, dV_x \quad (3-9) \]

And by substituting Eqs. (3-1) and (3-2) into (3-9) we obtain:

\[ I_x(y) \, dx = -\mu \, Z[C_\alpha(V_{GS} - V_x) + Q_B + Q_{SS}] \, dV_x \quad (3-10-a) \]

which rearranges to:

\[ I_x(y) \, dx = -C_\alpha \, \mu \, Z[V_{GS} - V_T - V_x] \, dV_x \quad (3-10-b) \]

with \( V_T \) being the threshold value of the gate voltage over which the surface inversion occurs. It is given by:

\[ V_T = -\frac{Q_B + Q_{SS}}{C_\alpha} \quad (3-11) \]
The total drain current $I_{DS}$ is obtained by integrating Eq. (3-10-b) with the boundary conditions: $x = 0$, $V_x = 0$ and $x = L$, $V_x = V_{DS}$, with $L$ being the channel length, then:

\[
\int_{0}^{L} I_x dx = -\int_{0}^{V_{DS}} C_{o x} \mu Z [(V_{GS} - V_{T}) - V_x] dV_x
\]

\[I_{DS} L = -C_{o x} \mu Z \left( (V_{GS} - V_{T}) V_{DS} - \frac{V_{DS}^2}{2} \right) \]  (3-12)

This equation is valid as long as the transistor is operated in its ohmic region ($V_{DS} < V_{DSS}$). When $V_{DS}$ exceeds its saturation value $V_{DSS}$, the channel is pinched-off beside the drain and a high resistance region is established within it. When $V_{DS}$ is increased further, the pinch off is enhanced further and the high resistance region is also increased and so on. This means that, when $V_{DS}$ is increased, $I_{DS}$ instead of increasing proportionally with $V_{DS}$ (as the case in its ohmic region) it saturates because of the increased resistance of the pinch-off region.

It saturates at a certain value $I_{DSS}$, which depends, as will be shown below, on the gate biasing voltage. In this case, the MOSFET is said to be switched into its saturation region of operation ($V_{DS} \geq V_{DSS}$). The value of $V_{DSS}$ at which $I_{DS}$ saturates can be deduced from equating the first derivative of Eq. (3-12) to zero,

\[V_{DSS} = (V_{GS} - V_{T}) \] (3-13)

and the saturation value of $I_{DS}$ is calculated from Eq.(3-12) by substituting $V_{DS} = V_{DSS}$ and thus the evaluation of $I_{DS}$ in the ohmic and saturation regions of operation is achieved,

\[I_{DS} = -C_{o x} \mu Z \left( (V_{GS} - V_{T}) V_{DS} - \frac{V_{DS}^2}{2} \right) \] $V_{DS} < V_{GS} - V_{T}$  \hspace{1cm} (3-14-a)

\[I_{DS} = -C_{o x} \mu Z \frac{(V_{GS} - V_{T})^2}{2} \] $V_{DS} \geq V_{GS} - V_{T}$ \hspace{1cm} (3-14-b)
The negative sign disappears from Eq. (3-14-a,b) when taking the sign of the electron charge into consideration. A gate-voltage induced pn junction is established in the MOSFET surface between the n-Channel and the p-Substrate. This junction is reverse biased by the surface potential \( \phi_s \) (\( \phi_s > 2\phi_p \), with \( \phi_p \) the quasi-Fermi level potential of the p-type substrate). Therefore a wide depletion region is elaborated between the channel and the substrate which keep a very good isolation of the channel from any substrate activities. The width \( w \) of this depletion layer can be expressed in terms of the silicon dielectric constant \( \varepsilon_{si} \) and the substrate background concentration \( N_A \) as

\[
W = \sqrt{\frac{2 \varepsilon_{si} \varepsilon_0 |2\phi_p|}{q N_A}}
\]  

(3-15)

We observe in Eq. (3-15) that \( 2\phi_p \) is used instead of \( \phi_s \) (\( \phi_s > 2\phi_p \)) because the band bending increases from zero to \( 2\phi_p \) and over this range of variation the surface population changes from \( P \) at \( \phi_s = 0 \) to \( n=P \) at \( \phi_s = 2\phi_p \).

As the gate voltage increases over the value corresponding to \( 2\phi_p \), stronger surface inversion occurs and more electrons are introduced into the MOSFET surface to accommodate the increase of \( V_{GS} \) while \( w \) remains constant at the value corresponding to \( 2\phi_p \). In other words \( w \) will have a certain maximum value which is given by Eq. (3-15) regardless of any increase of the surface potential over \( 2\phi_p \).

b) Trapezoidal Formed Gate MOSFET (TG-MOSFET)

In recent years many applications, based on hot carrier gate current and/or need to employ low leakage-current and fast response MOSFETs, have been introduced [70-72]. These applications have to employ short channel MOSFETs as hot-carrier gate current sources. Unfortunately, the leakage currents of these MOSFETs have been seen to be relatively high. However, the trapezoidal gate TG-MOSFET, investigated in this work has been shown to yield the high-level hot-carrier gate current (~2 decades greater than that given by the rectangular gate device RG-MOSFET) at reduced leakage current (~4 times) and smaller parasitic capacitance (~10 times) [6]. We also found that, the gate form of the TG-MOSFET cancels the channel-length modulation noise (25 times) and appreciably minimizes the device \( 1/f \) noise.
This new performance will allow for the integration of a greater number of MOSFETs per unit surface area and make it possible to achieve greater circuit and system complexity. It helps also to improve both the dynamic response and performance of the switched capacitor (SC) circuits and other VLSI applications and reduce the feed through and other parasitics [70-72]. Characterization and modelling of the TG-MOSFET becomes, therefore, extremely useful. A two-dimensional model is elaborated to evaluate the distribution of the longitudinal and transversal channel fields \( (E_x, E_z) \) and potentials \( (V_x, V_z) \). A channel current model is also established and used to predict the \( I_{DS} \) dependence on the device geometry and biasing conditions. Besides, the effect of the gate form on the device noise is investigated.

Formar studies have been performed on p-channel trapezoidal gate MOSFETs of channel length \( L \) ranging from 10 to 4 \( \mu \)m [5] while this work deals with n-channel devices with \( L \) ranging from 4 to 0.5 \( \mu \)m [6]. The formal modelling presented in [5] was not complete and suffers from ambiguity, which shows the need for a complete and accurate modelling. This modelling is necessary, as will be shown in section (3-3-4b), for the modelling and evaluation of the lateral potential and field distributions \( V_z(x) \) and \( E_x(x) \).

Figure (3-2) shows a top view and cross section of the TG-MOSFET, where \( L \) is the channel length, \( Z_o \) and \( Z_L \) are the channel widths at the source and drain respectively, \( Z_x \) is the channel width at distance \( x \) from the source and \( \beta \) is the slope of the channel sides,

\[
\beta = \frac{Z_o - Z_L}{2L} \tag{3-16}
\]

and

\[
Z_x = Z_o (1 - mx) \tag{3-17}
\]

with

\[
m = \frac{2\beta}{Z_o} \tag{3-18}
\]
A top view and cross section in a TG-MOSFET.
The current-voltage characteristic equations of the TG-MOSFET can be derived as follows, assuming that the effective channel depth $d_0$ is very small with respect to both the oxide thickness $h_0$ and the channel length $L$, then the channel current at any position $x$ is given by:

$$I_x = \int_0^y q n(y) \mu(y) E_x Z_x \, dy \quad \text{(3-19)}$$

where $n(y)$, $\mu(y)$, are respectively, the mobile-carrier density and mobility in device surface at distance $y$ from the Si-SiO$_2$ interface. Substituting by:

$$E_x = -\frac{dV_x}{dx},$$

$$\mu = \frac{\int_0^y q n(y) \mu(y) \, dy}{\int_0^y q n(y) \, dy} = \frac{1}{Q_n} \int_0^y q n(y) \mu(y) \, dy,$$

and

$$V_T = -\frac{Q_g + Q_{SS}}{C_{ox}}$$

yields

$$I_x = \mu Z_x C_{ox} (V_{gs} - V_T - V_x) \frac{dV_x}{dx} \quad \text{(3-20)}$$

combining Eqs. (3-17) and (3-20) and substituting by:

$$V_g = V_{gs} - V_T$$

we get

$$\frac{I_x \, dx}{(1 - mx)} = \mu Z_0 C_{ox} (V_g - V_x) \, dV_x \quad \text{(3-21)}$$
By integrating Eq. (3-21) along the channel length \( L \), the \( I_{DS}/V_{DS} \) current equation in the ohmic and saturation regions are obtained:

\[
I_{DS} = \frac{m C_{ox} \mu Z_0}{\ln(1-mL)^{-1}} \left( V_g V_{DS} - \frac{V_{DS}^2}{2} \right) \quad V_{DS} < V_g \\
I_{DSS} = \frac{m C_{ox} \mu Z_0}{2\ln(1-mL)^{-1}} V_g^2 \quad V_{DS} > V_g
\]  

(3-22-a)  

(3-22-b)

3.3 ACCURATE MODELLING AND CHARACTERIZATION OF MOSFETs IN SATURATION

In the modelling of RG MOSFETs (Eq.(3-14-a,b)) it was investigated that the channel current \( I_{DS} \) saturates to a certain characteristic value \( I_{DSS} \) (when \( V_{DS} \) exceeds its saturation value \( V_{DSS} \)) and remains thereafter constant even if \( V_{DS} \) is furtherly increased [1,2]. The measurements performed on test devices of different geometries (\( L-0.5 \mu m \) to 5 \( \mu m \), \( Z - 3 \mu m \) to 100 \( \mu m \) and \( h_0 - 400\degree \) to 1200\degree) revealed that \( I_{DS} \) increases proportionally but very slightly with \( V_{DS} \) inside the saturation region of operation. Practical and theoretical analysis of this behaviour investigated that the ohmic part of the channel length shrinks as the device is switched into its saturation region and continues to get shorter as \( V_{DS} \) increases further. To evaluate this behaviour and study its effect in the MOSFET operation and performance, it was necessary to elaborate a more accurate model for this region of operation. This model helps, as will be shown, to develop the hot carrier gate and substrate current theories and to investigate more precisely the evolution of the device threshold voltages. The novelty of this work related to the modelling is the elaboration of new experimental techniques for the determination of the channel depth \( d_0 \) and pinch off region length \( \Delta l \).

3.3.1 General Considerations

In analyzing the characteristics of MOSFET transistors several simplifying assumptions have to be used:
a) Gradual Channel Approximation

In this approximation it is assumed that the rate of change of the drift field along the channel $dE_x / dx$ is very small compared to the rate of change of the gate-voltage-induced field in the channel normal to the surface $dE_y / dy$.

In general, if the effective depth of the channel $d_o$ is very small compared to the channel length $L$, then it is to be expected that the gradual approximation will be valid over a substantial portion of the channel extending from the source to some point near the drain (at a distance $\Delta l$ from the drain). The drain region $\Delta l$ will be a space charge limited region and the gradual channel approximation is no longer valid.

b) Shallow Channel Approximation

The maximum potential drop across the surface inversion layer will not exceed half the band gap potential of the semi-conductor by more than a few $kT$, even if the inversion layer is degenerate. For silicon, the drop across the inversion layer will be in the order of 0.5 V or less. Hence, if the potential drop between the gate and the channel is several volts or greater, we can assume that most of the potential drop occurs across the oxide and that the total channel sheet charge density $Q(x)$ at the position $x$ (from the source) can be expressed as:

$$Q(x) = -C_{ox}[V_{GS} - V_x]$$  \hspace{1cm} (3-23)

In this approximation it is also assumed that the channel depth $d_o$ is much smaller than the oxide thickness $h_o$.

c) Negligible Substrate Gating of the Channel

The penetration of the drain field lines (see Fig. (3-3)) into the source region of the channel $(L-\Delta l)$ affects the density of mobile carriers and hence the channel conductance. This effect depends on the spacing between the metal gate and the substrate. Since the substrate is slightly p-type and acts as a control electrode just as in the P-N junction. This spacing includes the space-charge or depletion region.
Fig (3-3)
Effect of the drain potential on the channel charge distribution.

Fig (3-4)
Channel potential-well of the TG-MOSFET.
extending from the inversion layer channel into the substrate. For a sufficiently low
doping density in the substrate \((N_A \ll 10^{14}/\text{cm}^3)\) which is not the case, this spacing
may become as large or may even be greater than the channel length when the drain
voltage is in the saturation region. Under these conditions penetration of the drain field
lines into the source region of the channel may be significant and the MOSFET model
must be modified. Therefore the drain has (in our case) a negligible effect on the
channel conductance.

3.3.2 Current-Voltage Characteristics

From the above discussion we assume the validity of three important
assumptions which should be introduced to simplify the analysis:

1) A constant mobility \(\mu_o\).
2) Both a gradual and shallow channel approximation throughout the entire
channel length.
3) Negligible substrate gating of the channel.

It has been shown from the traditional current-voltage modelling that:

\[
I_{DS} = C_{ox} \mu_o \frac{Z}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad V_{DS} < V_{GS} - V_T \tag{3-24-a}
\]

\[
I_{DS} = C_{ox} \mu_o \frac{Z}{L} \left( \frac{(V_{GS} - V_T)^2}{2} \right) \quad V_{DS} \geq V_{GS} - V_T \tag{3-24-b}
\]

and seen that a pinch off is established beside the drain at \(V_{DS} \geq V_{GS} - V_T\).

In fact, there is never complete pinch-off at the drain. Complete pinch-off is
only mathematical fiction arising from the gradual channel approximation. In reality
as \(V_{DS}\) approaches \(V_{GS} - V_T\) the gradual channel approximation begins to break down,
and the drain region must be treated differently from the source region.

To determine the drain voltage at which the drain region begins to form, the
rate of change of the drift field \(\frac{dE_x}{dx}\) near the drain must be compared with
the rate of change of the field normal to the channel \(\frac{dE_y}{dy}\), from Eq. (3-24-a)
we have:

\[ I_{DS} = C_{ox} \mu_0 \frac{Z}{L} \left[ V_g V_{DS} - \frac{V_{DS}^2}{2} \right] \]

with \( V_g = V_{GS} - V_T \)

which may be developed to:

\[ I_{DS} = C_{ox} \mu_0 \frac{Z}{2x} \left[ V_g^2 - (V_g - V_x)^2 \right] \]  \hspace{1cm} (3-25)

Solving Eq.(3-25) for \( V_x \) yields:

\[ V_g - V_x = \left[ V_g^2 - \frac{2x}{\mu_0 C_{ox} Z} I_{DS} \right]^{1/2} \]  \hspace{1cm} (3-26)

differentiating twice with respect to \( x \) yields:

\[ \frac{dV_x}{dx} = -\frac{1}{2} \left[ V_g^2 - \frac{2x}{\mu_0 C_{ox} Z} I_{DS} \right]^{-1/2} \left( -\frac{2I_{DS}}{\mu_0 C_{ox} Z} \right) \]  \hspace{1cm} (3-27)

\[ \frac{d^2V_x}{dx^2} = \frac{1}{4} \left[ V_g^2 - \frac{2x}{\mu_0 C_{ox} Z} I_{DS} \right]^{-3/2} \left( \frac{2I_{DS}}{\mu_0 C_{ox} Z} \right)^2 \]  \hspace{1cm} (3-28)

As the drain approaches pinch-off, equation (3-25) gives a good approximation:

\[ \frac{2x}{C_{ox} \mu_0 Z} I_{DS} = V_g^2 \]

Substituting by \( x = L \) yields,

\[ \left( \frac{2I_{DS}}{C_{ox} \mu_0 Z} \right)^2 = \frac{V_g^4}{L^2} \]  \hspace{1cm} (3-29)
and
\[
\left( V_g^2 - \frac{2x}{\mu_0 C_{ax} Z} I_{DS} \right)^{\frac{3}{2}} = \left[ V_g^2 - V_g^2 + (V_g - V_{DS})^2 \right]^{\frac{3}{2}}
\]
\[= (V_g - V_{DS})^3 \quad (3-30)\]

From Eqs. (3-28), (3-29) and (3-30) we get:
\[
\frac{dE_x}{dx} = \frac{V_g^4}{4L^2 (V_g - V_{DS})^3} = \frac{V_g}{4L^2 \left( 1 - \frac{V_{DS}}{V_g} \right)^3} \quad (3-31)
\]

The rate of change of the normal field $E_y$ near the drain may be approximated as:
\[
\frac{dE_y}{dy} \propto \frac{E_{ps}}{d_o} = \frac{\epsilon_{ax} F_{ax}}{\epsilon_{st} d_o} = \frac{\epsilon_{ax} (V_g - V_{DS})}{\epsilon_{st} d_o h_o} \quad (3-32)
\]

where $E_{ps}$ is the normal field inside the source region of the channel and $\epsilon_{ax}$, $\epsilon_{st}$ being the oxide and the silicon dielectric constants respectively.

The condition for the formation of the drain region is:
\[
\frac{dE_x}{dx} = \frac{dE_y}{dy}
\]
which leads to:
\[
\frac{V_g}{4L^2 \left( 1 - \frac{V_{DS}}{V_g} \right)^3} = \frac{\epsilon_{ax} (V_g - V_{DS})}{\epsilon_{st} d_o h_o}
\]
or

\[
\frac{V_g}{4L^2 \left(1 - \frac{V_{DSS}}{V_g}\right)^3} = \frac{\varepsilon_{ox} (V_g - V_{DSS})}{\varepsilon_{st} d_o h_o}
\]

from which

\[
\left(\frac{\varepsilon_{st} d_o h_o}{4 \varepsilon_{ox} L^2}\right)^{\frac{1}{4}} = 1 - \frac{V_{DSS}}{V_g}
\]

or

\[V_{DSS} = V_g [1 - K]\] (3-33-a)

with \(K\) constant given by:

\[K = \left(\frac{\varepsilon_{st} d_o h_o}{4 \varepsilon_{ox} L^2}\right)^{\frac{1}{4}}\] (3-33-b)

It was observed that \(K\) is a function of the channel depth \(d_o\) which could not, till now, be experimentally determined. In section 3.6 a new experimental technique is introduced to evaluate \(d_o\) in the different modes of MOSFET operation.

It should be noticed that the channel charge is not zero at \(V_{DS} = V_{DSS}\) and that complete pinch-off does not occur. In fact for \(V_{DS} > V_{DSS}\) a space charge dominated current maintains a current continuity from the source region to the drain. Therefore saturation of the drain current for \(V_{DS} > V_{DSS}\) may be explained by identical arguments and the current in the source region of the channel during saturation is given by:

\[I_{DS} = C_{ox} \mu_o \frac{Z}{2L} V_g^2 (1 - K)^2 \quad V_{DS} > V_{DSS}\] (3-34)
3.3.3 Evaluation of the Pinch-off Region Length

Consider first the effect of the mobile channel charge as compared with the charge induced on the gate electrode by the field lines which start, as shown in Fig. (3-3), on the drain electrode and terminate on the gate electrode.

Assuming negligible influence of the gate field gradient on the charge distribution within the drain region, or

\[
\frac{dE_x}{dx} \approx \frac{dE_y}{dy}
\]

then using Poisson's equation, the channel current \( I_{DS} \) can be given by:

\[
I_{DS} = Q_x \nu_x = \left[ \frac{\varepsilon_{st} d_o Z}{\varepsilon_0} \right] \frac{dE_x}{dx} \mu_o E_x \tag{3-35}
\]

with \( Q_x \) being the mobile charge density due only to the one dimensional drain field. Assuming that the drift field at the end of the drain region \( E_x(L - \Delta t) \) is very small compared to the drain field at the drain electrode \( E_x(L) \) then by integrating Eq. (3-35) twice,

\[
I_{DS} \left|_o^{\Delta t} \right. = \left. \varepsilon_{st} d_o Z \mu_o E_x^2 / 2 \right|_o^{E(L)}
\]

\[
\left( \frac{2I_{DS}}{\varepsilon_{st} d_o Z \mu_o} \right)^{\frac{1}{2}} \cdot \frac{1}{2} E_x \left. \right|_o^{E(L)} \quad \left( \frac{2I_{DS}}{\varepsilon_{st} d_o Z \mu_o} \right)^{\frac{1}{2}} \cdot \frac{1}{2} \left. E_x \right|_o^{E(L)} = \left. \frac{2I_{DS}}{\varepsilon_{st} d_o Z \mu_o} \right)^{\frac{1}{2}} \cdot \frac{1}{2} \left. E_x \right|_o^{E(L)}
\]

\[
\left( \frac{2I_{DS}}{\varepsilon_{st} d_o Z \mu_o} \right)^{\frac{1}{2}} \cdot \frac{2}{3} \left. x^2 \right|_o^{E(L)} = V_x
\]

\[
\frac{2I_{DS}}{\varepsilon_{st} d_o Z \mu_o} \cdot \frac{4}{9} \left. x^3 \right|_o^{E(L)} = V_x^2
\]

\[
I_{DS} \left|_o^{\Delta t} \right. = \frac{9}{8} \left. \varepsilon_{st} \mu_o d_o Z V_x^2 \right|_o^{V_{DS}}
\]
This is the usual expression for a space-charge limited current through a solid with spacing \( \Delta \ell \) between the contacts and a \((V_{DS} - V_{DSS})\) across the region between contacts.

Because the current must be continuous, thus Eq.(3-36) may be equal to the second expression in Eq.(3-24) which is the saturation current through the source region, this equality leads to:

\[
C_{ox} \mu_o \frac{Z}{2L} \frac{V_{DSS}^2}{V_{DSS}^2} = \frac{9}{8} \varepsilon_{st} \mu_o d_o Z \frac{(V_{DS} - V_{DSS})^2}{\Delta \ell^3}
\]

from which,

\[
\Delta \ell = \left[ \frac{9 L d_o h_o \varepsilon_{st}}{4 \varepsilon_{ox}} \right]^{\frac{1}{3}} \left( \frac{V_{DS}}{V_{DSS}^2} - 1 \right)^{\frac{2}{3}} \tag{3-37}
\]

or

\[
\Delta \ell = k' \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}} \tag{3-38}
\]

with \( k' \) constant given by:

\[
k' = \left[ \frac{9 L d_o h_o \varepsilon_{st}}{4 \varepsilon_{ox}} \right]^{\frac{1}{3}} \tag{3-39}
\]
Equation 3-37 represents the backbone for elaborating the experimental technique of prediction of $d_0$ as will be shown in section 3.6.

From Eqs. (3-38) and (3-24-b) we deduce that,

$$I_{DS} = C_{ox} \mu_o \frac{Z}{2L \left(1 - \frac{\Delta \ell}{L}\right)} V_{DSS}^2 \quad V_{DS} \geq V_{DSS}$$

or

$$I_{DS} = C_{ox} \mu_o \frac{Z}{2L} \frac{V_{DSS}^2}{\left[1 - k' \left(\frac{V_{DS}}{V_{DSS}} - 1\right)\right]^2} \quad V_{DS} \geq V_{DSS}$$

(3-40)

3.3.4 Potential $V_x$ and Field Distribution $E_x$ in the RG and TG-MOSFET's

This section presents a study and analysis of the surface activities in the RG and TG MOSFET's in the absence of and in the presence of carrier heating phenomena. A model will be developed to evaluate the potential $V_x$ and field $E_x$ distributions. This analysis is very important for the determination of hot carrier energy distribution.

a) Case of RG-MOSFET

Referring to Eq.(3-26) the distribution of the channel potential $V_x$ can be formulated as

$$V_x = V_g - \sqrt{V_g^2 - \frac{2x}{\mu_o \alpha C_{ox} Z} I_{DS}}$$

(3-41)

i) In the ohmic region where $V_{DS} < V_{DSS}$ and

$$I_{DS} = C_{ox} \mu_o \frac{Z}{2L} \left[V_g^2 - (V_g - V_{DS})^2\right]$$

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equation (3-41) develops to:

\[ V_x = V_g \left[ 1 - \sqrt{1 - \frac{x}{L} \left( 1 - \left( \frac{V_{DS}}{V_g} \right)^2 \right)} \right] \]  \hspace{1cm} (3-41-a)

ii) In the saturation region where \( V_{DS} \geq V_{DSS} \) and

\[ I_{DS} = C_{ox} \mu_0 \frac{Z}{2L(1 - \Delta t/L)} V_{DSS}^2 \]

equation (3-41) develops to

\[ V_x = V_g \left[ 1 - \sqrt{1 - \frac{x}{(L - \Delta t)} \left( \frac{V_{DSS}}{V_g} \right)^2} \right] \]

By substitution from Eq.(3-38), we get:

\[ V_x = V_g \left[ 1 - \sqrt{1 - \frac{x}{L - k'} \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}} \left( \frac{V_{DSS}}{V_g} \right)} \right] \]  \hspace{1cm} (3-41-b)

In referring to Eq.(3-27) we can express the channel field \( E_x \) as:

\[ E_x = \frac{1}{2} \left[ \frac{V_g^2}{\mu_0 C_{ox} Z} \frac{2x}{I_{DS}} \right]^{\frac{1}{2}} \left( \frac{2I_{DS}}{\mu_0 C_{ox} Z} \right) \]  \hspace{1cm} (3-42)

i) In the ohmic region where \( V_{DS} < V_{DSS} \) and

\[ I_{DS} = C_{ox} \mu_0 \frac{Z}{2L} \left[ V_g^2 - (V_g - V_{DS})^2 \right] \]

equation (3-42) takes the form:
ii) In the saturation region where \( V_{DS} \geq V_{DSS} \) and

\[
I_{DS} = C_{ox} \mu \frac{Z}{2L \left( 1 - \frac{\Delta t}{L} \right)} V_{DSS}^2
\]

equation (3-42) can be written as follows:

\[
E_x = \frac{V_{DSS}^2}{2V_g (L - \Delta \ell) \sqrt{1 - \frac{x}{(L - \Delta \ell)} \left( \frac{V_{DSS}}{V_g} \right)^2}}
\]

or by substitution from Eq. (3-38),

\[
E_x = \frac{V_{DSS}^2}{2V_g \left[ L - k \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}} \right] \sqrt{1 - \frac{x}{L - k \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}} \left( \frac{V_{DSS}}{V_g} \right)^2}}}
\]  

(3-42-b)

b) Case of Trapezoidal Formed Gate TG-MOSFET

Owing to the trapezoidal form of the gate, additional transverse field component \( E_x \) and a corresponding transversal potential component are introduced and control, in conjunction with the longitudinal components, the operation and performance of the TG MOSFET.
b-1) **Longitudinal Potential and Field Distributions**

The channel potential distribution can be evaluated in the ohmic and saturation regions as follows:

Equation (3-22-a) can be written as,

\[
I_{DS} = \frac{m C_{ox} \mu Z_o}{2 ln (1 - m)} \left[ V_s^2 - (V_g - V_s)^2 \right] 
\]

from which,

\[
V_s = V_g \left( 1 - \sqrt{1 - \frac{2 ln (1 - m)}{m C_{ox} \mu Z_o V_g^2} I_{DS}} \right) \quad \text{(3-43)}
\]

i) **Ohmic region** \( V_{DS} < V_{DSS} \)

Combining Eqs. (3-22) and (3-43) we get,

\[
V_s = V_g \left( 1 - \sqrt{1 - \frac{ln(1 - m)}{ln(1 - mL)} \left[ 1 - \left( 1 - \frac{V_{DS}}{V_g} \right)^2 \right]} \right) \quad \text{(3-44-a)}
\]

ii) **Saturation Region** \( V_{DS} \geq V_{DSS} \)

We have two cases:

1) \( V_{DS} = V_{DSS} \) or the channel pinch-off just begins beside the drain \( V_g = V_{DS} \)

then Eq.(3-44-a) is developed to

\[
V_s = V_g \left( 1 - \sqrt{1 - \frac{ln(1 - m)}{ln(1 - mL)} \left[ 1 - \left( 1 - \frac{V_{DS}}{V_g} \right)^2 \right]} \right) \quad x \leq L \quad \text{(3-44-b)}
\]
2) $V_{DS} > V_{DSS}$, pinch-off region of length $\Delta \ell$ appears beside the drain. The source-region length of the channel $L_s$ is reduced to

$$L_s = L - \Delta \ell$$

Substituting by $L = L_s$ in Eq. (3-22-b) and combining it with Eq.(3-43), yields,

$$V_x = V_g \left( 1 - \sqrt{\frac{\ln(1-mx)}{\ln(1-mL_s)}} \right) x \leq L_s \quad (3-44-c)$$

Since the current is constant throughout the channel, then Eq.(3-21) may be written as:

$$E_x = -\frac{dV_x}{dx} = \frac{-I_{DS}}{\mu_o C_{ox} Z_o (1-mx) (V_g - V_x)} \quad (3-45)$$

We can formulate the channel field $E_x$ in the ohmic and saturation regions as follows:

i) **Ohmic Region, $V_{DS} < V_{DSS}$**

Combining Eqs. (3-22-a) and (3-45) we obtain,

$$E_x = \frac{m}{2(1-mx) \ln(1-mL_s)^{-1}} \left( \frac{V_g V_{DS} - \frac{V_{DS}^2}{2}}{V_g - V_x} \right) \quad (3-46)$$

Substituting from Eq.(3-44-a) into Eq.(3-46) we get:

$$E_x = \frac{mV_g}{2(1-mx) \ln(1-mL_s)^{-1}} \frac{\left[1 - \left(1 - \frac{V_{DS}}{V_g} \right)^2 \right]}{\sqrt{\frac{\ln(1-mx)}{\ln(1-mL_s)}} \left[1 - \left(1 - \frac{V_{DS}}{V_g} \right)^2 \right]} \quad (3-46-a)$$

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ii) Saturation Region, $V_{DS} \geq V_{DSS}$

There are also two cases:

1) $V_{DS} = V_{DSS}$ and $\Delta t = 0$

Combining Eqs. (3-22-b) and (3-45) we obtain:

$$E_x = \frac{mV_s^2}{2(1-mx) b n (1-mL)^{-1} (V_s - V_x)}$$

Substituting from Eq. (3-44-b) we get

$$E_x = \frac{mV_s}{2(1-mx) b n (1-mL)^{-1}} \left(1 - \frac{\ln(1-mx)}{\ln(1-mL)}\right)^{-1}$$  \hspace{1cm} (3-46-b)

2) $V_{DS} > V_{DSS}$, a pinch off region $\Delta t$ is formed and the source-region length of the channel shrinks to $L_s = L - \Delta t$. Substituting by $L = L_s$ in Eq.(3-46-b), $E_x$ becomes,

$$E_x = \frac{mV_s}{2(1-mx) b n (1-mL_s)^{-1}} \left(1 - \frac{\ln(1-mx)}{\ln(1-mL_s)}\right)^{-1}$$  \hspace{1cm} (3-46-c)

Equations (3-44,a,b,c) and (3-46,a,b,c) are used to evaluate the potential and field distributions in the TG MOSFET channel in the different regions of operation. They also evaluate their dependence on the device geometry and the channel-sides steepness.

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Transversal Field and Potential Distributions

The channel field is exactly longitudinal at the center of the channel while the lines of field at the lateral boundaries are parallel to the channel sides. This situation creates an additional transversal field component \( E_z \) in a direction pointing from the channel boundaries toward its center line. The \( E_x \) and \( E_z \) intensities vary with position \( x, z \) in the channel. That is why we use \( E_x(x, z) \) and \( E_z(x, z) \), respectively, instead of \( E_x \) and \( E_z \). The evaluation of \( E_x(x, z) \) and \( E_z(x, z) \) proceeds as follows: in the steady state, no additional carrier accumulation, should occur inside the channel well, i.e. \( \frac{dn}{dt} = 0 \). All carrier streams coming from the source must sweep an equal longitudinal distance \( x \) toward the drain, after a certain transit time \( t \),

\[
t = \frac{x}{\mu(x) E_x(x, 0)} = \sqrt{\frac{x^2 + \frac{z^2}{4}}{\mu(x) E_{xx}(x, z)}}
\]

Assuming that the channel mobility \( \mu(x) \) is independent of \( z \), we have

\[
E_{xx}(x, z) = E_x(x, 0) \sqrt{1 + \left( \frac{z}{2x} \right)^2}
\]  

(3-47)

Referring to Fig. (3-2), we can formulate \( E_z(x, z) \) as:

\[
E_z(x, z) = \frac{mE_{zz}}{\sqrt{1 + m^2}}(x, z)
\]

or

\[
E_z(x, z) = \frac{mE_z}{\sqrt{1 + m^2}}(x, 0) \sqrt{1 + \left( \frac{z}{2x} \right)^2}
\]  

(3-48)
Substituting by Eqs. (3-46-a) and (3-46-b) into Eq.(3-48) we can formulate \( E_z(x,z) \) in the ohmic and saturation regions:

i) In the ohmic region where \( V_{DS} < V_{DSS} \)

\[
E_z(x,z) = \frac{m^2 V_g}{2 \sqrt{1+m^2 (1-mx) \ln(1-mL)^{-1}}} \left[ 1 - \left( \frac{V_{DS}}{V_g} \right)^2 \right] \sqrt{1 + \frac{\left( \frac{z}{2x} \right)^2}{1 - \frac{\ln(1-mx)^{-1}}{\ln(1-mL)^{-1}} \left[ 1 - \left( \frac{V_{DS}}{V_g} \right)^2 \right]}}
\]

Equations (3-47) and (3-48) show that \( E_z(x,z) \) is always smaller than \( E_x(x,z) \) but both are increasing as \( z \) increases. They also increase as \( x \) increases since the increasing of \( E_x(x,o) \) with \( x \) is dominant. Integration of equation (3-48) with respect to \( z \) gives the increase occurring in the channel well potential due to \( E_z \) in the \( z \)-direction,

\[
V_z(x,z) = \int_z^0 E_z(x,z) \, dz
\]

Substituting from Eq.(3-48) yields:

\[
V_z(x,z) = \frac{mE_x(x,o)}{\sqrt{1+m^2}} \left[ z \sqrt{1+\frac{z^2}{4x^2}} + x \ln \left( \frac{z}{2} + x \sqrt{1 + \frac{z^2}{4x^2}} \right) \right]
\]
Combining Eqs. (3-46-a) and (3-46-b) with Eq.(3-49) gives the $V_z(x, z)$ distribution in the ohmic and saturation regions.

i) In the ohmic region, $V_{DS} < V_{DSS}$

$$V_z(x,z) = \frac{m^2V_g}{2\sqrt{1+m^2(1-mx)\ln(1-mL)}^{-1}} \frac{1-\left(\frac{V_{DS}}{V_g}\right)^2}{\ln(1-mx)^{-1}} \sqrt{1-\frac{\ln(1-mL)}{\ln(1-mL)^{-1}} \left[1-\left(\frac{V_{DS}}{V_g}\right)^2\right]}$$

$$\left[ z \sqrt{1+\frac{z^2}{4x^2}} + x\ln \left(\frac{z}{2} + x \sqrt{1+\frac{z^2}{4x^2}}\right) \right]$$ (3-49-a)

ii) In the saturation region, $V_{DS} \geq V_{DSS}$

$$V_z(x,z) = \frac{m^2V_g}{2\sqrt{1+m^2(1-mx)\ln(1-mL)}^{-1}} \frac{1-\left(\frac{V_{DS}}{V_g}\right)^2}{\ln(1-mx)^{-1}} \sqrt{1-\frac{\ln(1-mL)}{\ln(1-mL)^{-1}} \left[1-\left(\frac{V_{DS}}{V_g}\right)^2\right]}$$

$$\left[ z \sqrt{1+\frac{z^2}{4x^2}} + x\ln \left(\frac{z}{2} + x \sqrt{1+\frac{z^2}{4x^2}}\right) \right]$$ (3-49-b)

Figure (3-4) shows the variation of $V_z$ as a function of the position $x, z$ inside the channel. We observe that the channel well becomes increasingly deeper besides the drain which prevents electrons from escaping into the substrate. However, decreasing dramatically, the lateral-channel leakage-current $I_{L}$ ($I_{L}$ decreases exponentially with $V_z$). This renders the device suitable for the leakage-sensitive applications [7].
3.4 STUDY AND MODELLING OF THE HOT CARRIER GATE CURRENT

This section presents a study and modelling of the hot carrier phenomena and the resultant hot carrier gate current in the traditional rectangular gate and the proposed trapezoidal gate MOSFETs [6,89].

3.4.1 Hot Carrier Gate Current of RG-MOSFET

This section comprises a 2-D analysis and evaluation of the crystal temperature $T(x,y)$ in the MOSFET substrate and surface, from which the hot-carrier temperature distribution $T_e(x,y)$ and its dependence on the device biasing and geometry is deduced. Precise evaluation of the hot-carrier distribution $n(e,T_e)$ and its dependence on the same parameters is consequently investigated. This leads, however, to a more accurate evaluation of the hot-carrier injection efficiency, escape probability, mean energy and finally to the precise modelling of the hot-carrier gate current and its associated effects.

a) Crystal Temperature Distribution $T(x,y)$

When the channel of a MOSFET is switched by a strong electric field $E_x$, the mobile carriers are accelerated and gain energy. These carriers emit some of their energy into the crystal through carrier-lattice collisions [10,23,75]. When the channel field is so strong that the energy gain is greater than that lost in collisions, carrier heating takes place. The energy exchange between the hot carriers and lattice continues and tends to increase the lattice temperature $T$, especially if the lattice radiation-capability is noticeably small. This provokes stronger lattice vibrations (optical and acoustic phonons) and leads to greater interaction between hot carriers and these vibrations which decreases the hot carrier mobility $\mu$. Therefore the rate at which these carriers gain energy from the channel field $E_x \left( \frac{dE}{dt} = q \mu E_x^2 \right)$ and that at which energy is transferred to the lattice are decreased. This process continues until balance is reached between these two rates and the crystal and carrier temperatures $T$ and $T_e$ attain their steady state values.
The MOSFET power is dissipated within the channel region. As shown in Fig.(3-5), this region is sandwiched between the oxide layer (from above) and the silicon substrate (downwards). Since the thermal conductivity of Si is a thousand times greater than that of SiO₂, it is expected that most of the thermal power diffuses downwards into the substrate, and a temperature gradient, with its maximum at the channel and minimum at the bottom of the substrate, is established. Also the dissipation of power inside the channel is longitudinally position dependent owing to the nonlinear distribution of the channel potential. The channel temperature is, therefore, expected to vary with distance $x$ and to acquire maximum value besides the drain.

The evaluation of the crystal temperature $T(x,y)$ in the MOSFET surface proceeds as follows: $T(x,y)$ is related to the volume power-density $P_v(x,y)$ by the continuity equation [76]

$$\frac{\partial T(x,y,t)}{\partial t} = \alpha \nabla^2 T(x,y,t) + \frac{P_v(x,y)}{\rho_v C_t} \tag{3-50}$$

with $\alpha$ is the thermal diffusivity,

$\rho_v$ the specific mass,

and $C_t$ is the thermal capacity.

Since the channel depth $d_0$ is very small compared to the thickness of the substrate, Eq.(3-50) could be developed to:

$$\frac{\partial T(y,t)}{\partial t} = \alpha \frac{\partial^2 T(y,t)}{\partial y^2} + \frac{P_v(x,y)}{\rho_v C_t} \tag{3-51-a}$$

$$\frac{\partial T(x,t)}{\partial t} = \alpha \frac{\partial^2 T(x,t)}{\partial x^2} + \frac{P_v(x,y)}{\rho_v C_t} \tag{3-51-b}$$

Referring to Fig. (3-5), the following boundary conditions can be deduced:

$$T(x,y,0) = 0 \tag{3-52}$$

$$T(x,0,t) = T_0$$

$$\frac{\partial T}{\partial y}\bigg|_{y=H} = 0$$
Temperature distribution in MOSFET [89].

Variation of $T$ in the $X$ and $Y$ direction [89].
The solution of Eq.(3-51) with the boundary conditions of (3-52) reveals the 2-D steady state distribution of the crystal temperature \( T(x,y) \) in the MOSFET surface [23,35,50,77],

\[
T(x,y) = T_0 + \frac{d_o P_y(x,y)}{\alpha \rho_y C_t} y, \quad H - d_o > y > 0
\]  

(3-53-a)

\[
T(x,y) = T_0 + \frac{P_y(x,y)}{2 \alpha \rho_y C_t} [2Hy - (H - d_o)^2 - y^2], \quad H > y > H - d_o
\]  

(3-53-b)

The dependence of \( T \) on \( x \) comes from the dependence of \( P_y(x,y) \) on \( x \),

\[
P_y(x) = \frac{\sigma I_{DS}^2}{(C_o \mu_o Z)^2 \left[ V_g^2 - \left( \frac{2I_{DS}}{C_o \mu_o Z} \right) x \right]}
\]  

(3-53-c)

with \( I_{DS}, V_{DS}, V_{DSS} \) and \( \Delta t \) are the channel current, the drain to source voltage, the drain saturation voltage and the pinch-off region length respectively,

\[
I_{DS} = C_o \mu_o \frac{Z}{L} \left[ V_g V_{DS} - \frac{V_{DS}^2}{2} \right], \quad V_{DS} < V_{DSS}
\]  

(3-54-a)

\[
I_{DS} = C_o \mu_o \frac{Z}{2(L - \Delta t)} V_{DSS}^2, \quad V_{DS} \geq V_{DSS}
\]  

(3-54-b)

\[
V_g = (V_{GS} - V_T)
\]  

(3-54-c)

\[
V_{DSS} = V_g \left[ 1 - \frac{\varepsilon_o \varepsilon_{d_0} L}{4 \varepsilon \varepsilon_{d_0} L^2} \right]
\]  

(3-54-d)

\[
\Delta t = \left[ \frac{9 \varepsilon_o \varepsilon_{d_0} L}{4 \varepsilon \varepsilon_{d_0} L} \right]^{\frac{1}{3}} \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}}
\]  

(3-54-e)

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Figures (3-5) and (3-6) show the expected variation of $T$ in the $x$ and $y$ directions. We see that $T$ increases, in the $y$-direction, as approaching the Si–SiO$_2$ interface. It also increases in the $x$-direction as approaching the drain.

b) Carrier Temperature Distribution, $T_e(x,y)$

In the steady state, the hot carrier mobility decreases due to random collisions of carriers with lattice vibrations. It tends consequently to decrease the rate at which carriers gain energy from the channel fields and makes it equal to that at which carriers emit energy into the crystal. In this case $T_e$ and $T$ become constant and related to each other by [78]:

$$T_e = T \left[ 1 + \left( \frac{E_x}{E_c} \right)^n \right] \quad 2 > n > 1$$  \hspace{1cm} (3-55)

With $E_c$ the critical value of $E_x$ at which appreciable carrier heating starts ($E_c \sim 1.5$ V/µm for electrons and $\sim 2$ V/µm for holes). $E_x$ is position dependent [78]. It is given by:

$$E_x(x) = \frac{I_{DS}}{C_{ox} \mu_o Z \sqrt{V_g^2 - \left( \frac{2I_{DS}}{C_{ox} \mu_o Z} \right) x}}$$ \hspace{1cm} (3-56)

Substituting from Eq. (3-56) into Eq. (3-55) yields:

$$T_e(x,y) = T(x,y) \left[ 1 + \left( \frac{I_{DS}}{C_{ox} \mu_o Z E_c \sqrt{V_g^2 - \left( \frac{2I_{DS}}{C_{ox} \mu_o Z} \right) x}} \right)^n \right]$$ \hspace{1cm} (3-57)

Equation (3-57) shows that $T_e$ increases with $x$, while it remains nearly constant over all the channel depth.
c) Carrier Energy Distribution

When the channel field is so small that thermal equilibrium conditions are established at a crystal temperature $T$ equal to the room temperature, the density of the free carriers, over all the channel length $L$, varies with the carrier energy $e$ and the carrier temperature $T_e$ according to the well known Maxwell Boltzmann distribution [44,79]:

$$n(e,T_e) = N_c e^\frac{e-e_F}{kT_e}$$  \hspace{1cm} (3-58)

When this distribution is adopted in the model used to evaluate the hot-carrier gate-current $I_g$, a noticeable deviation of the simulation results below measurements were observed. These deviations are seen to increase when raising the biasing voltages $V_{DS}$ and $V_{GS}$ and/or the channel length $L$ is shortened. A new distribution which is bias and device geometry dependent should, therefore, be derived. However as carrier heating takes place due to operation of strong channel fields, $T$ increases over that of room temperature and $T_e$ no longer becomes constant over the channel length. The free carrier distribution $n(e,T_e)$ deviates therefore from being the above mentioned Maxwell-Boltzmann distribution. A perturbation term $\delta n(e,T_e)$ should be added to that given by equation (3-58) to describe the new environment [79,80,81]. The following distribution function is proposed.

$$n(e,T_e) = N_c e^\frac{e-e_F}{kT_e} + \delta n(e,T_e) \hspace{1cm} (3-59-a)$$

with

$$\delta n(e,T_e) = \Delta T_e \left( \frac{\partial n(e,T_e)}{\partial T_e} \right) + \frac{\Delta T_e^2}{2} \left( \frac{\partial^2 n(e,T_e)}{\partial T_e^2} \right) + ... \hspace{1cm} (3-59-b)$$

combining Eqs. (3-59-a) and (3-59-b) yields

$$n(e,T_e) = N_c \left[ 1 + \left( \frac{e-e_F}{kT_e} \right) \frac{\Delta T_e}{T_e} + \left( \frac{e-e_F}{kT_e} \right) \left( \frac{\Delta T_e}{2kT_e} - 1 \right) \left( \frac{\Delta T_e}{T_e} \right)^2 \right] e^\frac{e-e_F}{kT_e}$$

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The third term in between the brackets is negligibly small with respect to the second one, then

\[ n(e,T_e) = N_e \left[ 1 + \left( \frac{e - e_f}{kT_e} \right) \frac{\Delta T_e}{T_e} \right] e^{-\frac{e - e_f}{kT_e}} \] (3-60)

Since \( T_e \) is position and bias dependent (see equation (3-57)) then \( n(e,T_e) \) and \( \delta n(e,T_e) \) will also be functions of position \( x, y \) and biasing voltages \( V_{GS} \) and \( V_{DS} \). \( n(e,T_e) \) and \( \delta n(e,T_e) \) increase as \( V_{GS}, V_{DS} \) are increased and/or \( L \) is shortened. Simulation and experimental work show that the use of this distribution removes the above mentioned inconsistency between the theory and measurements.

d) Hot-Carrier Gate-Current Model

The hot carrier gate current \( I_g \) results from the injection of hot carriers into the oxide and the transport of these carriers towards the gate electrode [10,75]. Figure (3-7) shows a cross section in a MOSFET structure with the mechanism shown of the creation of \( I_g \). Referring to Figs.(3-5) and (3-7), the formulation of \( I_g \) proceeds as follows:

\[ I_g = \int_o^L \rho_{ox} v_{ox} Z \, dx \] (3-61)

with \( \rho_{ox} \) being the oxide mobile charge density. It is given, in terms of the channel mobile charge density \( \rho_{ch} \), the injection efficiency \( P_{inj} \) and the escape probability \( P_{esc} \), by [10]:

\[ \rho_{ox} = P_{inj} \rho_{esc} P_{ch} \] (3-62)

and \( v_{ox} \) being the hot carrier velocity inside the oxide. It is given in terms of the oxide carrier mobility \( \mu_{ox} \) and oxide field \( E_{ox} \), by [10,23]:

\[ v_{ox} = \mu_{ox} E_{ox} \] (3-63-a)
Fig (3-7)

Mechanism of creation of $I_g$ [89]
The probability of injection is defined as [12,23],

\[ P_{\text{inf}} = \frac{n(\varepsilon > \phi_B)}{n(\varepsilon > \varepsilon_c)} \]

substituting from equation (3-60) yields:

\[ P_{\text{inf}} = \left[ 2 + \frac{\phi_B}{kT_e} \right] e^{-\frac{\phi_B}{kT_e}} \quad \Delta \phi \geq 0 \]  
(3-64-a)

\[ P_{\text{inf}} = \left[ 2 + \frac{\phi_B}{kT_e} \right] e^{-\frac{\phi_B}{kT_e}} \quad \Delta \phi < 0 \]  
(3-64-b)

with

\[ \Delta \phi = \frac{e_g}{2} - \frac{kT_e}{q} \ln \left[ \frac{C_{\alpha x}}{d_o n_i} (V_{GS} - V_T - V_s) \right] \]  
(3-65)

and \( e_g \) the energy gap width (1.1eV).

\( E_{\alpha x} \) the critical value of the oxide field (~1.1 x 10^8 V/m) over which, \( \mu_{\alpha x} \) begins to decrease as increasing \( E_{\alpha x} \) further.
Equation (3-64) is only valid for hot-carriers existing at the Si–SiO₂ interface. For those carriers existing deeper in the channel, only \( \exp(-y/\ell_r) \) carriers of the total number, existing at distance \( y \) from the Si–SiO₂ interface, will succeed in arriving at the interface, \( \ell_r \) being the mean free path of hot carriers in silicon (\( \sim 40\,\text{Å} \)) [10]. The worst case concerns carriers existing at the bottom of the channel (\( y = d_o \), with \( d_o \) being the channel depth). Also the potential barrier peak is shifted by a distance \( \lambda_o \) (\( \sim 10\,\text{Å} \)) into the oxide due to the interface image forces. This decreases \( P_{\text{inj}} \) by a factor of \( \exp(-\lambda_o/\ell_{ox}) \), with \( \ell_{ox} \) being the mean free path of hot carrier inside the oxide (\( \sim 16\,\text{Å} \)). Equation (3-64) develops, therefore, to:

\[
P_{\text{inj}} = \left[ 2 + \frac{\phi_B}{kT_e + \Delta \phi} \right] \exp \left[ -\left( \frac{\phi_B}{kT_e + \frac{d_o}{\ell_r}} + \frac{\lambda_o}{\ell_{ox}} \right) \right] \quad \Delta \phi \geq 0 \tag{3-66-a}
\]

\[
P_{\text{inj}} = \left[ 2 + \frac{\phi_B}{kT_e} \right] \exp \left[ -\left( \frac{\phi_B}{kT_e + \frac{d_o}{\ell_r}} + \frac{\lambda_o}{\ell_{ox}} \right) \right] \quad \Delta \phi < 0 \tag{3-66-b}
\]

and

\[
P_{\text{esc}} = \left[ 1 - \frac{\phi_B}{\varepsilon_m} \right] \tag{3-67}
\]

with \( \varepsilon_m \) the mean energy of hot carriers. It is given by [80,81]:

\[
\varepsilon_m = \phi_B + \frac{\int_{\phi_B}^{\infty} n(e,T_e) e \, de}{\int_{\phi_B}^{\infty} n(e,T_e) \, de} \tag{3-68}
\]

substituting from Eq.(3-60) into Eq.(3-68) yields,

\[
\varepsilon_m = \phi_B + kT_e + \frac{2(kT_e)^2}{\phi_B + 2kT_e} \tag{3-69}
\]

substituting from Eq.(3-62) up to (3-69) into Eq.(3-61) yields

\[
I_s = I_{sn} \quad V_{DS} < V_{DSS} \tag{3-70-a}
\]
\( I_g = I_{gn} \left( 1 - \frac{\Delta \ell}{L} \right) - I_{gp} \quad V_{DS} \geq V_{DSS} \)  

(3-70-b)

with [10,75]

\[
I_{gn} = \frac{ZC_{ox}}{d_o} \int_0^L \mu_{ox} E_{ox} (V_{GS} - V_T - V_x) \left( 1 - \sqrt{\frac{\phi_{Bn}}{\epsilon_m}} \right)
\]

(3-71-a)

\[
\left[ \left( 2 + \frac{\phi_B}{kT_e + \Delta \phi} \right) \exp \left[ - \left( \frac{\phi_{Bn}}{kT_e} + \frac{d_o}{\ell_r} + \frac{\lambda_o}{\ell_{ox}} \right) \right] \right] dx
\]

(3-71-b)

\[
I_{gp} = \frac{ZC_{ox}}{2d_o} \left( \frac{V_g^2}{(V_{DS} - V_g)} \right) \int_{L-\Delta \ell}^L \mu_{ox} E_{ox} \left( 1 - \sqrt{\frac{\phi_{BP}}{\epsilon_m}} \right)
\]

(3.4.2) Evaluation and Modelling the Hot Carrier Gate Current in TG-MOSFET

The hot carrier gate current density can be evaluated as follows:

\[
J_{gn} = \frac{1}{A} \int_{X_g}^L \rho_{inv}(x) v_{ox}(x) Z(x) dx
\]

(3-72)

where \( \rho_{inv}(x) \) is the charge density of hot carriers injected into the oxide layer. It is given by Eq.(3-64).

\( v_{ox}(x) \) is the hot carrier velocity in the oxide given by[36]:

\[
v_{ox} = \mu_{ox} E_{ox}
\]

(3-73)
\( Z(x) \) is the channel width at distance \( x \) from the source given by Eq. (3-17).

\( A \) is the cross-section of the gate over the channel region extending from position \( X_c \) (\( X_c \) is the position at which \( E_x \) becomes to be greater than \( E_c \)) to position \( L \). It is given by (see Fig. (3-2):

\[
A = \frac{Z_o (L - X_c)}{2} \left[ 2 - m (L + X_c) \right]
\]  

(3-74)

\( x_c \) is determined [8,24] by equating \( E_x \) given by Eq. (3-46) to \( E_c \),

\[
x_c = \frac{1}{m} - \frac{V_{DS}}{E_c \ln (1-mL)}
\]  

(3-75)

Combining Eqs. (3-72) up to (3-75) yields,

\[
J_{sn} = \frac{C_{ax} \mu_{ax} E_{ax} Z_o}{A d_o} \left[ 1 - \frac{\phi_B}{\epsilon_m} \exp \left[ -\left( \frac{\phi_B}{KT'} + \frac{d_o}{l_r} + \frac{\lambda}{l_{ox}} \right) \right] \right] \left[ \int_{X_c}^{L} (V_{GS} - V_T - V_x) (1-mx) dx \right]
\]

The solution of this equation yields [24]:

\[
J_{sn} = \frac{C_{ax} \mu_{ax} E_{ax} Z_o}{A d_o} \left[ 1 - \frac{\phi_B}{\epsilon_m} \exp \left[ -\left( \frac{\phi_B}{KT'} + \frac{d_o}{l_r} + \frac{\lambda}{l_{ox}} \right) \right] \right] \left[ (V_{GS} - V_T) \left( L - X_c \right) - \frac{m}{2} \left( L^2 - X_c^2 \right) \right] - \int_{X_c}^{L} (1-mx) V_x dx
\]  

(3-76)

where \( V_x \) is the channel potential at position \( x \). It is given by Eq.(3-44a,b). Also, the integral of \( (1-mx) V_x dx \) between \( X_c \) and \( L \) is given by using the Newton's code quadrature formula [8,40]:
Combining Eqs. (3-74), (3-76) and (3-77), the hot carrier gate current density is calculated for different values of channel steepness, \( m \) in TG MOSFETs.

\[
\int_{x_c}^{L} (1-mx) V_x \, dx = (L-x_c) (1-mx_c) \left[ 19 \ln(1-mx_c) \right] \\
+ 75 \ln \left( 1 - \frac{m}{5} (L+4x_c) \right) + 50 \ln \left( 1 - \frac{m}{5} (2L+3x_c) \right) \\
+ 50 \ln \left( 1 - \frac{m}{5} (3L+2x_c) \right) + 75 \ln \left( 1 - \frac{m}{5} (4L+x_c) \right) \\
+ 19 \ln(1-mL)
\]  

(3-77)

3.5 STUDY AND MODELLING OF THE HOT CARRIER SUBSTRATE CURRENT

In this section the mechanism by which the hot-carrier substrate current \( I_b \) is created is explained, together with formulation of \( I_b \) in the different modes of MOSFET operation. Effects of this current on the threshold voltage instability and on the surface potential distribution are also investigated.

3.5.1 Modelling

In scaled-down MOSFETs, where the drain to source separation is reduced, the surface fields are increased and carrier heating takes place [17,37,89]. The energetic electrons (case of N-channel MOSFET) cause impact ionization and lead, therefore, to surface-carrier multiplication [10,36]. As shown in Fig.(3-8), the generated electrons are accelerated by the longitudinal-field component \( E_x \) towards the drain and contribute to the MOSFET drain current \( I_{DS} \). The generated holes are accelerated by the transversal-field component \( E_y \) towards the substrate where they are collected and constitute the substrate current \( I_b \). This current is formulated in four different modes of operation as follows [8]:
Fig (3-8)
Surface carrier multiplication.
Mode 1: $V_{GS} > V_T, V_C > V_{DS} > V_{DSS}$

In this mode the MOSFET is biased into its saturation region ($V_{DS} > V_{DSS}$) with its drain to source voltage $V_{DS}$ kept smaller than a certain critical value $V_C$ (at which-channel-carrier multiplication begins, $V_C \approx 4V/\mu m$). In this case carrier multiplication occurs only in the pinch-off region and the substrate $I_B$ is given by:

$$I_B = A V_{DSS}^{2/3} \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{1/2} \left[ \exp (\alpha \Delta \ell) - 1 \right]$$  \hspace{1cm} (3-78)

Mode 2: $V_{GS} > V_T, V_{DSS} > V_{DS} > V_C$

The MOSFET is biased into its ohmic region ($V_{DS} < V_{DSS}$). With $V_{DS} > V_C$ carrier multiplication occurs only in the channel and $I_B$ is formulated by:

$$I_B = B V_{DS}^{1/2} \left( V_{DSS} - \frac{V_{DS}}{2} \right) \left[ \exp (\alpha L) - 1 \right]$$  \hspace{1cm} (3-79)

Mode 3: $V_{GS} > V_T, V_{DS} > V_{DSS} > V_C$

Here carrier multiplication occurs simultaneously in the pinch-off and the channel regions. $I_B$ is given in this case by:

$$I_B = I_B \text{ (mode: 1)} + I_B \text{ (mode: 2)}$$  \hspace{1cm} (3-80)

Mode 4: $V_{GS} < V_T$ or $V_{GS} > V_T, V_C > V_{DSS} > V_{DS}$

In this case no carrier multiplication takes place and $I_B$ is null,

$$I_B = 0$$  \hspace{1cm} (3-81)

with $V_{DSS}$ the drain saturation voltage.

$\Delta \ell$ the pinch-off region length given by Eq. (3-54-e)

$\alpha$ - the multiplication factor (see Ref:[1])

$A, B$ are constants depending on the device geometry.

They are given by [8]:
\[ A = \frac{Z C_{ox} \mu_o \gamma E_c^{1/2} K_b^{3/2}}{w_d L \left( 1 + \frac{L_D}{L} \right)^2} \sqrt{1 + \left( \frac{w_d}{L} \right)^2} \]  

(3-82)

\[ B = \frac{2 C_{ox} \mu_o \gamma E_c^{1/2} Z L}{w_d \left[ 1 + \theta_G \left( V_{GS} + \frac{V_{DS}}{2} \right) \right] \left( 1 + \frac{L_D}{L} \right)^2} \sqrt{1 + \left( \frac{w_d}{L} \right)^2} \]  

(3-83)

and

- \( L_D \) the drain width.
- \( w_d \) depletion layer depth.
- \( \gamma \) constant accounting for the surface-recombination effect.
- \( E_c \) the critical field at which mobility degradation begins.
- \( C_{ox} \) the oxide capacitance per unit surface area.
- \( \mu_o \) the channel mobility.
- \( K_b = k' \) constant given from equation (3-39).

3.5.2 Effects of \( I_B \) on the TG MOSFET Operation and Performance

The hot carrier substrate current \( I_B \) is one of the most important effects of the carrier heating phenomenon in short channel devices. \( I_B \) is shown to shift the device threshold voltage and degrade its stability. It also affects the surface potential, the surface-carrier distribution and the channel depth, which leads to important variations in the device performance [8,15]. Precise modelling and evaluation of the hot-carrier substrate current and the resulting threshold voltage shift and instability is, therefore,
seen to become extremely important for the proper design of the VLSI circuits and the accurate prediction of their operation and performance. Although much work and several studies have been done to characterize the carrier heating phenomena and the related effects on device parameters and circuit performance [17,23,82], no important effort has been given to the phenomena presented in this section.

a) Back-Bias Effect

The flow of the substrate current $I_B$ through the substrate resistance $R_B$ causes an $I_B R_B$ voltage drop $\Delta V_B$ which we call the back-bias voltage. This voltage elevates the potential of the depletion layer bottom over the value expected to be maintained in the absence of the substrate current. If $I_B$ is so large that the $I_B R_B$ product exceeds a certain critical limit (~0.6V), the source-substrate junction will be forward biased and inject more electrons into the depletion zone which enhances the carrier multiplication. This latter process causes $I_B$ and $\Delta V_B$ to be, regeneratively, increased through a positive feedback loop and may lead to source to substrate breakdown [10,36]. The back-bias voltage $\Delta V_B$ tends also to decrease the surface potential $\phi_s$ and increase the channel depth $d_o$ via modifying the surface carrier distribution [8,23]. It also shifts down the device threshold voltage and makes it unstable.

b) Formulation of the Back-Bias Voltage

The formulation of $\Delta V_B$ necessitates modelling of the substrate resistance $R_B$. As shown in Fig.(3-8), $R_B$ is the resistance of a certain substrate region lying below the channel and has a length $H$; the substrate thickness (given that the depletion layer width $W_d$ is negligibly smaller compared to $H$) and a cross section $A(y)$ which is variable with position $y$ measured from the Si-$SiO_2$ interface. $A(y)$ is seen to increase as going forward to the substrate bottom. This, in fact, is caused by the diffusion force created at the edge of the substrate current stream owing to the transversal hole concentration gradient [1]. This force spreads out the hole streams, which makes the cross-section of $R_B$ increase with distance $y$ and leads to a smaller value for $R_B$. The simple one-dimensional diffusion process of holes can be given by:
\[
\frac{\partial P(x,t)}{\partial t} = D_p \frac{\partial^2 P(x,t)}{\partial x^2}
\]  \hspace{1cm} (3-84)

with

\[
t = \frac{y}{\mu_p E_y}
\]  \hspace{1cm} (3-85)

With the condition of constant hole flux and total amount of hole charge \(Q_p\), the solution of Eq. (3-84) is given by the Gaussian function [51]:

\[
P(x,t) = \frac{Q_p}{\sqrt{\pi D_p t}} \exp \left( -\frac{x^2}{4D_p t} \right)
\]  \hspace{1cm} (3-86)

The adopted criterion does not consider the zones surrounding the hole flux where \(P(x,t)\) drops by 90%. With \(\mu_p = 500 \text{ cm}^2/\text{V.s}\), \(D_p = 12.5 \text{ cm}^2/\text{sec}\) and \(H = 300 \mu\text{m}\) the distance of deviation \(\Delta x\) is seen to be equal to 4.68 \(\mu\text{m}\), which is much smaller than \(H\). Therefore we can consider that the cross section \(A(y)\) varies linearly with \(y\) without fear of any important error [8],

\[
R_B = \frac{\rho}{ZL} \int_0^H dy \frac{dy}{(1 + \beta y)}
\]  \hspace{1cm} (3-87-a)

with \(\rho\) the substrate resistivity and

\[
\beta = \frac{2\Delta x}{HL}
\]  \hspace{1cm} (3-87-b)

The solution of this equation yields [8],

\[
R_B = \frac{\rho H}{ZL} \left[ \frac{L}{2\Delta x} \ln \left( 1 + \frac{2\Delta x}{L} \right) \right]
\]  \hspace{1cm} (3-88)

The term between great brackets represents the reduction in \(R_B\) value caused by the divergence of the \(I_B\) current streams. Calculations showed that \(R_B\) is reduced to 32.1% of its expected value. Equation (3-88) shows also that the value of \(R_B\) is dependent on the device geometry and the technology of fabrication. Combining Eqs. (3-78) and (3-88), we can evaluate and study the back-bias voltage \(\Delta V_B\),

\[
\Delta V_B = \frac{\rho H}{ZL} \left[ \frac{L}{2\Delta x} \ln \left( 1 + \frac{2\Delta x}{L} \right) \right] I_B
\]  \hspace{1cm} (3-89)
c) Surface Potential Evolution Caused Due to $\Delta V_B$

The back-bias voltage $\Delta V_B$ subtracts, as shown in Fig.(3-9), from the surface potential $\phi_s$, and modifies the surface potential $\phi(y)$. The new formulas are:

$$\phi_s = V_{DS} + 2\phi_p - \Delta V_B$$  \hspace{1cm} (3-90)

and

$$\phi(y) = \phi_s \left(1 - \frac{y}{w}\right)^2$$  \hspace{1cm} (3-91)

As shown in Fig.(3-9), the energy level $e_c$, $e_v$ of the conduction and valence bands at the Si–SiO$_2$ interface are not changed. Then the difference in energy between the new distribution and the old one (in absence of $I_B$) is given as:

$$\Delta \phi(y) = \Delta V_B \left[\left(1 - \frac{y}{w}\right)^2 - 1\right]$$  \hspace{1cm} (3-92)

d) Surface Carrier Distribution And Channel Depth

The solution of Poisson equation in the surface-space-charge region of a short channel MOSFET showed that the mobile carrier density $n(y)$ (in case of N-channel device) varies with distance $y$ according to the following Eq. [2,36]:

$$n(y) = n_{po} \exp[\beta (\phi(y) + \Delta \phi(y))]$$  \hspace{1cm} (3-93)

with $\phi(y)$ given by Eq. (3-91). Combining Eqs. (3-90) to (3-93), $n(y)$ is shown to be increased by $\Delta n(y)$ and acquires a new distribution $n^*(y)$ (see Fig.(3-10)) whose steepness is noticeably smaller than that of the distribution expected to be obtained in the absence of $I_B$.

$$n^*(y) = n(y) \exp[\beta \Delta \phi(y)]$$  \hspace{1cm} (3-94-a)

Substituting from Eq.(3-92),

$$n^*(y) = n(y) \exp[\beta \Delta V_B \left(1 - \frac{y}{w}\right)^2 - 1)\right]$$  \hspace{1cm} (3-94-b)

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Ignoring $\Delta V_B$

Considering $\Delta V_B$

**Fig (3-9)**
Back-bias effect on the MOSFET energy band structure

**Fig (3-10)**
Back-bias effect on the mobile carrier distribution $n(y)$
Referring to Fig. (3-10), one can expect that the channel depth $d_0$ (the distance $y$, measured from the Si-SiO$_2$ interface, at which $n(y)$ decreases to 10% of its value at the surface $n(0)$) will be increased [23,26].

e) Threshold Voltage Shift and Instability

The threshold voltage $V_T$ may be shifted due to many processes occurring in short channel MOSFETs [1,36,37,82]. Creation of new interface states at the Si–SiO$_2$ interface, injection and trapping of hot carriers into the oxide layer, and change of the depletion region width through application of substrate voltage are examples of these processes. This shift may be permanent or temporary according to the conditions under which the device is operated or examined [24,36]. If the process causes the threshold to stocastically vary with time and depends on the device biasing conditions, the threshold voltage will be unstable. If the process causes the threshold to attain permanent change, the threshold is called to be shifted. A new mechanism based on the back-bias effect is presented in this section. Formulation of the threshold voltage $V_T$ under this mechanism yields [1,23],

$$V_T = V_{FB} + \phi_{MS} + 2\phi_p + \frac{Q_B^- + Q_{SS}^- + Q_{ox}^-}{C_{ox}} \quad (3-95)$$

with

$$Q_B = \sqrt{2qN_A \varepsilon_d \varepsilon_o \phi_s} \quad (3-96)$$

The creation of the back-bias voltage $\Delta V_B$ decreases the surface potential $\phi_s$ which reduces the depletion layer width $W_d$ and the immobile charge $Q_B$ accommodated within it. It shifts, therefore, down $V_T$. The threshold voltage shift $\Delta V_T$ is given by:

$$\Delta V_T = \frac{\sqrt{2qN_A \varepsilon_d \varepsilon_o}}{C_{ox}} \left(\sqrt{V_{DS} + 2\phi_p - \Delta V_B} - \sqrt{V_{DS} + 2\phi_p}\right) \quad (3-97)$$

Equation (3-97) shows that $\Delta V_T$ is negative and becomes more important when increasing the substrate current $I_B$ and/or decreasing the device geometry. Since $I_B$ is sensitive to the device geometry, biasing and operating temperature which are all variable parameters, then $V_T$ will acquire a non-negligible instability.
3.6 MODELLING OF THE CHANNEL DEPTH

In section 3.3.3, equation 3-37 can be written as:

\[ d_0 = \left[ \frac{4 \varepsilon_{ox}}{9 \varepsilon_{sl} h_o L} \right] \frac{\Delta l^3}{\left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^2} \] (3-98)

where

- \( d_0 \) is the Channel Depth
- \( \varepsilon_{ox} \) is the Oxide Dielectric Constant
- \( \varepsilon_{sl} \) is the Silicon Dielectric Constant
- \( h_o \) is the oxide thickness (450Å)
- \( L \) is the Channel Length
- \( \Delta l \) is the pinch-off region
- \( V_{DS} \) is the Drain to Source Voltage.
- \( V_{DSS} \) is the saturation Drain to Source Voltage.

Therefore, to measure \( d_o \), it is necessary to know \( \Delta l \). In the following, a new model measuring \( \Delta l \) based on the hot Carrier Gate Current is presented.

When the MOSFET channel is switched by a strong electric field \( E_x \), the mobile carriers electrons in this case are accelerated and gain energy. These carriers emit some of their energy into the crystal through carrier lattice collisions. When the channel field is so strong that the energy gain is greater than that lost in collision, carrier and crystal heating take place. The hot carrier jumps over the Si-SiO\(_2\) interface and penetrates into the SiO\(_2\) layer where they are accelerated by the normal oxide field towards the gate electrode and constitute the hot carrier gate current \( I'_{gn} \). This current increases as \( V_{DS} \) increases and/or \( V_{GS} \) decreases as shown in Fig. (3-11). However, \( I'_{gn} \) begins to decreases after attaining some peak value when increasing \( V_{DS} \) further (\( I_{gn} \) decreases to \( I''_{gn} \)). This behaviour can be explained as follows:

When \( V_{DS} \) exceeds its saturation value, \( V_{DSS} \), the injecting surface shrinks due to the channel pinch-off. Moreover, the highly energetic carrier exercise impact ionisation and cause carrier multiplication. The secondary electrons created in the pinch-off regions are pushed back into the substrate because the normal oxide \( E_{ox} \) reverses its polarity while the secondary holes injection into the SiO\(_2\) layer is favoured which constitutes the hot hole gate current \( I_{gh} \). This current subtracts from \( I'_{gn} \) and results in a smaller one, \( I''_{gn} \).
Fig (3-11)
Variation of $I_{gn}$ with $V_{DS}$ for different $V_{GS}$.

Fig (3-12)
Carrier multiplication effect.
The multiplication factor \( M_{ohm} \) corresponding to the ohmic part of the channel (see Fig.(3-12)) is given by:

\[
M = e^{\alpha L} - 1
\]  
(3-99)

The net value of the hot carrier gate current \( I''_{gn} \) (see Fig. 3-11) may be formulated by:

\[
I''_{gn} = I'_{gn} - I_{gp}
\]  
(3-100)

with \( I'_{gn} \) the hot electron gate current injection from the ohmic part of the channel and \( I_{gp} \) the hot hole current created due to the carrier multiplication in the pinch off region, it is given by:

\[
I_{gp} = \frac{\mu_{exp}}{\mu_{oxn}} \frac{\Delta l}{L} I_{gn} (e^{\alpha L} - 1)
\]  
(3-101)

Combining equations 3-99, 3-100 and 3-101 yields:

\[
\frac{I''_{gn}}{I_{gn}} = \frac{I'_{gn}}{I_{gn}} - \frac{I_{gp}}{I_{gn}}
\]  
(3-102)

or

\[
\frac{I''_{gn}}{I_{gn}} = \left(1 - \frac{\Delta l}{L}\right) - \frac{\mu_{exp}}{\mu_{oxn}} \frac{\Delta l}{L} (e^{\alpha L} - 1)
\]  
(3-103)

from which, the pinch off region length \( \Delta l \) is given by:

\[
\Delta l = \frac{L \left(1 - \frac{I''_{gn}}{I_{gn}}\right)}{1 + \frac{\mu_{exp}}{\mu_{oxn}} (e^{\alpha L} - 1)}
\]  
(3-104)

Equation 3-104 shows that \( \Delta l \) can be measured from measurements of \( I''_{gn} / I_{gn} \) ratio given that \( \mu_{oxn}, \mu_{oxn} \) and \( \alpha \) are specified.
PART 2: NOISE
3.7 NOISE SOURCES AND NEW TECHNIQUES OF NOISE REDUCTION

In this section, a novel topological technique is presented.

The idea of the proposed technique and the principle of operation are presented with modelling and analysis.

3.7.1 Study And Investigation Of MOSFET Noise Sources

The 1/f noise associated with the MOSFET channel has been given a lot of attention and several theories have been proposed to predict and characterize it. However, rather less attention has been given to the 1/f noise associated with the hot carrier gate-current in short channel MOSFETs. This is referred to the measurement difficulties due to the small level of this noise ($\sim 10^{-30} \, \text{V}^2 \, \text{Hz}$) and the limited sensitivity of the available instruments ($\sim 10^{-20} \, \text{V}^2 \, \text{Hz}$)\cite{40,83}.

The 1/f noise, associated with the MOSFET channel current, has been studied for weak and strong inversion by many authors\cite{25,46,84}. This has allowed the analysis and modelling of the noise behaviour and has revealed its dependence on the device geometry, biasing conditions and technology. Although measurements were not easy to carry out, the channel current noise level ($\sim 10^{-14} \, \text{V}^2 \, \text{Hz}$) was compatible with the measuring capabilities and sensitivities of the available measuring instruments\cite{35,72,81,82}. On the other hand, the hot-carrier gate-current noise is expected to be much smaller ($\sim 10^{-30} \, \text{V}^2 \, \text{Hz}$) which shifts it out of sensitivity of these instruments.
The central idea in this later work concerning the hot carrier gate current noise [40] was to:

a) Model the hot carrier gate current $I_s(V_{DS}, V_{GS})$.

b) Verify the proposed model by experimental measurements; with $V_{DS}$ and $V_{GS}$ the drain to source and gate to source voltages respectively.

c) Deduce the oxide transconductance $g_{max}$ of the test MOSFETs from these measurements.

d) Comparing its measured value with the analytical expression derived from the $I_s(V_{DS}, V_{GS})$ model to remove any disagreement in case it exists.

Then the equivalent input noise spectrum $S_{v_{gs}}$ is measured and its experimental results are used to determine and to specify the equivalent hot-carrier gate-current noise spectrum $S_{r}$ from the $g_{max}^2 S_{v_{gs}}$ product.

This work comprises an analytical modelling of the hot-carrier gate-current noise. The effects of the device biasing, geometry and technology are taken into account. As has been shown [40], the hot-carrier gate-current noise is a mix of $1/f$ and $1/f^n$ noise, with $n$ being a constant ($2 \geq n > 0.5$) whose value depends on the density and distribution of the oxide traps along the channel length and over the oxide thickness.

3.7.2 Topological Technique

The analysis and measurements show that the MOSFET channel current $I_{DS}$ is given by [88]:

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\[
I_{DS} = C_{ox} \mu \frac{Z}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad V_{DS} < V_{DSS} \quad (3-107-a)
\]

\[
I_{DS} = C_{ox} \mu \frac{Z}{L} \frac{V_{DSS}^2}{2} \quad V_{DS} \geq V_{DSS} \quad (3-107-b)
\]

and

\[
V_{DSS} = V_{GS} - V_T
\]  

(3-108)

where

- Cox is the oxide capacitance per unit area (\( \sim 8.85 \times 10^{-4} \) pF/\( \mu \text{m}^2 \) at 400 Å oxide thickness),
- \( \mu \) is the effective value of the channel mobility (\( \sim 600 \) cm\(^2\)/V.sec),
- \( Z, L \) are, respectively, the channel width and length, see Fig.(3-16).
- \( V_T \) is the threshold voltage (\( \sim 0.5 \) to 1.5 V).
- \( V_{GS}, V_{DS} \) are, respectively, the gate and drain biasing voltages.
- \( V_{DSS} \) is the value of the drain saturation voltage, over which \( I_{DS} \) saturates and becomes independent of the \( V_{DS} \) variations \( \left( \frac{dI_{DS}}{dV_{DS}} \right) = 0 \). As shown in Fig.(3-17).

The \( I_{DS} \) / \( V_{DS} \) characteristics comprise two zones of operation, the first is the ohmic zone (1) where \( I_{DS} \) increases proportionally with \( V_{DS} \) and small channel resistance \( r_{DS} \) is investigated. The second is the saturation zone (2), in which the channel is pinched off besides the drain due to the reversal of the direction of the transversal surface field \( E_y (L > x > L - \Delta \ell) \) occurring when \( V_{DS} \) exceeds the operating value of \( V_{GS} \). As shown in Fig.(3-16), the length \( \Delta \ell \) of the pinch-off region is determined by the distance, from the drain, at which \( E_y \) shrinks to zero. Precise analysis and modelling have been recently performed and showed that:

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Fig (3-16)
RG-MOSFET structure
Fig (3-17)
Traditional and precise current models of RG-MOSFET.
\[ \Delta \ell = \left[ \frac{9 \varepsilon_{si} d_o h_o L}{4 \varepsilon_{ox}} \right]^{\frac{1}{3}} \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{\frac{2}{3}} \]  

(3-109)  

where \( d_o \) is the channel depth (~100 to 160 Å)  
\( h_o \) is the oxide thickness (~450 to 1200 Å)  
\( \varepsilon_{si}, \varepsilon_{ox} \) are, respectively, the silicon and oxide dielectric constants (12 and 4).  

It is also shown that the expression of \( V_{DSS} \) in Eq.(3-108) should be developed to:  

\[ V_{DSS} = (V_{GS} - V_T) \left[ 1 - 4 \sqrt{\frac{\varepsilon_{si} d_o h_o}{4 \varepsilon_{ox} L^2}} \right] \]  

(3-110)  

Equations (3-109) and (3-110) show that \( \Delta \ell \) increases (which makes the ohmic channel length \( L_8 \) shrink back as shown in Fig.(3-16)) as \( V_{DS} \) increases and/or \( V_{GS} \) decreases and vice versa. This behaviour reveals that the effective channel length becomes \( L - \Delta \ell \) instead of \( L \) during the operation of MOSFET in saturation \( (V_{DS} > V_{DSS}) \). Eqs. (3-107-a,b) should therefore be modified to:  

\[ I_{DS} = C_{ox} \mu_o \frac{Z}{L} (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \]  

(3-111-a) \hspace{1cm} V_{DS} < V_{DSS}  

\[ I_{DS} = C_{ox} \mu_o \frac{Z}{L} \frac{V_{DSS}^2}{2 \left(1 - \frac{\Delta \ell}{L}\right)} \]  

(3-111-b) \hspace{1cm} V_{DS} \geq V_{DSS}  

These equations show that \( I_{DS} \) instead of being constant and independent of the \( V_{DS} \) variations during the device operation in the saturation region, increases as \( V_{DS} \) increases and vice versa. It is also shown that the transconductance \( g_m = \frac{dI_{DS}}{dV_{GS}} \) is increased by a factor of \( \left(1 + \frac{\Delta \ell}{L}\right) \). This factor increases as the channel length \( L \), decreases (by increasing the value of \( V_{DS} \) and/or decreasing the value of \( V_{GS} \))  

\[ g_m = C_{ox} \mu_o \frac{Z}{L} V_{DS} \]  

(3-112-a) \hspace{1cm} V_{DS} < V_{DSS}  

\[ g_m = C_{ox} \mu_o \frac{Z}{L} \frac{(V_{GS} - V_T)}{\left(1 - \frac{\Delta \ell}{L}\right)} \]  

(3-112-b) \hspace{1cm} V_{DS} \geq V_{DSS}
Equations (3-109), (3-110) and (3-111) show that the $V_{GS}$ fluctuations cause the channel length to fluctuate and create drain current fluctuations which are dealt with as a new MOSFET noise called the CLM noise. Since the interaction between the channel carriers, the oxide and surface traps (see Fig.(3-18)) through tunnelling is very sensitive to the value and polarity of $V_{GS}$, the $V_{GS}$ fluctuations will therefore also contribute to the thermal and $1/f$ noise [18,25,40,46,59,62]. To reduce these effects we should decrease the value of $g_m$ and compensate, in adaptive manner, the fluctuations caused due to the $\Delta \ell$ and $V_{GS}$ fluctuations.

The analysis of mathematical and experimental work in this chapter investigates a novel and original technique, based only on the device topography, making it possible to realize a MOSFET whose $g_m$ is smoothly free from any fluctuations and consequently, a noise-free MOSFET. This original device is constructed, as shown in Fig.(3-19), using a trapezoidal gate MOSFET (TG-MOSFET) whose gate has a trapezoidal form with its narrow width $Z_0$ beside the source and the wider width at the drain.

The principle of operation of the proposed TG-MOSFET is as follows: if the gate voltage at a certain instance fluctuates so as instantaneously to decrease $V_{GS}$, then according to Eqs. (3-109) and (3-111), the pinch-off region length $\Delta \ell$ increases and tends consequently to increase $I_{DS}$. In reference to Fig.(3-19), the increase of $\Delta \ell$ simultaneously causes the effective channel width $Z(x)$ to decrease and forces $I_{DS}$ instantaneously to decrease. If the sides steepness of the trapezoidal gate is so selected that the decrease of $I_{DS}$ resulting from narrowing $Z(x)$ is equal to its increase caused by the decrease of the channel length $L$, the current $I_{DS}$ will remain constant regardless of the $V_{GS}$ fluctuations. The same arguments are valid for the dependence of $I_{DS}$ on the $V_{DS}$ fluctuations.

Although the explained technique is very simple to construct and easy to realize, it seems to be a powerful and adaptable technique for the cancellation of MOSFET noise. The algorithm used to optimise the gate form and the device dimensions is presented below.
Fig (3-18)
Effect of the gate voltage on the electron-trap interaction.
Fig (3-19)
TG-MOSFET structure

Fig (3-20)
Higher order steepness (n>1) of TG-MOSFET gate sides
a) Modelling and analysis

The current-voltage characteristic equations of the proposed TG-MOSFET can be derived as follows: assuming that the effective channel depth $d_0$ is very small with respect to both the oxide thickness $h_0$ and the channel length $L$, then the channel current at any position $x$ is given by [6,88]:

$$I_x = \int_0^y qn(y) \mu(y) E_x Z_x \, dy$$

(3-113)

with $E_x$ and $Z_x$ being the longitudinal channel field and the channel width at position $x$ respectively. They can be formulated by:

$$E_x = -\frac{d\psi_x}{dx}$$

(3-114)

and

$$Z_x = z_0 \left(1 + \frac{2\beta x}{Z_0} \right)$$

(3-115)

where $\beta$ is the gate side steepness (see Fig.(3-19)), given by

$$\beta = \frac{Z_L - Z_0}{2L}$$

(3-116)

Combining Eqs.(3-115) and (3-116) yields

$$Z_x = z_0 (1 + mx)$$

(3-117-a)

and

$$m = \frac{Z_L - Z_0}{Z_0 L}$$

(3-117-b)

$n(y)$ and $\mu(y)$ are, respectively, the mobile-carrier density and mobility in the device surface at distance $y$ from the Si-SiO$_2$ interface. Substituting:

$$n(y) = \frac{C_{ox}}{\psi_y} (V_{gs} - V_x - V_T)$$

$$V_T = -\frac{Q_s + Q_{ss}}{C_{ox}}$$
\[ \mu = \frac{\int \gamma q_n(y) \, \mu(y) \, dy}{\int \gamma q_n(y) \, dy} \]

in Eq. (3-113) and combining with Eqs. (3-114) and (3-117) yields

\[ \frac{I_{dx}}{(1 + mx)} = C_{ox} \mu Z_0 (V_{GS} - V_T - V_x) \, dV_x \]  

By integrating Eq. (3-112) along the channel length \( L \)

\[ I_{DS} = \frac{mL}{\ln(1 + mL)} C_{ox} \mu Z_0 \frac{V_{DS}^2}{2} \left( \frac{V_{SS} - V_T}{V_{DS}} - \frac{V_{DS}^2}{2} \right) \quad , \quad V_{DS} < V_{DSS} \]  

(3-119-a)  

\[ I_{DS} = \frac{mL}{\ln[1 + mL(L - \Delta t) \ln]} C_{ox} \mu Z_0 \frac{V_{DSS}^2 (1 - \delta)}{2} \quad , \quad V_{DS} > V_{DSS} \]  

(3-119-b)  

\[ \delta = 4 \frac{\epsilon_{si} d_o h_o}{4 \epsilon_{ox} L^6} \Delta t \]  

(3-119-c)  

Comparing Eqs. (3-119-b) and (3-111-b) we observe the following serious implications:

1) The increase (or decrease) of \( I_{DS} \) caused by the reduction (or increase) of \( L \) is compensated by instantaneous and proportional decrease (or increase) of \( Z \) occurring due to the trapezoidal gate form.

2) The variation in \( I_{DS} \) owing to variations of \( \Delta t \) in the logarithmic term is compensated by instantaneous and proportional variations in the value of \( \delta \).

3) The transconductance \( g_{mr} \) is appreciably reduced, in the ohmic and saturation regions, below its value \( g_{mr} \) given by Eqs. (3-112,a,b).

\[ g_{mr} = \chi g_{mr} \quad , \quad V_{DS} < V_{DSS} \]  

(3-120-a)  

\[ g_{mr} = \chi (1 - \delta) g_{mr} \quad , \quad V_{DS} > V_{DSS} \]  

(3-120-b)  

\[ \chi = \frac{mL}{\ln(1 + mL)} \]  

(3-120-c)  

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in this case we expect to cancel completely the CLM noise and to minimise the thermal and 1/f noise by factor of $\chi^2$ [46,59,88,89,90].

From the above analysis, where the MOSFET gate is linearly steeped (the power $n$ of $x$ in Eq.(3-117-a) is 1), to take a trapezoidal form, appreciable performance improvement has been achieved. This encourages us to study and analyse a higher order ($n>1$) gate side steeping, similar to that shown in Fig.(3-20),

$$Z_x = Z_o (1 + mx^n) \quad (3-121-a)$$

$$m = \frac{Z_L - Z_o}{Z_o L^n} \quad (3-121-b)$$

Combining Eqs.(3-121) and (3-113) and following a similar mathematical analysis leads to a more complicated expressions for the channel current $I_{ds}$ and transconductance reduction-factor $\chi$.

$$I_{ds} = \sum_{k} \frac{(nk+n+1) L}{(1)^k(mL^n)^k(1+mL^n)} \cdot C_{ox} \mu_o \frac{Z_o^2}{L} \left[ \left( V_{gs} - V_t \right) V_{ds} - \frac{V_{ds}^2}{2} \right], V_{ds} < V_{dss} \quad (3-122-a)$$

$$I_{ds} = \sum_{k} \frac{(nk+n+1) L}{(1)^k(mL^n)^k(1+mL^n)} \cdot C_{ox} \mu_o \frac{V_{dss}^2 (1-\delta)}{2}, V_{ds} > V_{dss} \quad (3-122-b)$$

$$\chi = \frac{(nk+n+1) L}{(1)^k(mL^n)^k(1+mL^n)} \quad (3-122-c)$$

In this case the device performance has been further improved. The improvement becomes better with increasing the values of $n$. 

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PART 3: STRESSING
3.8 EFFECTS OF INTERFACE AND OXIDE STATES ON DEVICE PARAMETERS

Recent studies of MOSFET VLSI show that the channel mobility, the $1/f$ noise and the threshold voltage represent the most critical device parameters affecting the reliability and performance of MOSFET VLSI circuits and systems [8,30,91,92,93]. Instability and degradation of these parameters is found to be, principally, related to interface and oxide states activity and their distribution in energy [30,74,89,91]. This problem becomes bigger with decreasing the MOSFET geometry and/or the greater the device biasing voltages [2,3,30]. The surface states are those energy states existing within: the forbidden gap and which are introduced due to interruption of the periodic lattice structure at or near the Si-SiO$_2$ interface. The oxide structural defects correspond also to energy states which assist, but by a much smaller participation, to the activities of the surface and interface states [3,30]. This assistance becomes smaller the deeper these defects are located inside the oxide layer [30]. Among the anticipated mechanisms by which the periodicity of the lattice structure is interrupted are: a) breaking of the atomic bonds by exposure to x-ray radiation or due to hot-carrier bombardment occurring when high biasing voltages are used [2,3,8,30], b) formation of a large amount of dislocations strongly related to technology of wafer preparation and/or device fabrication, c) contamination of the oxide and/or the Si-SiO$_2$ interface by mobile ions or foreign atoms and d) the movement and migration of these defects and their enhancement by the hot-carrier caused crystal-heating [91,93,94].

Besides the high voltage, X-ray or UV irradiation may be used as a tool to change the interface and oxide structures and consequently introduce or repair the defects [24,73]. Since the quantum energy of X-ray ($\sim 20$ KeV) and UV ($\sim 10$ eV) is much greater than that of hot electrons ($\sim 4$ eV) [2,3], then we expect to introduce defects by X-ray during a certain stressing time ($\sim 20$ sec.) which is much shorter (4X10$^3$ times) than that needed to introduce the same defects when high voltage stressing (hot carriers) is used. That is why we will exploit X-ray and UV techniques. These tools may exercise creation or annealing of defects.

The threshold voltage shift is referred to carrier trapping inside the oxide and/or at the Si-SiO$_2$ interface [3,94]. The variation of the mobility and the $1/f$ noise are referred to exchange of charge between the inversion layer and the surface and/or the Si-SiO$_2$ interface states [30,68,74,91]. This latter process involves two important mechanisms: 1) tunnelling of charge carriers between these states and the inversion layer and 2) Hopping transitions of charge carriers between these states [30,32,68]. This process is much more sensitive to activation by temperature
and/or surface and oxide fields, than trapping. The channel mobility variations are very sensitive to the interface and oxide states, in particular the frequency \( \nu \), at which the charge trapping and liberation occur or to the trapping time constant \( \tau_t \) \((\tau_t = \frac{1}{\nu})\) [32]. To give a wide spectrum analysis of the channel mobility we will assume the existence of two distinct types of states: a) fast states and b) slow states. The existence of fast and slow states will be experimentally verified in chapters 4 and 5.

In what follows we overview the expected nature and kinetics of the fast and slow states followed by theoretical analysis and modeling of the device parameters in terms of these states.

3.8.1 Nature And Kinetics of the Fast And Slow States

The above argument leads to the fact that the traps correspond to two kinds of states:

1) Fast states: which exist at and near the Si-SiO\(_2\) interface. They are considered donors if they could be neutral or positive by donating electrons. The acceptors are those states which could be neutral or negative by accepting electrons. When a gate voltage is applied, the interface trap levels move up or down with the valence and conduction band edges while the quasi Fermi level remains fixed. A fast change of charge in these traps occurs when the corresponding states cross the Fermi level. These traps, are therefore, expected to have a short trapping time constant \( \tau_t \sim 10^{-4} \) sec at \( E_y = 200 \text{ V}/\mu\text{m} \) and \( y = 40\text{Å} \) inside the oxide from the Si-SiO\(_2\) interface with \( E_y \) being the surface normal field). This time constant gets shorter when going close to the Si-SiO\(_2\) interface and vice versa. These traps are also expected to be potential wells characterized by a low energy barrier which enable easier and faster re-excitation of the trapped carrier out of it. These features make them very sensitive and fast in response to variations of surface potential and therefore responsive, as will be shown latter on, to the variations of the channel mobility and the device \( 1/f \) noise [3,30,68,74].

2) Slow states: which exist inside the oxide layer far from the Si-SiO\(_2\) interface. They may be donors or acceptors characterized by a relatively much longer trapping time constant \( \tau_t \sim 10^{-7} \) sec at \( E_{ox} = 0 \text{ V}/\mu\text{m} \) and \( \tau_t = 1 \text{ sec} \) at \( E_{ox} = 50\text{V}/\mu\text{m} \) in dry SiO\(_2\)). They are expected to be potential wells characterized by a high energy barrier \( \sim 2\text{eV} \), and for this reason are neither sensitive nor fast in response to the variations of the oxide field or the surface potential. These features make the slow states to be responsive to the threshold voltage shift with small secondary effect on the channel mobility [8,32,68,95].
3.8.2 Modelling of the Device Parameters

This section comprises modelling of the device parameters $\Delta V_T$, $\mu$ and $\mu_n$.

a) The Threshold Voltage Shift $\Delta V_T$

Straight forward analysis of the MOSFET showed that the threshold voltage $V_T$ is given by [2,8,68]:

$$ V_T = \Phi_{NS} + \phi_s + \frac{Q_b + Q_{ss} + Q_{ox}}{C_{ox}} \quad (3-123) $$

where

- $\Phi_{NS}$ is the substrate to gate-electrode work-function difference.
- $\phi_s$ is the surface potential.
- $Q_b$ is the depletion layer immobile charge (negative in n-channel MOSFETs and vice versa).
- $Q_{ss}$ is the surface state charge (always positive).
- $Q_{ox}$ is the oxide charge (negative in n-channel MOSFETs and vice versa).
- $C_{ox}$ is the oxide layer capacitance.

The variation of $V_T$ is caused due to variation of $Q_{ss}$ and $Q_{ox}$ resulting from trapping or detrapping of electrons (case of n-channel) by the surface (fast and slow states) and the oxide (slow states) defects. The threshold voltage shift $\Delta V_T$ can, therefore, be formulated by:

$$ \Delta V_T = \frac{q}{C_{ox}} \left( \Delta N_{ss} + \frac{\Delta N_{ox}}{2} \right) \quad (3-124) $$

where

- $q$ is the electron charge.
- $\Delta N_{ss}$ is the surface state (fast and slow) density.
- $\Delta N_{ox}$ is the oxide state (slow) density.

The formulation of $\Delta N_{ss}$ and $\Delta N_{ox}$ proceeds as follows: the rate at which electrons are captured by the positive interface states $\frac{dN}{dt}$ is proportional to the available number of positive states ($N_{ss} - N$), the electron flux across the interface $\frac{J}{q}$ and the capture cross section...
\[ \frac{dN}{dt} = \sigma_s \frac{J}{q} \left( N_{sg}^* - N \right) - \frac{1}{\tau_{an}} N \]  

(3-125)

The second term in Eq. (3-125) is the rate of disappearance by annealing of the surface defects with annealing time constant \( \tau_{an} \). The solution of this equation (assuming that \( N = 0 \) at \( t = 0 \)) yields

\[ N(t) = N_{ss}^* \left[ 1 - \exp \left( -\frac{t}{\tau_{cs}} \right) \right] \]  

(3-126)

with \( \tau_{cs} \) is the capture time-constant of electrons by surface defects \( \left( \tau_{cs} = \frac{q}{\sigma_s J} \right) \).

It should be pointed out that \( \tau_{cs} \) of fast states is much shorter than that of slow states and both are much shorter than \( \tau_{an} \). The same is true with respect to \( N_{ox} \). Also \( \tau_{cs} \) represents the effective capture time constant of the fast and slow surface states only if global effect is considered [68]. The fraction \( N_{ox}^- \) of the oxide states (slow states) that will be negatively charged, owing to electron capturing, can be evaluated using a similar procedure,

\[ N_{ox}^- = N_{ox} \left[ 1 - \exp \left( -\frac{t}{\tau_{co}} \right) \right] \]  

(3-127)

where

\[ N_{ss}^* = N_{ssm}^* \left[ 1 - \exp \left( -\frac{t}{\tau_{ts}} \right) \right] \]  

(3-128-a)

and

\[ N_{ox} = N_{oxm} \left[ 1 - \exp \left( -\frac{t}{\tau_{fo}} \right) \right] \]  

(3-128-b)
with \( \tau_{co} \) being the capture time constant of electrons by oxide defects. As will be shown below, \( \tau_{co} \) is much longer than \( \tau_{cs} \cdot \tau_{fs} \) and \( \tau_{fo} \) are the formation time constant of defects at the Si-SiO\(_2\) interface and oxide respectively. Combining Eqs. (3-124), (3-126) and (3-127), we can evaluate the threshold simultaneous shift and excursion owing to the slow and fast states respectively. It was believed from the former publication that the oxide and interface slow and fast states cause only permanent threshold shift \([68]\) which is not consistent with the explained nature and kinetics of the fast states.

\[
\Delta V_T(t) = \frac{eN_{ss}c}{C_{ox}} \left[ 1 - \exp \left( -\frac{C_{ss}}{\tau_{cs}} \right) + \frac{eN_{ox}c}{2C_{ox}} \left[ 1 - \exp \left( -\frac{C_{ox}}{\tau_{co}} \right) \right] \right]
\]  

(3-129)

Equation 3-129 shows that \( V_T \) increases with \( t \) and saturates at an upper limit \( V_{Tm} \) corresponding to the maximum value of the surface state density \( N_{ssm} \) \( (N_{ssm} = N_{fs} + N_{st}) \) as shown in Fig. (3-21).

b) The Effective Channel Mobility \( \mu_{eff} \)

The increase in mobility by stressing can be explained and evaluated as follows: we assume that \( Q_{ss} \) and \( Q_{ox} \) in Eq. (3-123) can be classified into slow states \( Q_{ss} \) and fast states \( Q_{fs} \) and reclassify \( Q_{ox} \) into positively and negatively charged states \( Q_{ox}^+ \) and \( Q_{ox}^- \), then equation (3-123) is developed to:

\[
V_T = \phi_{ns} + \phi_s + \frac{1}{C_{ox}} \left( Q_{ox} + Q_{ss} + Q_{fs}^+ + Q_{fs}^- \right)
\]  

(3-130)

and \( V_{gs} \) at any inversion level is, therefore given by

\[
V_{gs} = V_T + \frac{Q_n}{C_{ox}}
\]  

(3-131)

with \( Q_n \) being the mobile-charge density (electrons in case of N-channel MOSFET). It can be expressed in terms of the surface potential \( \phi_s \), by \([3,30,68,98]\):

\[
Q_n = Q_{no} \exp \left( \frac{e\phi_s}{2kT} \right)
\]  

(3-132)
Fig (3-21)
Variation of threshold voltage with stressing time.
Figure (3-22) shows the dependence of $\Phi_s$ on the MOSFET biasing voltages and on the slow and fast states activities. Referring to the $I/V$ MOSFET model, the unstressed channel mobility $\mu_0$ can be formulated by [2,3,68]:

$$\mu_0 = \frac{dI_{DS}}{dV_{GS}} / C_{ox} \frac{Z}{L} V_{DS}$$  \hspace{1cm} (3-133)

with $I_{DS}$ is the channel current, $V_{GS}, V_{DS}$ are respectively the gate and drain biasing voltages, and $Z, L$ are respectively the channel width and length.

$$I_{DS} = C_{ox} \mu_0 \frac{Z}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$  \hspace{1cm} (3-134)

Assuming that $Q^*_s$ and $Q^*_s$ are varying with $\Phi_s$ (refer to Eq. (3-132)) which varies in turn with $V_{GS}$ (see Fig.(3-22)), then by substitution from Eqs. (3-130) and (3-134) into Eq. (3-133) we obtain

$$\mu_0 = \frac{\mu_{eff}}{1 + \frac{2kT}{qQ_c} \left[ 1 + \frac{1}{C_{ox}} \frac{d}{d\Phi_s} (Q^*_s + Q^*_s) \right]}$$  \hspace{1cm} (3-135)

At strong inversion ($Q_c > 10^{11}/cm^2$, equation (3-135) develops to:

$$\mu_0 = \frac{\mu_{eff}}{1 + \frac{2kT}{qQ_c} \cdot \frac{d}{d\Phi_s} (Q^*_s + Q^*_s)}$$  \hspace{1cm} (3-136)

with $\mu_{eff}$ is the effective mobility.

As a result of stressing, new fast and slow states are introduced. Also the originally existing states are redistributed, which varies $Q^*_s$ and $Q^*_s$ and their response of variation with $\Phi_s$ and leads consequently to a new stressed mobility $\mu_{st}$, which can be expressed as:
Variation of the surface potential $\phi_s$ with the interface trap density.
This model has been used by reference [68] to study the dependence of $\mu$ on the variation of the density and distribution of the fast states caused by high voltage stressing. However, it does not depend on the mechanism by which fast states are created or distributed [24]. Therefore, the attention here is focused on stressing by X-ray and UV and introduce, for reasons of correlation studies, some data related to stressing by high voltage operation, while adding new data about the dependence of noise level on the high voltage stressing.

Equation 3-137 shows that $\mu_n$ increases as the fast state density decreases and vice versa. Assuming defect creation and annealing proceed with the stressing time $t_s$ as shown in Fig. (3-23), $\mu_n$ increases first with $t_s$ till a certain peak value. Afterwards, $\mu_n$ decreases with $t_s$ till it saturates at a certain limit where it becomes constant and independent of $t_s$.

c) The $1/f$ Noise $\varepsilon_{n,st}$

The $1/f$ noise, associating the channel and oxide activities in MOSFETs has been studied by many authors [30,74,75,91]. This allowed us to analyze and model the noise behavior and derive its dependence on the device geometry, biasing conditions and technology of fabrication. It also showed that the most serious noise to be observed in MOSFETs and used to qualify successfully the level of its performance, is the $1/f$ noise. This noise originates from interaction between fast surface states, existing at and near the Si-SiO$_2$ interface, and the mobile channel-carriers. The corresponding drain and gate currents frequency spectrums $S_{I_d}$ and $S_{I_g}$ are given respectively by [30,76]:

$$S_{I_d} = \frac{q^2 Z\mu_0^2}{f L^2 E_c} \int_0^L \frac{N_{f_s}(E_{F,s})}{1 + \left(\frac{dV_x}{dx}/E_c\right)^2} \cdot \frac{dV_x}{dx} dV_x$$

(3-138-a)
\[ S_{tg} = \int_0^{V_{gs}} \int_0^L K \left[ \frac{N_{fa} \tau_{cs}}{\alpha} \left( \frac{\Delta h_{ox}}{2} \ln \frac{1 + \omega^2 \tau_{cs}^2 \varepsilon_{ox}^2}{1 + \omega^2 \tau_{cs}^2} \right) \right] Z dV_x dx \]

\[ + \frac{N_{fa}}{\alpha \omega} \left( \tan^{-1} \omega \tau_{cs} e^{\alpha h_{ox}} - \tan^{-1} \omega \tau_{cs} \right) \]  

with

\[ K = 4 \Delta f \left[ \frac{I_g q^2}{k T_c Z L (C_D + C_{ox} + C_n)} \sqrt{\frac{q^3 \varepsilon_{si}^2}{4 \pi \varepsilon_{ox} W_D E_{ox}}} \right] f_c f_{nt} \]

where

\( C_D, C_n \) are the depletion layer and channel capacitances respectively.

\( W_D \) is the depletion layer width.

\( \varepsilon_{si}, \varepsilon_{ox} \) are the silicon and oxide dielectric constants respectively.

\( I_g \) is the hot carrier gate current.

\( \alpha \) is a trapping constant \((-10^9/cm)\) [76]

References [30 and 76] assumed that all the interface and oxide states participate to the noise generation. They also provided no evidence about the variation of the noise level with stressing. On the contrary, two types of traps, fast and slow, have been distinguished. It has been shown that the first is the active partner and that stressing by any means first anneals some fast states and introduces thereafter fast and slow states which establish a global fast state generation rate like that shown in Figure (3-23).

Figure (3-24) shows the expected variation of the \(1/f\) noise with \(t_n\) in terms of variations of the fast states due to annealing and creation processes.

3.8.3 UV Annealing: Theory and Modelling

The UV (as shown in Fig.(3-25))exercises two effects on the MOSFET oxide [100-103]

1) Annealing of the available broken bonds.
Fig (3-25)
Dual stressing/annealing effect of U.V on the MOSFET oxide.

Fig (3-26)
Variation of the annealing rate $N(t)$ with time at different values of irradiation intensity $I_r$. 
GLOBAL F.S.

CREATION F.S.
and S.S.

ANNEALING F.S.

\[ t_{st} \]

\[ \frac{dQ_{ts}}{d\phi_s} \]

Fig (3-23)
Global fast state generation rate.

Fig (3-24)
Expected variation of the 1/f noise with \( t_{st} \) in term of variations of the fast state due to annealing and creation processes.
2) Creation of new types of defects through breaking, dangling bond and/or dissociation of new bonds.

1) Annealing

Assume UV radiation intensity $I_x$ with photon energy $hv$ impinging a number of broken bonds $N$, the radiation capture cross section of each trap (or broken bond) is $\sigma_{ph}$, the annealing photon energy $hv$ should be greater than a certain threshold [100,101].

The rate of annealing of these broken bonds $\frac{dN}{dt}$ is proportional to the number of these broken bonds, the radiation capture cross section $\sigma_{ph}$, the radiation intensity $I_x$ and the photon energy $hv$. Since annealing tends to decrease $N$, then

$$\frac{dN}{dt} = -\sigma_{ph} \cdot \frac{I_x}{hv} N$$

Separation of variables yields

$$\frac{dN}{N} = -\frac{dt}{\tau_{ph}}$$

where

$$\tau_{ph} = \frac{1}{I_x \sigma_{ph}}$$

By integration with the following boundary conditions

$N$ varies from $N_o$ to $N$.

as $t$ varies from 0 to $t$

we obtain,

$$\ln \frac{N}{N_o} = -\frac{t}{\tau_{ph}}$$
\[ N = N_0 \exp - \frac{t}{\tau_{ph}} \]  

which shows that the number of traps (which is equal to the number of broken bonds) \( N \) decreases exponentially with time at a time constant \( \tau_{ph} \). Referring to equation (3-141) we see that \( \tau_{ph} \) decreases as the irradiation intensity \( I_r \) and/or the radiation capture cross section of the broken bond increase. Referring to Fig.(3-26), we state that the annealing rate is greater the higher the level of irradiation intensity \( I_r \) and/or the greater the energy capture cross section \( \sigma_{ph} \).

2) New Defect Creation

If the photon energy becomes appreciably greater than the bond critical energy, some new bonds will be broken. If the available number of bonds which are susceptible to being broken is \( N_{ox} \) and the number of new broken bonds is \( N \), the efficiency at which the bonds receive and accept the photon energy and break is \( \eta_b \) then the rate at which new broken bonds are created is given by:

\[ \frac{dN}{dt} = \eta_b \frac{N_{ox} - N}{I_r} h \nu \]  

(3-143)

by separation of variables

\[ \frac{dN}{N_{ox} - N} = \frac{t}{\tau_b} \]

which yields,

\[ \tau_b = \frac{1}{\eta_b I_r} \]  

(3-144)

Integrating Eq. (3-143) with the boundary conditions

\( N \) varies from 0 to \( N \)
\( t \) varies from 0 to \( t \)

yields

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\[ \ln \frac{N_{ox} - N}{N_{ox}} = - \frac{t}{\tau_b} \]

or

\[ N = N_{ox} \left(1 - \exp \left(-\frac{t}{\tau_b}\right) \right) \quad (3-145) \]

which shows that the number of traps introduced through breaking bonds due to U.V. irradiation increases exponentially with time at a time constant \( \tau_p \). Referring to Eq. (3-144) we see that \( \tau_b \) becomes shorter as the irradiation intensity \( I_x \) increases and/or the efficiency at which bonds receive the photon energy and break. In other words, a greater rate of defect generation is achieved (see Fig.(3-27)) at a higher level of irradiation and/or at greater efficiency of photon energy accumulation [102].

The global effect of UV is expected to be (see Fig.(3-28)) the sum of these two effects.

When the annealing rate is equal to the defect generation rate, \( N(t) \) attains a constant value as shown in Fig.(3-29) and saturates at a certain lower limit where it becomes independent of the radiation time \( t \).

The steady state value of \( N \) can therefore be deduced from equating the rate of annealing (disappearance of defect) and that of the creation (bonds breaking),

\[ \left. \frac{dN}{dt} \right|_{\text{ann}} = -\sigma_{ph} I_x N \quad \text{annealing} \quad (3-146-a) \]

\[ \left. \frac{dN}{dt} \right|_{\text{cre}} = \eta_b (N_{ox} - N) I_x \quad \text{creation} \quad (3-146-b) \]

\[ \left. \frac{dN}{dt} \right|_{\text{cre}} - \left. \frac{dN}{dt} \right|_{\text{ann}} = 0 \quad (3-146-c) \]

Straight forward analysis yield
Fig (3-27)
Variation of the rate of defect creation with time $t$ at different values of irradiation intensities $I_r$.

Fig (3-28)
The global effect of UV on the defect creation rate.
Fig (3-29)
Global effect of UV intensity on the defect creation rate.
From these equations we conclude that:

1) Annealing proceeds faster at the greater value of $I_r$ and $\sigma_{ph}$.
2) New defect generation proceeds faster when $\eta_b$ and $I_r$ are increased.
3) The steady state value of $N$ becomes greater the greater the value of $N_{ox}$ and $\eta_b$.

3.8.4 Modification by UV Irradiation of the MOSFET Parameters

The study of this chapter shows that the x-ray irradiation will introduce new defects at the Si-SiO$_2$ interface and inside the oxide layer through breaking: dangling bonds or dissociation of new bonds. This phenomena becomes more pronounced the shorter the channel length and/or the thinner the oxide layer.

It has also been shown, through analysis, that the UV irradiation has two contradictory effects depending on the radiation wavelength $\lambda$ and the beam intensity $I_r$:

a) It may reduce the defects densities at the Si-SiO$_2$ interface and inside the oxide through the annealing process. In this case the crystal lattice is "heated up" by the UV irradiation (phonon process) which excites the particular defects and provides a chance for the broken bonds to reconstruct and/or displace, and for excited atoms to release any excess energy and relax to their original position in the spatial lattice.

b) It may create new defects through breaking new bonds and displacing new atoms from their equilibrium positions.

We can therefore employ the x-ray irradiation and/or the high voltage operation to increase the defects densities (fast and slow states) which tend to increase the threshold voltage $V_T$ (through increasing the slow state density). We can, on the other hand, employ the UV irradiation to anneal these defects and redecree, consequently, $V_T$. However, the two tools may be used simultaneously to control and smooth up $V_T$. This services in:
1) Controlling and smoothing up the channel conductivity and mobility.
2) It enables the cancellation of the channel voltage and current excursions which lead to an improved device signal to noise ratio.
3) In digital application where a wide margin between logical "0" and "1" is requested we can modify the value of $V_T$ so as to fulfil this requirement.
4) Since the UV irradiation has the ability to anneal (remove) band gap levels, we expect the UV irradiation to play a very important part in the noise reduction and mobility smoothing.
5) In some special applications requesting high mobility (Hall effect in MOSFET) we can select $\lambda$ so that the energy of the UV irradiation increases, to some specific degree, the fast state density so as to obtain the maximum possible channel mobility.
PART 4: MAGNETIC PROPERTIES
3.9 STUDY AND INVESTIGATION OF THE HALL VOLTAGE AND MAGNETORESISTANCE IN VLSI MOSFETs

The Hall effect in Si MOSFET devices (Rectangular and trapezoidal formed gate MOSFETS) are studied and investigated for the following case: the low level injection or the injected current $I_x$ is not too high so that the created excess hole or electron densities $\Delta p(y)$ and $\Delta n(y)$ remain appreciably smaller than the majority hole and electron densities $p$ and $n$ respectively, (i.e. $\Delta p < p$, $\Delta n < n$).

This work is focused on n-channel MOSFETs (supplied by Thompson Microelectronics).

For the characterisation of the MOSFET magnetic properties one needs direct measurements of the Hall and magnetoresistance effects which are manifested as channel lateral voltage or the evolution of the longitudinal channel current. The second one can be directly measured in MOSFET while the first one cannot be measured due to the absence of the lateral contacts. To understand the implications of this problem we used thin film to study these effects and quantify the expected limitations.

The modelling in this section will consider several side effects which have not been studied or considered elsewhere:

a) Edge defects and recombination.
b) Magnetoresistance.
c) Relative displacement of the Hall contacts.
d) Effects of the longitudinal current transients.
3.9.1 Theory and Modelling

As shown in Fig. (3-30) the current density \( J_x \) is taken in the positive X-direction and the magnetic field \( B_z \) is taken in the positive Z-direction, the charge separation will be produced in the negative Y-direction. This will produce an electric field \( E_y \) in the negative Y-direction, if the Hall contacts are left open circuited. In this case the field \( E_y \) builds up until there is no net current in the y-direction. It should be noted, however, that this does not mean that the current is everywhere zero, but only that the integration of the current \( J_y \) over the cross section is zero.

\[
\begin{align*}
\int (J_{py} + J_{ny}) \, dx &= 0 \\
E_y &= \text{const}
\end{align*}
\]  

(3-148)

If a long specimen is considered, then the end effects can be neglected and the current flow can be taken as parallel to the surface. Since this is not the case, then some carriers leave the stream even in the absence of the magnetic field and deviate up and down towards the thin film edges, and equal numbers of carriers (holes in case of p-type, electrons in case of n-type or both in case of intrinsic material) are accumulated at the upper and lower film edges. The electric field relating to this behaviour is zero and remains so as long as the disappearance of carriers in recombination is equal at both edges. In fact this may not be the case because the two Hall contacts may be displaced in the X-direction one with respect to the other. In our case these contacts may be represented by equivalent diodes \( D_1 \) and \( D_2 \) [6,73] at distances \( x_1 \) and \( x_2 \) from the left side end of the thin film. Straight forward analysis shows that these diodes are forward biased respectively by:
Fig (3-30)
Schematics of the charge accumulation by the Hall force in a-GaAs.
The currents \( I_{d1} \) and \( I_{d2} \) of these diodes cause disappearance of accumulated carriers at rates

\[
\begin{align*}
V_1 &= I_R x_1 = \rho J_x x_1 = \rho J_x \left( x - \frac{\Delta x}{2} \right) \\
V_2 &= I_R x_2 = \rho J_x x_2 = \rho J_x \left( x + \frac{\Delta x}{2} \right)
\end{align*}
\]

(3-149)

The currents \( I_{d1} \) and \( I_{d2} \) of these diodes cause disappearance of accumulated carriers at rates

\[
\begin{align*}
J_{d1} &= \left[ q n_i^2 \left( \frac{L_n}{N_A \tau_n} + \frac{L_p}{N_D \tau_p} \right) \exp \frac{\rho J_x x}{V_T} \right] \exp -\frac{\rho J_x \Delta x}{2 V_T} \\
J_{d2} &= \left[ q n_i^2 \left( \frac{L_n}{N_A \tau_n} + \frac{L_p}{N_D \tau_p} \right) \exp \frac{\rho J_x x}{V_T} \right] \exp \frac{\rho J_x \Delta x}{2 V_T}
\end{align*}
\]

(3-150)

With \( q \) being the electron charge, \( n_i \) the thermal equilibrium density of carriers, \( L_n \) and \( L_p \) the electron and hole diffusion lengths respectively, \( \tau_n \) and \( \tau_p \) the electron and hole lifetimes respectively, \( N_A \) and \( N_D \) the doping of the thin film and Hall contact material respectively, \( \rho \) the film resistivity, \( V_T = \frac{kT}{q} \) the thermal voltage, \( x \) the position of the Hall contacts and \( \Delta x \) the contacts displacement. Referring to Eq.(3-150) we observe that accumulated carriers at the lower end are drained at a rate which is greater than that which is sustained at the upper end. A different carrier accumulation is consequently established in the absence of the magnetic field \( (B = 0) \) which creates a carrier concentration gradient which participates to that caused by the Hall force and introduce therefore an additional field component in the same direction as \( E_y \), \([1,45]\).

In what follows we will study and evaluate the different phenomena which contribute positively or negatively to the Hall field and present a model which includes all these phenomena.
3.9.2 Limitations and Restrictions

Our measurements show, for the first time, several participating phenomena which can be categorized as follows:

1) Different accumulation rates of charge at the slab edges due to the two contacts displacement.
2) Charge separation by the magnetic field $B$.
3) Magnetoresistance caused due to non-zero transversal (magnetic) current.
4) Degradation of carrier mobility and conductance at strong biasing voltages or currents.
5) Effects of the film structure (single crystal, polycrystalline, Amorphous) and geometry.

3.9.3 Charge Accumulation in Absence of the Magnetic Field $B$

To evaluate the charge accumulation in the Y-direction, we should solve the continuity equation

$$\frac{dp}{dt} = G - R$$  \hspace{1cm} (3-151)

with $G$ being the generation rate given by $\frac{1}{q} \cdot \frac{\partial J_y}{\partial y}$ by \(G \) and $R$ is the recombination given by $\frac{\Delta p}{\tau_p}$ \([22,23,89]\). In the steady state Eq.(3-151) develops to:

$$\frac{1}{q} \cdot \frac{\partial J_y}{\partial y} - \frac{\Delta p}{\tau_p} = 0$$ \hspace{1cm} (3-152)

with the boundary conditions:

\[
\begin{align*}
J_y &= \left[ \frac{q n^2}{N_A \tau_n} \exp \left( \frac{\rho J_x}{2 V_T} \Delta x \right) \right] \exp \left( \frac{\rho J_x}{V_T} x \right) \quad y = 0 \\
J_y &= \left[ \frac{q n^2}{N_A \tau_n} \exp \left( \frac{\rho J_x}{2 V_T} \Delta x \right) \right] \exp \left( \frac{\rho J_x}{V_T} x \right) \quad y = \omega \end{align*}
\] \hspace{1cm} (3-153)
Now,

\[ J_{py} = q\mu_p E_y - qD_p \frac{\partial p}{\partial y} \]

\[ J_{ny} = qn\mu_n E_y + qD_n \frac{\partial n}{\partial y} \]

Since \( p = p_0 + \Delta p \) and \( n = n_0 + \Delta n \) and \( \Delta n = \Delta p \), then

\[
\begin{align*}
J_{py} &= q\mu_p E_y - qD_p \frac{\partial \Delta p}{\partial y} \\
J_{ny} &= qn\mu_n E_y + qD_n \frac{\partial \Delta p}{\partial y}
\end{align*}
\]

\[ J_y = J_{py} + J_{ny} \]

\[
J_y = q\mu_p (p+bn) E_y - qD_p (1-b) \frac{\partial \Delta p}{\partial y}
\]

Combining Eqs. (3-152) and (3-155) with \( E_y = \text{constant} \), yields

\[ D_p (b-1) \frac{\partial^2 \Delta p}{\partial y^2} - \frac{\Delta p}{\tau_p} = 0 \]

\[
\left( D^2 - \frac{1}{L^2} \right) \Delta p = 0
\]

with \( L^2 = \tau_p D_p (b-1) \), then

\[ \Delta p = A \exp \frac{Y}{L_p} + B \exp -\frac{Y}{L_p} \]

\[ \Delta p = A \exp \frac{Y}{L_p} + B \exp -\frac{Y}{L_p} \]

Combining Eqs. (3-153), (3-155) and (3-156), yields,

\[
\left[ \frac{q\mu_p L_p}{N\tau_n} \exp -\frac{\rho J_X \Delta x}{2V_T} \right] \exp \frac{\rho J_X x}{V_T} = q\mu_p (p+bn) E_y - qD_p (1-b) \left[ \frac{A}{L_p} - \frac{B}{L_p} \right]
\]

\[
\left[ \frac{q\mu_p L_p}{N\tau_n} \exp +\frac{\rho J_X \Delta x}{2V_T} \right] \exp \frac{\rho J_X x}{V_T} =
\]
\[ q \mu_p (p+bn) E_y - q D_p (1-b) \left[ \frac{A}{L_p} e^\frac{\omega}{L_p} - \frac{B}{L_p} e^{-\frac{\omega}{L_p}} \right] \]

\[ \chi \left( \exp -\alpha \Delta x + \frac{\omega}{L_p} - \exp \alpha \Delta x \right) = \]

\[ q \mu_p (p+bn) E_y \left( \exp \frac{\omega}{L_p} - 1 \right) - q D_p (1-b) \frac{A}{L_p} e^{-\frac{\omega}{L_p}} - e^{\frac{\omega}{L_p}} \]

which leads to:

\[ \chi e^{\frac{\omega}{2L_p}} \left( \exp -\alpha \Delta x + \frac{\omega}{2L_p} - \exp \alpha \Delta x - \frac{\omega}{2L_p} \right) = \]

\[ q \mu_p (p+bn) e^{\frac{\omega}{2L_p}} E_y \left( \exp \frac{\omega}{2L_p} - e^{-\frac{\omega}{2L_p}} \right) - q D_p (1-b) \frac{A}{L_p} e^{-\frac{\omega}{2L_p}} - e^{\frac{\omega}{2L_p}} \]

Then,

\[ \chi \left[ e^{-\left(\alpha \Delta x - \frac{\omega}{2L_p}\right)} - e^{\left(\alpha \Delta x - \frac{\omega}{2L_p}\right)} \right] = \beta E_y (e^{\frac{\omega}{2L_p}} - e^{-\frac{\omega}{2L_p}}) + \gamma B (e^{\frac{\omega}{L_p}} - e^{-\frac{\omega}{L_p}}) e^{-\frac{\omega}{2L_p}} \]
\[ \chi \left[ e^{-\left(\frac{\alpha \Delta x - \omega}{2L_p}\right)} - e^{\left(\frac{\alpha \Delta x + \omega}{2L_p}\right)} \right] = \beta E_y \left( e^{-\frac{\omega}{2L_p}} - e^{\frac{\omega}{2L_p}} \right) + \gamma A \left( e^{\frac{\omega}{L_p}} - e^{-\frac{\omega}{L_p}} \right) e^{\frac{\omega}{2L_p}} \]

with:

\[ \chi = \frac{q n^2 L^2}{N \tau_n} \exp 2\alpha x \]

\[ \alpha = \frac{p J_x}{2 \nu_r} \]

\[ \beta = q \mu_p (p + bn) \]

\[ \gamma = \frac{q D_p (1 - b)}{L_p} \]

\[ b = \frac{\mu_n}{\mu_p} \]

By substituting,

\[ \chi \text{Sinh} \left( \frac{\alpha \Delta x - \omega}{2L_p} \right) = -\beta E_y \text{Sinh} \frac{\omega}{2L_p} - \gamma B \text{Sinh} \frac{\omega}{L_p} \cdot e^{-\frac{\omega}{2L_p}} \]

\[ \chi \text{Sinh} \left( \frac{\alpha \Delta x + \omega}{2L_p} \right) = +\beta E_y \text{Sinh} \frac{\omega}{2L_p} - \gamma A \text{Sinh} \frac{\omega}{L_p} e^{\frac{\omega}{2L_p}} \]

From which the constants \( A \) and \( B \) are determined.
Combining Eqs. (3-156) and (3-157) yields:

\[
\Delta p = \frac{\beta E_y \sinh \left( \frac{\omega}{2L_p} \right) - \chi \sinh \left( \alpha \Delta x + \frac{\omega}{2L_p} \right)}{\gamma \sinh \frac{\omega}{L_p}} e^{-\frac{\omega}{2L_p}} \left\{ \frac{\chi}{L_p} - \frac{\omega}{2L_p} \right\} \]  

(3-158)

Combining Eqs. (3-158) and (3-155) yields:

\[
J_y = \beta E_y \left[ \frac{\beta E_y \sinh \left( \frac{\omega}{2L_p} \right) - \chi \sinh \left( \alpha \Delta x + \frac{\omega}{2L_p} \right)}{\sinh \frac{\omega}{L_p}} e^{-\frac{\omega}{2L_p}} \right] \left\{ \frac{\chi}{L_p} - \frac{\omega}{2L_p} \right\} \]  

\[
- \left[ \frac{\beta E_y \sinh \left( \frac{\omega}{2L_p} \right) + \chi \sinh \left( \alpha \Delta x - \frac{\omega}{2L_p} \right)}{\sinh \frac{\omega}{2L_p}} e^{-\frac{\omega}{2L_p}} \right] \left\{ -\frac{\chi}{L_p} + \frac{\omega}{2L_p} \right\} \]  

(3-159)
Equating $J_y = 0$ yields,

$$
E_y \left[ \beta - \frac{\beta \sinh \frac{\omega}{2L_p} e^{\frac{Y}{L_p} - \frac{\omega}{2L_p}} - \beta \sinh \frac{\omega}{2L_p} e^{-\frac{Y}{L_p} + \frac{\omega}{2L_p}}}{\sinh \frac{\omega}{L_p}} \right] = - \frac{\chi \sinh \left( \alpha \Delta x + \frac{\omega}{2L_p} \right) e^{\frac{Y}{L_p} - \frac{\omega}{2L_p}} - \chi \sinh \left( \alpha \Delta x - \frac{\omega}{2L_p} \right) e^{-\frac{Y}{L_p} + \frac{\omega}{2L_p}}}{\sinh \frac{\omega}{L_p}}
$$

From which:

$$
E_y = \frac{\chi \sinh \left( \alpha \Delta x + \frac{\omega}{2L_p} \right) e^{\frac{Y}{L_p} - \frac{\omega}{2L_p}} - \chi \sinh \left( \alpha \Delta x - \frac{\omega}{2L_p} \right) e^{-\frac{Y}{L_p} + \frac{\omega}{2L_p}}}{\beta \left[ \sinh \frac{\omega}{L_p} - \sinh \frac{\omega}{2L_p} \cdot e^{\frac{Y}{L_p} - \frac{\omega}{2L_p}} - \sinh \frac{\omega}{2L_p} \cdot e^{-\frac{Y}{L_p} + \frac{\omega}{2L_p}} \right]}
$$

$$
= \frac{2\chi \left[ -\sinh \alpha \Delta x \cosh \frac{\omega}{2L_p} \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) + \cosh \alpha \Delta x \sinh \frac{\omega}{2L_p} \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) \right]}{\beta \sinh \frac{\omega}{2L_p} \left[ 2 \cosh \frac{\omega}{2L_p} - \left( e^{\frac{Y}{L_p} - \frac{\omega}{2L_p}} - e^{-\frac{Y}{L_p} + \frac{\omega}{2L_p}} \right) \right]}
$$

$$
= \frac{2\chi \left[ -\sinh \alpha \Delta x \cosh \frac{\omega}{2L_p} \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) + \cosh \alpha \Delta x \sinh \frac{\omega}{2L_p} \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) \right]}{2 \beta \sinh \frac{\omega}{2L_p} \left[ \cosh \frac{\omega}{2L_p} - \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) \right]}
$$

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\[ E_y = \frac{2\chi \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right) \sinh \left( \frac{\omega}{2L_p} - \alpha \Delta x \right)}{\beta \left[ \sinh \frac{\omega}{L_p} - 2 \sinh \frac{\omega}{2L_p} \right] \sinh \left( \frac{Y}{L_p} - \frac{\omega}{2L_p} \right)} \]  

(3-160)

3.9.4 Charge Separation By the Magnetic Field B

Referring to Fig. (3-30), the X and Y current transport equations can be deduced,

\[ \begin{align*}
J_{px} &= q \mu_p E_x - qD_p \frac{\partial p}{\partial x} \\
J_{nx} &= q \mu_n E_x + qD_n \frac{\partial n}{\partial x}
\end{align*} \]  

(3-161)

\[ \begin{align*}
J_{py} &= q \mu_p E_y - qD_p \frac{\partial p}{\partial y} + \theta_p J_{px} \\
J_{ny} &= q \mu_n E_y + qD_n \frac{\partial n}{\partial y} - \theta_n J_{nx}
\end{align*} \]  

(3-162)

With \( \theta_p \) and \( \theta_n \) are respectively the Hall angles for holes and electrons \((\theta_p = \mu_p B_z, \theta_n = \mu_n B_z)\). Assuming no carrier concentration gradient occurs, i.e. \( \frac{\partial p}{\partial x} = 0 = \frac{\partial n}{\partial x}, \frac{\partial p}{\partial y} = 0 = \frac{\partial n}{\partial y} \), then Eqs. (3-161) and (3-162) develop to:

\[ \begin{align*}
J_{px} &= q \mu_p E_x \\
J_{nx} &= q \mu_n E_x
\end{align*} \]  

(3-163)

\[ \begin{align*}
J_{py} &= q \mu_p E_y + \mu_p B_z (q \mu_p E_x) = q \mu_p E_y + q \mu_p^2 B_z E_x \\
J_{ny} &= q \mu_n E_y - \mu_n B_z (q \mu_n E_x) = q \mu_n E_y - q \mu_n^2 B_z E_x
\end{align*} \]  

(3-164)
When keeping the Hall contacts open circuited, i.e. \( J_y = J_{ny} + J_{py} = 0 \), then

\[
q \nu_p E_y + q \nu_p^2 B_z E_x + q \nu_n E_y - q \nu_n^2 B_z E_x = 0
\]

or

\[
q \nu_p (p + b n) E_y + q \nu_p^2 (p + b^2 n) B_z E_x = 0
\]

From which,

\[
E_y = - \frac{(p - b^2 n)}{(p + b n)} \mu_p B_z E_x \quad (3-165)
\]

Equation (3-165) shows that \( E_y \) increases proportionally as \( E_x \) and/or \( B_z \) are increased. It becomes greater by increasing the carrier mobilities \( \mu_n, \mu_p \) which indicate that \( E_y \) is very sensitive to the device material and biasing conditions [1,45,86]. \( E_y \) is also seen to depend on the device doping and its excursion [98-102]. Figure (3-31) shows the expected behaviour of \( E_y \) as a function of \( E_x \) at different values of \( B_z \) and doping conditions.

The Hall voltage \( V_H \) is given by the integration of \( E_y \) over the slab width \( w \).

\[
V_H = - \int_0^w E_y \, dy
\]

\[
= \int_0^w \frac{E - b^2 n}{p + b n} \mu_p B_z E_x \, dy
\]

### 3.9.5 Magnetoresistance Effects

When Hall contacts are kept short circuited, i.e. \( J_y = J_{ny} + J_{py} \neq 0 \) which sinks the charge accumulated at the slab edges and forces \( E_y \) to decay to zero. Assuming no charge accumulation, the \( Y \)-direction hole and electron transport equations develop to:
Fig (3-31) Variation of the Hall field $E_y$ as a function of longitudinal field $E_x$ at different values of the magnetic field intensity $B$ and doping levels.

Fig (3-32) Hall angle $\theta$ and the transversal current $J_y$. 

Slightly n $p < b^2n$

Strongly p $p > b^2n$
\[
\begin{align*}
J_{py} &= \mu_p B_x (q^2 \mu_p E_x) \\
J_{ny} &= -\mu_n B_z (q^2 \mu_n E_x)
\end{align*}
\] (3-167)

From which the total Y-direction current is given by

\[
J_y = J_{py} + J_{ny} = \left[ q^2 \mu_p^2 - q^2 \mu_n^2 \right] B_z E_x
\]

\[
= (p-b^2 n) q^2 \mu_p^2 B_z E_x
\] (3-168)

The X-direction current density is similarly derived and expressed as:

\[
J_x = q^2 \mu_p E_x + q^2 \mu_n E_x
\]

\[
= (p+b n) q^2 \mu_p E_x
\] (3-169)

Combining Eqs. (3-168) and (3-169) to formulate the total slab current \( J \), yields

\[
J = \sqrt{J_x^2 + J_y^2} = \sqrt{(p+b n)^2 (q^2 \mu_p E_x)^2 + (p-b^2 n)^2 (q^2 \mu_p^2 B_z E_x)^2}
\] (3-170)

This current becomes no longer X-directed owing to the Hall force which deviates the current stream up by an angle \( \theta \). The X-directed current component is decreased, as shown in Fig. (3-32) and may be decreased further with further increase of the magnetic field density \( B_z \), which means that the X-component conductivity \( \sigma_x \) becomes smaller than the expected value of the slab conductivity \( \sigma \)

\[
\frac{\sigma_x}{\sigma} = \frac{J_x}{J} = \frac{1}{\sqrt{1 + \left[ \frac{(p-b^2 n)}{(p+b n)} \mu_p B_z \right]^2}}
\]
Assuming $B_z$ is so small that the second term in the square root is sufficiently smaller than one, then

$$\frac{\sigma_x}{\sigma} = \frac{1}{1 + \frac{1}{2} \left\{ \frac{(p-b^2n)}{(p+bn)} \mu_p B_z \right\}^2}$$

Equation (3-171) may be rewritten in terms of the X-directed slab resistivities $\rho_x$ and $\rho$ as:

$$\frac{\rho_x}{\rho} = \left[ 1 + \frac{1}{2} \left\{ \frac{(p-b^2n)}{(p+bn)} \mu_p B_z \right\}^2 \right]$$

From which X and Y-directed resistivity components $\rho_x$ and $\rho_y$ are formulated by:

$$\rho_x = \rho \left[ 1 + \frac{1}{2} \left\{ \frac{(p-b^2n)}{(p+bn)} \mu_p B_z \right\}^2 \right]$$

and

$$\rho_y = \rho \left[ 1 + \frac{1}{2} \left\{ \frac{(p+bn)}{(p-b^2n)} \mu_p B_z \right\} \right]$$

3.9.6 Effects of the Sample Parameters on the Magnetoresistance

Figure (3-33) demonstrates the expected variations of $\sigma_x$ and $\sigma_y$ with $B_z$ for different values of the doping level $\rho$. We observe that $\sigma_x$ remains equal to $\sigma$ as long as $B_z$ is kept smaller than a certain threshold (the second term in Eqs.(3-171) and (3-172) is ten times smaller than one),

$$B_{th} = \frac{p+bn}{5(p-b^2n)\mu_p}$$

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Variation of $\sigma_x$ and $\sigma_y$ with $B_z$ for different doping conditions.

Effect of transversal current $J_y$ on $V_x$. 
Over which \( \sigma_x \) begins to decrease as increasing \( B_z \) further. On the other hand \( \sigma_y \) increases as \( B_z \) increases and the contrary is true with respect to \( \rho_x \) and \( \rho_y \). \( \sigma_y \) becomes nearly equal to \( \sigma \) when \( B_z \) exceeds its threshold \( B_{zth} \) given by Eq.(3-174). The incremental increase \( \rho_m \) in the value of \( \rho_x \) over \( \rho \) is called the magnetoresistivity. It is given by

\[
\rho_m = \frac{1}{2} \rho \left[ \frac{(p-b^2n)}{(p+bn)} \mu_p B_z \right]^2
\]

(3-175)

### 3.9.7 \( E_y/J_y \) Behaviour When the Hall Contacts are not Open Circuited and the \( Y \)-Current is not Zero

This, in fact, represents a practical case since the voltmeter used to measure the voltage \( V_H \) is not ideal, i.e. it functions as a sink as shown in Fig.(3-34) for a certain but very small current \( J_y \) which tends to reduce the value of \( V_H \).

From Eqs. (3-164) up to (3-167),

\[
E_y = -\frac{(p-b^2n)}{(p+bn)} \mu_p B_z E_x + \frac{J_y}{q\mu_p (p+bn)} = -E_{yo} + \frac{J_y}{q\mu_p (p+bn)}
\]

(3-176)

From which,

\[
V_H = \int_0^\omega \left[ \frac{(p-b^2n)}{(p+bn)} \mu_p B_z E_x - \frac{J_y}{q\mu_p (p+bn)} \right] dy
\]

or

\[
V_H = \left[ \frac{(p-b^2n)}{(p+bn)} \mu_p E_x \omega \right] B_z - \int_0^\omega \frac{J_y}{q\mu_p (p+bn)} dy.
\]

(3-177)

Figure (3-35) illustrates the variation of \( E_y \) with \( J_y \) for different values of \( B_z \) and \( E_x \). We observe that \( E_y \) decreases as \( J_y \) increases and becomes zero when \( J_y \) attains its short circuit value \( J_{sc} \). It has also been observed that the \( E_y \) is always negative and both \( E_y \) and \( J_{sc} \) increase as the values of \( B_z \) and/or \( E_x \) increase.
Fig (3-35)
Variation of $E_y$ with $J_y$ for different values of $B_z$ and $E_x$. 
3.9.8 Hall Voltage and Magnetoresistance in MOSFET

This case differs from that studied in thin films in that the charge acted upon by the magnetic field is controlled by the gate and drain voltages. Also some MOSFET parameters (such as the threshold voltage \( V_T \), the channel depth \( d_0 \), the pinch-off region length, etc.) affect the behaviour of the Hall voltage. The Hall voltage and the magnetoresistance are dependent on the biasing conditions and device geometry. This makes the magnetic properties more strongly dependent on the biasing voltages and the device geometry.

Referring to Eq. (3-167), the channel transversal current \( \Delta I_{DS} \) caused due to the Lorentz force can be formulated in terms of the MOSFET biasing voltages \( V_{GS} \) and \( V_{DS} \), the magnetic field \( B_z \) and the longitudinal channel field \( E_x \) by

\[
\frac{\Delta I_{DS}}{I_{DS}} = \frac{q \mu_n B_z}{d_0 \left[ 1 - \frac{V_{DS}}{2(V_{GS} - V_T)} \right]}
\] (3-178)

This equation shows that \( \frac{\Delta I_{DS}}{I_{DS}} \) increases as \( V_{DS} \) increases and becomes larger for increasing values of \( B_z \) and/or smaller values of \( V_{GS} \). It is also observed that \( \frac{\Delta I_{DS}}{I_{DS}} \) is dependent on the channel depth \( d_0 \). We have shown in some publications [8,26] that \( d_0 \) is dependent on the MOSFET biasing and geometry which affects the behaviour of the \( \frac{\Delta I_{DS}}{I_{DS}} \) curves strongly varying with \( V_{GS} \), \( V_{DS} \), \( L \), and \( h_0 \).

Figures (3-36), (3-37) and (3-38) show the expected variations of \( \frac{\Delta I_{DS}}{I_{DS}} \) with the device biasing voltages \( V_{GS} \) and \( V_{DS} \) at different values of the magnetic field \( B_z \) when rectangular formed gate MOSFETs (RG-MOSFETs) are considered.
Fig (3-36-a,b,c)
Dependence of the drain current reduction $\Delta I_{DS}$ on $V_{DS}$ and $B$ when $d_0$ is either constant or variable.
Fig (3-37-a,b)
Dependence of the drain current reduction $\Delta I_{DS}$ on $V_{GS}$ and $V_{DS}$ when $d_0$ is either constant or variable.

**Fig (3-38)**
Variation of $\Delta I_{DS}$ with $I_m$ force at different values of $V_{DS}$. 
The analysis and modeling of the trapezoidal formed gate MOSFET (TG-MOSFET) indicate completely different behaviour for \( \frac{\Delta I_{DS}}{I_{DS}} \). As Fig. (3-39) and Fig. (3-40) show: \( \frac{\Delta I_{DS}}{I_{DS}} \) decreases as \( V_{DS} \) increases. This is caused by the lateral field \( E_z \), which prevents the current from being shifted up or down by the action of the magnetic field, as \( V_{DS} \) increases. The increase of \( V_{GS} \) inhibits the increase of \( E_z \) which allows \( \frac{\Delta I_{DS}}{I_{DS}} \) to be larger for increased values of \( V_{GS} \).

Referring to Eq. (3-166) the Hall voltage \( V_H \) can be formulated by

\[
V_H = \int_0^2 E_z \, dz = Z \mu_n B_z E_x
\]

which develops to

\[
V_H = \frac{Z \mu_n B_z V_{DS}}{L} \quad V_{DS} < V_{GS} - V_T \tag{3-179-a}
\]

\[
V_H = \frac{Z \mu_n B_z (V_{GS} - V_T)}{L} \quad V_{DS} \geq V_G - V_T \tag{3-179-b}
\]

This equation shows that \( V_H \) increases as \( V_{DS} \) increases (as long as \( V_{DS} \) remains smaller than the saturation value \( V_{DSS} = V_{GS} - V_T \)). When \( V_{DS} \) is larger than \( V_{DSS} \), \( V_H \) becomes constant and independent of \( V_{DS} \) variations. However, the increase of \( V_{DS} \) even in the ohmic region of operation tends to decrease the probability of charge separation (by Lorentz force) because the electrons go to the drain before succeeding in arriving at the channel lateral sides. As a consequence, \( V_H \) may decrease at high values of \( V_{DS} \) as shown in Fig. (3-41).

According to Eq. (3-179), \( V_H \) should increase as \( V_{GS} \) increases, this is because the channel current \( I_{DS} \) increases as \( V_{GS} \) increases which creates a greater Lorentz force and leads to a greater lateral current \( \Delta I_{DS} \).
Fig (3-39-a,b)
Variation of $\Delta I_{DS}$ with $V_{DS}$ for different values of $V_{GS}$ when $d_0$ is either constant or variable.
Fig (3-40) Variation of $\Delta I_{DS}$ with $V_{GS}$ for different values of $V_{DS}$ in TG-MOSFET's.

Fig (3-41-a,b) Dependence of $V_H$ on $V_{DS}$ and $V_{GS}$
PART 5: CONCLUSIONS
3.10 CONCLUSIONS

We have studied the carrier and crystal heating phenomena and evaluated their effects on the VLSI MOSFET operation and performance (section 3-3 to 3-5). This type of study is very important for the understanding and investigation of the hot carrier energy distribution and its dependence on the electric fields in MOSFET VLSI devices and circuits. The traditional MOSFET models failed to follow the scaling down trends which forced us to introduce a new simple but accurate model to evaluate the channel activities of the rectangular (traditional) and trapezoidal (novel) formed gate MOSFETs. This helped to develop analytical models for the prediction and simulation of the hot carrier gate current $I_g$, the hot carrier substrate current $I_S$ and the threshold voltage shift $\Delta V_T$. The effects of the device geometry, biasing conditions and technology of fabrication are taken into account.

The studies and analysis of this chapter reveal the precautions which have to be considered and are to be taken into account in order to remove or minimize the device leakage current and/or the threshold voltage shift. It has been shown that it is possible to increase the hot carrier gate current at relatively smaller biasing voltages by employing the trapezoidal formed gate MOSFET, and also that this new type of gate form has great potential both in respect of reducing the MOSFETs $1/f$ noise and in improving the MOSFET operation and performance.

Attention has been given to the defect generation in the Si-SiO$_2$ interface and oxide and their effect on the channel depth (section 3-6). A new modeling of the channel depth determination have been elaborated. This new criterion helped to remove a lot of inconsistencies in the hot carrier models.

A study and investigation of MOSFET noise sources is introduced in section 3.7. It has been shown that the most important sources are associated with 1) the channel current and 2) the hot carrier gate current. The first effect has been described in detail by many authors. However, the second effect has not been given the appropriate attention. We have overviewed the efforts devoted to the study and analysis of the $1/f$ noise associated with the channel and the hot carrier gate current.
CHAPTER 4

EXPERIMENTAL DETAILS
4.1 INTRODUCTION

Modeling and formulation of hot carrier phenomena and related activities in MOSFET's, and other devices have been described in the previous chapter. Device stressing by different mechanisms and magnetic propertization have also been developed. Moreover, two new techniques of noise cancellation have been suggested.

In this chapter experimental details are dealt with; the measurement to be carried out; the techniques to be adopted; the apparatus to be used; the procedures to be followed; the constraints and precautions to be considered; and, finally, the sample design and preparation and the experimental setup.

Device stressing by high voltage and current was used as a tool for reliability monitoring and study. In this case carriers are heated up by strong electric fields and allowed to bombard the structural lattice where bonds are broken and atoms are displaced or removed from their original sites. Thermal heating is done thereafter to enable the lattice to reconstruct the broken bonds and return the displaced atoms to their sites: in other words to enable the structural lattice to reconstitute its original state. However this mechanism manifested a narrow region of operation existing at the Si-SiO₂ interface (case of MOSFET structure). Aimed at widening this region (going deeper into the oxide layer), X-ray was used as a stressing tool and UV was used as an annealing one. The significance behind this utilisation is attributed to greater capability of penetration and greater quantum energy of X-ray over UV. These features make X-rays break the bonds and cause the atoms to move out of their equilibrium positions while exposure to UV excites lattice vibrations. These vibrations, as will be shown, make it probable that a broken bond will reconstruct and that a displaced atom will regain its equilibrium site. Owing to their penetrability both X-ray and UV cover the majority of the oxide layer.
4.2 MEASUREMENTS TO BE CARRIED OUT

The measurements to be performed are:

a) Channel Activities which manifest themselves through the variation of the channel current $I_{DS}$ with the drain and gate voltages $V_{DS}$ and $V_{GS}$ and the influence of the device geometry (channel length $L$/width $W$ and oxide thickness $h_o$) on the current/voltage characteristics. New parameters of interest are the channel depth $d$, and the pinch-off region length $\Delta \ell$.

b) Oxide Layer Activities which manifest themselves through the variation of the hot carrier gate current $I_g$ with the device biasing voltages $V_{DS}$ and $V_{GS}$ and geometry $L$, $W$ and $h_o$. Here the parameters and variables to be investigated and characterised are the crystal and carrier temperatures $T$ and $T_c$ respectively, the hot carrier injection probability $P_{inj}$ and finally the threshold voltage shift and instability $\Delta V_T$ caused by defect generation and carrier trapping inside the oxide.

c) Substrate Activities which manifest themselves through the variation of the hot carrier substrate current $I_s$ with the device biasing voltages $V_{DS}$, $V_{GS}$ and $V_b$ and geometry $L$, $W$ and $h_s$. Here, the new parameters of interest are the back bias $\Delta V_b$ caused by $I_s$ and its effect on the threshold voltage shift and instability $\Delta V_T$. The bulk resistance $R_s$ and its regenerative effect on surface carrier multiplication are also to be investigated.

d) Study the effect of the gate form and/or nature on the carrier heating capability and on the cancellation of device noise. Here the MOSFET transconductance $g_m$ and its dependence on the gate form and channel length is to be demonstrated.

e) Device stressing by high voltage and current operation and/or by X-ray and UV irradiation. Here the device mobility $\mu$, threshold voltage $V_T$ and noise $e_n$ are to be characterised in terms of the stressing tool, period of stressing, stressing procedure and device geometry.

f) Magnetic properties, shown by thin films of amorphous GaAS can be characterised in terms of the magnetic field intensity $H$ and the sample doping and geometry. The significance behind this choice is the analogy between the MOSFET channel and the thin film while both of them provide a thin sheet of mobile carriers responding to applying magnetic and electric fields. Here the characteristic parameter to be investigated are the Hall voltage $V_H$, the magnetoresistivity and conductivity $\rho_m$ and $\sigma_m$ and the magnetic current $I_m$. 

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4.3 TECHNIQUES AND APPARATUS

The technique of measurements we apply to characterise a certain activity depends on a related background theory and modeling. The apparatus used to achieve these measurements depend on the phenomenon to be investigated, the physical parameters to be dealt with, the levels and orders of magnitude of these parameters and the desired accuracy and precision to be accomplished.

4.3.1 Channel Activities

The channel activities' characterisation deals with current levels ranging from tenth to tens of milliamperes and drain and gate voltages ranging from half to tens of volts; therefore no special apparatus is need. Only a minimum of precautions are considered when building up the experimental set-up (see Fig. (4-1)) used to perform the measurements, in which the device is directly shunted by the voltmeter while multimeter is connected in series with the drain resistance $R$. This scheme guarantees minimum percentage error in current ($\sim 0.02\%$) without any error in voltage. The background theory is as follows: The slope of the $I/V$ characteristic curves (see Chapter 3) is:

$$\frac{\partial I_{DS}}{\partial V_{GS}} = C_0 \mu \frac{Z}{L} V_{DS}$$  \hspace{1cm} (4-1)

This slope is experimentally measured and oxide capacitance $C_0 = \frac{\varepsilon_{ox}}{h}$ is equal to $8.85 \times 10^{-4}$ F/m$^2$ at $h_o = 400 \ \text{Å}$ and oxide dielectric constant of 4. The values of $Z$, $L$ and $V_{DS}$ are also known. This manipulation gives the value of $\mu$ under any condition of operation. The cross-over intersection of the tangent to the $I_{DS}/V_{GS}$ curve with $V_{GS}$ axis gives the value of the $V_T$ and declare any shift $\Delta V_T$.

4.3.2 Oxide Activities

In these activities hot carrier gate current as small as $10^{-14}$ A are to measured with minimum percentage error. We therefore use HP4140 pico-ampermeter which can measure currents as small as $10^{-15}$A and guarantees accuracy better than $0.1\%$
Experimental set up for hot carrier measurement.
when measuring currents greater than $10^{-12}$A. The experimental setup of Fig. (4-1) was used and the following precaution is to be considered:

a) On the chip level (see Fig. (4-2)), a guard ring surrounding the gate window and the gate electrode connections is diffused. When this guard ring is biased to the same gate potential, the surface and gate edge leakage currents are decreased beneath $10^{-15}$A assuming gate to ring mismatch voltage of $10^3$V and the surface resistance per unit surface $R = 10^{12}\Omega$.

b) On the package level, the chip is encapsulated inside a metallic package filled with nitrogen. The gate lead is surrounded by isolating pearls and biasing the metal package to the same gate potential to cancel the package leakage current.

c) On the printed circuit board level, a copper guard ring is deposited around the gate copper lead and biased at the same gate potential. (see representation on Fig. (4-1)).

The background theory is as follows: the hot carrier gate current $I_g$ is measured and plotted with $V_{DS}$ at different values of $V_{GS}$ for several device geometries ($L \sim 5\mu m$ to $0.5\mu m$, $Z \sim 100\mu m$ to $3\mu m$ and $h_o \sim 1200 A^0$ to $400 A^0$ (see Fig. (4-2-a)). $I_g$ is also measured with time $t$. The models of Chapter 3 are used to achieve computer-aided simulation of $I_g$. Some parameters (oxide capture cross section of electrons $\sigma_e$ and holes $\sigma_p \sim 10^{-12} m^2$/oxide electron mobility $\mu_{oax} = 40 cm^2/v. sec.$, oxide hole mobility 3.9 $cm^2/v. sec./oxide$ defect density $N_{ox} \sim 10^{10}/cm^3$ etc.) were not yet precisely determined. Fitting of measurements and simulation helped to get an accurate value of these parameters.

4.3.3 Substrate Activities

These activities comprise currents ranging from $10^{-10}$ to $10^6$A. A lower performance pico-ampermeter is connected as shown in Fig. (4-1) where the same experimental set-up is used. Here we need to plot $I_B$ as a function of $V_B$ for different values of $V_{DS}$ and $V_{GS}$. Different device geometries are to be examined. Similar curves can be simulated using the $I_B$ models elaborated in Chapter 3. Fitting of simulation and measurements helped to get an accurate value of those parameters which were not precisely determined. The efficiency by which carriers are collected by the substrate $\eta (\sim 0.09$ to $0.0007)$, the substrate bulk resistance $R_S (\sim 37$ to $166 k\Omega)$ and surface recombination velocity $S (\sim 5m/sec.)$ are examples of these parameters.
Different channel length rectangular MOSFET

(a) Photolithography layout, b) Silicon wafer and c) Copculates chip.
4-3.4 Effect of Gate form on Device Performance

In this concern two special MOSFET's were designed and realised:

a) Trapezoidal formed gate with its narrow width at the drain which is characterised by greater capability of carrier heating due to the channel field enhancement. This device is used with the new fast EEPROM for erasing and programming. The experimental set-up shown by Fig. (4-1) is used to investigate this feature, which manifests itself as an appreciable increase in the value of Ig in comparison with rectangular gate MOSFET's when same biasing conditions are used. Fig. (4-3-a) shows the layout of a pair of trapezoidal gate MOSFET's TG1 and TG2 and another pair of rectangular ones, RG1 and RG2, implanted on the same chip and having the same channel length L. These test devices were fabricated by the French company Thomson-Microelectronics. Fig. (4-3-b) shows the chip encapsulated and prepared for measurements.

b) A Trapezoidal formed gate, with its wide width at the drain, is used (as explained in chapter 3) for noise cancellation. This occurs through the reduction of the device transconducance. Its capability of cancellation increases with increase of the gate side steepness \( \beta \) (\( \sim 10 \) to \( 100 \) for \( \beta \sim 2 \) to 6). The experimental set-up shown in Fig. (4-4) is used to verify this feature. One of the two trapezoidal gate MOSFET's of Fig. (4-3) is used (rectangular gate MOSFET may be used instead) in amplifying scheme. The MOSFET input is short-circuited. The drain voltage \( V_1 = A e_n \) represents partially amplified noise and is further amplified by a high gain noise free amplifier which yields.

\[
V_o = G A e_n
\]

(4-2)

with \( A = g_m R_o \)

(4-3)

and G is given. The reference voltage \( V_R \) is variable and used for zero adjustment.
Fig (4-3-a, b)

a) Lay out pair of trapezoidal gate MOSFET's. and another pair of rectangular gate MOSFET's.

b) Shows the ship encapsulated.
Fig (4-4)
Experimental set-up used to measure MOSFET noise.
4-3.5 Device Stressing by X-ray and UV

For reasons of reliability and persistivity studies of MOSFET, hot carriers have been used to stress the Si-SiO$_2$ interface. Unfortunately the effect of this mechanism is limited to very thin sheet (~40 Å to 100 Å) of SiO$_2$ layer. This is attributed to the relatively limited energy of the hot carriers and the fast dissipation of this energy as the hot carriers penetrate into the oxide. Thermal heating (600 °C) was used for annealing.

To cover thicker layers of oxide during stressing and annealing, X-rays have been used since they have shown high penetrability through the Al-layers of the MOSFET gate electrodes and the SiO$_2$. They also have small reflectance and absorption. The following aspects are necessary for understanding this later subject.

a) Absorption and Reflectance of X-rays

Further understanding of the electronic transitions which can occur in atoms can be gained by considering not only the interaction of electrons and atoms, but also the interaction of X-rays and atoms. [103]

When X-rays encounter any form of matter, they are partly transmitted and partly absorbed. Experiment shows that the fractional decrease in the intensity $I$ of an X-ray beam as it passes through any homogeneous substance is proportional to the distance traversed $x$. In differential form [103],

$$\frac{-dI}{I} = \mu dx$$

(4-4)

where the proportionality constant $\mu$ is called the linear absorption coefficient and is dependent on the substance considered, its density, and the wave length of the X-rays. Integration of Eq. (4-4) gives

$$I_x = I_0 e^{ux}$$

(4-5)

where $I_0 = $ intensity of incident X-ray beam and $I_x = $ intensity of transmitted beam after passing through a thickness $x$. 

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The linear absorption coefficient \( \mu \) is proportional to the density \( \rho \) which means that the quantity \( \mu / \rho \) is a constant of the material and independent of its physical state (solid, liquid, or gas). This latter quantity, called the mass absorption coefficient, is the one usually tabulated. Equation (4-5) may be rewritten in a more usable form

\[
I_x = I_e e^{-(\frac{\mu}{\rho})px}
\]

(4-6)

Where the values of the mass absorption coefficient \( \mu / \rho \) are given for Al [103] with different wavelength of x-rays used as follows:

\( (\mu / \rho) = 50.23 \text{ cm}^2/\text{gm}, 37.14 \text{ cm}^2/\text{gm} \) corresponding to x-ray wavelengths \( \lambda_{x\alpha} = 1.542 \text{ Å} \) and \( \lambda_{x\beta} = 1.392 \text{ Å} \) respectively, and the density \( \rho = 2.70 \text{ gm/cm}^3 \) for Al.

From these values we can calculate the linear absorption coefficient \( \mu \) as follow \( \mu = 135.82 \text{ cm}^{-1} = 135.82 \times 10^2 \text{ m}^{-1} \) with \( \lambda_{x\alpha} = 1.542 \text{ Å} \).

The way in which the absorption coefficient varies with wavelength gives the clue to the interaction of X-rays and atoms. The lower curve of Fig. (4-5) shows this variation for a nickel absorber, it is typical of all materials. The curve consists of two similar branches separated by a sharp discontinuity called an absorption edge. Along each branch the absorption coefficient varies with wavelength, approximately according to a relation of the form

\[
\frac{\mu}{\rho} = k\lambda^3Z^3
\]

(4-7)

where \( K \) = a constant, with a different value for each branch of the curve, and \( z \) = atomic number of absorber. Short wavelength X-rays are therefore highly penetrating and are termed hard, while long wavelength X-rays are easily absorbed and said to be soft.

In this work, the thickness of the Al layer is about \( \approx 0.2 \mu \text{m} \) (this thickness was measured by DRD lab. of Thomson Semiconductor Grenoble, France) and the linear absorption coefficient \( \mu \) (Al) is \( \approx 135.621 \text{ cm}^{-1} \) with Cu K\( \alpha \) radiation \( \lambda = 1.542 \text{ Å} \).
Fig (4-5)
Variation with wavelength of the energy per X-ray quantum and of the mass absorption coefficient of nickel[103]
Theoretical and measured reflectance values as a function of wavelength for aluminum film in the infrared[104].
Å [Cu Kα is monochromatic and strong beam], therefore the intensity of reflected beam is very weak and the intensity of the transmitted beam of X-ray is very high.

b) Absorption And Reflectance of UV

The reflectance $R$ of evaporated Al films prepared under high vacuum conditions has been measured, by Bennet, Silver and Ashley, with precision in the wavelength region from 0.2μm in the UV to 32μm in the IR. The results of these measurements are shown in Figs. (4.6 and 4.7), from which we observe that $R$ has a shape having its minimum at $\lambda = 0.825μm$. It is also noticed that $R$ becomes smaller at shorter wavelengths $\lambda$ (UV region). These results are in agreement with the theory of Bennet, Silver and Ashley,

$$R = 1 - (\frac{2ω}{πσ₀})^{1/2} [(1 + \omega^2τ^2)^{1/2} - ωτ]^{1/2}$$

(4-8)

with $σ₀$ is the dc conductivity
$τ$ is the electron relaxation time
ω is the angular frequency

though the transmittance is still low

c) Radiation induced defect

Radiation damage has been perhaps the most important aspect to be researched in MOSFET. Attention will be focused on radiation-induced traps which seem to offer good links for studying the defect related phenomena. Defect generation occurs at impingement of radiation such as γ-rays, x-rays, neutrons. This process is associated with creation of hot electron or hot hole. These entities travel, as shown in Fig. (4-8), away from the collision site and migrate to the gate electrode or to the Si-SiO₂ interface (depending on the MOSFET biasing) with a transport rate determined by the diffusion constant and the intensity of the oxide electric field. It was conceptually known (by Helms and Poindexter) that the secondary holes react with hydrogen and release H⁺ ions which migrate to the interface and react to produce interface traps. This latter process of oxide defect generation and consequent interface trap creation is, as was verified by measurements of McLean et al., the dominant. McLean et al. showed also that wet oxide allows more damage than the dry one. The interface traps
Fig (4-7)
Measured reflectance values as a function of wavelength for aluminum film in the ultraviolet, visible, and near infrared[104].
Fig (4-8)
Mechanism of defect generation by X-ray irradiation.
are then considered to be positively charged and have a build-in rate (during irradiation) which is oxide field dependent.

A monochromatic CuKα (λ = 1.5 Å) radiation was used as X-ray source. The power supply of the X-ray tube could be operated in steps of 10kV and currents between 5 and 80 mA in steps of 5mA. The experimental condition chosen was a fixed X-ray potential of 20kV (which corresponds to phonon energy of 20keV) and tube current varying between 10, 20 and 30mA corresponding to beam power of 0.2kVA, 0.4kVA and 0.6kVA and photon fluxes of 0.6, 1.2 and 1.8 x 10^{17}/sec. The dose rate at the sample position has been established by measuring the dose rate received on an X-ray film badge placed at the sample position and irradiated. The irradiation process was carried out on a standard Philips 1050/70 powder diffractometer, in Loughborough University Department of Physics X-ray Lab.

The devices to be irradiated were neither biased nor heated during stressing. They are left under irradiation for different lengths of irradiation time (1 to 500 sec.) by different beam energies.

Concerning annealing by UV the stressed devices are exposed under the same biasing and heating conditions to UV for different lengths of annealing time using the experimental set-up shown in Fig. (4-9). Five 8w, 254 nm wavelength UV sources were used. The measured irradiation intensity was 30, 60, 90, 120 and 150 mw/cm² (i.e in terms of photons are 3.8x10^{16}/sec, 7.6x10^{16}/sec,11.4x10^{16}/sec, 15 x 10^{16}/sec, 19 x 10^{16}/sec).

The experimental procedure was as follows:
1. Adjust the height of moving base.
2. Locate a photometer on the test sample base.
3. Measure the UV intensity in W/cm².
4. Replace the photometer by the sample to be irradiated.
5. Leave the sample under irradiation for the prescribed irradiation time (~ some hours).
6. Take out the test sample at the end of the irradiation time, measure the I/V characteristics and the evolution of its V_T.
Fig (4-9)

Schematic Diagram of UV apparatus.
In both X-ray and UV irradiation the effective dose of radiation received by SiO$_2$ is smaller than that given from the source. This is attributed to the attenuation of the beam power caused due to the absorption in the overlying aluminum or polycrystalline silicon. Several chips were irradiated and examined so as to have a certain and clear picture of the device performance and reliability. In the case of UV this would be very much smaller.

In both cases the \( I/V \) characteristics are established using the experimental set-up of Fig. (4-1) and the noise is measured using that shown in Fig. (4-4). Straightforward manipulation of these results gives a complete picture about the behaviour and variation of the device parameters: the threshold voltage \( V_T \), the mobility \( \mu \), the surface state density \( N_{ss} \) and oxide density of defects \( N_{ox} \) with the stressing time \( t_n \), the X-ray beam intensity, the number of stressing cycles etc.

4-3.6 Magnetic Properties

It is desired here to study and characterise MOSFET behaviour in the presence of magnetic field. We focus our attention on the Hall Voltage, transversal Lorentz current and the magneto-resistance. The magnetic field needed to perform the measurements related to the magnetic properties and characterization of the MOSFET behaviour in the presence of a perpendicular applied magnetic field was provided using the arrangement shown in Fig. (4-10). The magnetic field density \( B \) at the sample position was controlled through varying the magnetic current \( I_m \) as well as by the gap distance between the poles of the magnet. The magnetic field was measured at the position of the device by means of a Hall probe (Chauvin Arnoux: CTM 2010).

The calibration curve for the small magnet used in the Physics Department in Jeddah given in Fig. (4-11). This magnet could be operated with a maximum current of 10A, corresponding to a magnetic field 0.3T. At the Physics Department in Loughborough University a much larger magnet was used (a Newport-Pagnell Type A 401/2 Electromagnet in connection with two Phillips PW 1040 power supplies). The calibration curves for this magnet is given in Fig. (4-12). In order to obtain a sufficiently large magnetic field, both magnet cores were separately powered with a maximum current of 20A corresponding to a field of 2T. This modification necessitates the addition of a new water cooling circuit.

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Fig (4-10)
Experimental set up for hot carrier measurement.
Calibration curves of magnetic field $B$ (King Abdul-Aziz University).
Fig (4-12)
Calibration curves of magnetic field B (Loughborough University).
Special devices have to be designed to perform the magnetic measurement, a) Thin films, which allows easy and direct Hall voltage measurement. The experimental setup used is shown in Fig. (4-13).

b) Rectangular and trapezoidal gate MOSFET's (RG MOSFET and TG MOSFET's) like those shown in Figs (4-14-a and 4-14-b) respectively are used to measure the channel current shift caused due to the transversal Lorentz current.

c) To increase the sensitivity towards much smaller current shifts, a split channel oval drain MOSFET (see Fig. 4-15) was designed and realised. This new channel form introduced a clear technique for leakage compensation and provides a possibility of compensating for any mismatch between the two channel splits. The use of an operational amplifier in the experimental set-up increased further the sensitivity and accuracy of measurement.

4-4 SAMPLE DESIGN AND PREPARATION

MOSFET devices and (A-GaAs) thin film samples were used to perform measurements and verify the theory of the thesis. (A-GaAs) thin film were supplied by Nottingham University, UK. and the MOSFET samples were supplied by the French Society Thomson EFCIS of Grenoble, France. As pointed out different MOSFET layouts and topologies were needed:

a) Short channel, rectangular formed gate MOSFET to perform the carrier heating phenomena (see Fig. (4-2)).

b) Trapezoidal formed gate MOSFET to perform the noise reduction and leakage minimisation measurements (see Fig.(4-3)).

c) Dual formed (rectangular and trapezoidal on the same chip) were used to perform dressing phenomena and study effect of gate form (see Fig. 4-3)).

d) Split drain MOSFET to characterise the Hall voltage and magnetoresistance effects (see Fig. (4-15)). RG and TG MOSFET's (see Fig. 4-14-a and 4-14-b) were also used.

The different topologies are designed in Jeddah and fabricated in the French Society Thomson EFCIS of Grenoble, France. The test samples were supplied in two forms:
Fig (4-13)
Experimental set up for Hall voltage measurement.
Fig (4-14-a)
Experimental set up for measuring $\Delta I_{DS}$. 
Fig (4-14-b)
Experimental set up for measuring $\Delta I_{DS}$ in the RG and TG MOSFET's.
a) IC arrays on wafers (150000 device/cm²) where the measurements were achieved with help of mobile needles and a microscope having magnification of 300. (Fig. (4-2)).

b) IC device on chip capsulated in such a manner as to allow access and visual examination by microscope of the device and its connections (Fig. (4-3)). It allowed exposure of the device to X-ray or UV radiation.

N-channel polycrystalline silicon gate test MOSFET's have been used. They were 3μm up to 100 μm wide with channel length L ranging from 0.5μm to 5μm. p-type silicon wafers of (100) orientation and 40±5Ω cm resistivity (N_A = 3.5 ± 0.5 x 10¹⁴/cm³) were used. Thick field oxide of about 0.5μm thickness was grown by a selective oxidation process using silicon nitride masks. The gate oxide (with thickness h_0 = 400 Å) was grown in dry oxygen ambient at 1000°C. SiTa_2 was used for the interconnections of the polycrystalline silicon to the source and drain junctions through contact holes The polycrystalline silicon (highly doped n-type or Al gate 2-3 μm thick) and the SiTa_2 layers (about 0.2μm thick) are deposited by sputtering magnetron. All samples were given a post-metallisation annealing at 450°C to reduce the density of the interface states and the fixed oxide charges. In special cases when transparent gates are required, thinner Al layers are used (~ 0.2 μm).

A top view of the TG and RG-MOSFET on chips which were used for hot carrier stressing, magnetic properties and noise cancellation experiments are shown in Figs. (4-2 and 4-3). The hot carrier-related measurements and the device scaling down were studied on-wafer MOSFET situated on a VLSI array. These MOSFET devices have a polysilicon or Al-gate (the same is true with respect to Figs. (4-2 and 4-3)). The electrical measurement on these devices were made with the help of needle contacts equipped with a microscope for this purpose. This arrangement was made at the Engineering Department of the King Abdul Aziz University.

All test samples are integrated on p-type silicon wafers of 99.9999% purity, 5 inch diameter and 300 μm thickness in integration density of more than 150,000 device per cm² of the wafer surface. The wafers are cut thereafter in tranches by a special laser technique and are provided with contacts and are then encapsulated in chips.
Fig (4-15).
Experimental setup for measuring $V_H$. 
Thin film samples supplied by Nottingham University have been used to measure the Hall voltage and magneto-resistance effects and to make a comparison with those of MOSFET.

4-5 COMPUTER AIDED ANALYSIS

A simulation program, based on the modelling of the preceding chapter, has been developed with the help of the technical staff at King Abdul Aziz University Physics Department. This software is capable of characterising and analysing all parameters related to the theory of carrier heating phenomena and their effects on the MOSFET operation and their dependence on the device geometry, technology and biasing.

The channel depth $d_0$, pinch-off region length $\Delta l$, carrier multiplication factor $\alpha$, noise reduction factor $\chi$, surface recombination velocity $S$, channel mobility $\mu$ and threshold voltage $V_T$ are examples of these parameters. Simulation programs for the magnetic properties are also elaborated.

A lot of devices were automatically examined using CAPA techniques to determine the values of their parameters (nominal value and standard deviation). These values are continually updated and fed into a simulation program.

Figs. (4-16 and 4-17) show examples of flow diagrams of some simulation programs elaborated for characterization and analysis.

4-6 CONCLUSIONS

The measurement to be carried out have been demonstrated in this chapter with detailed explanation of the background theory, the technique of measurements, the design and implementation of experimental set-up used to perform the desired measurements, the design and preparation of test samples and the constraints and precautions to be considered with each experiment.
\[ I_{DS} = C_{ox} \mu \frac{Z}{L} \left( V_g \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \]

Flowchart:

1. \( V_{DS} > V_{DSM} \)
   - Yes
   - \( V_{GS} > V_{GSM} \)
   - Yes
   - END

   - No
   - No

Fig. (4.16)
Channel Activity Program
\[ V_{DS}, V_{GS}, V_{TO}, V_{DSO}, \Delta V_{DSO}, V_{GSO}, V_{GSO}, \Delta V_{GSD}, V_{DSJ}, \]
\[ Z, L, h_0, d_0, \varepsilon_{si}, \varepsilon_{ox}, C_{ox}, \mu_{oxn}, \mu_{oxp}, \Phi_B, \Phi_B', n_l, \]
\[ \lambda, \ell_f, \ell_{ox}, k, T_0, \sigma, E_c, E_{oxc}, \varepsilon_g, q, x, Y, \alpha, \rho, C_1 \]

\[ V_g = V_{GS} - V_{TO} \]

\[ V_{GSO} \cdot V_{GS\mu} \]

\[ V_{QSO} = V_{QS} + \Delta V_{QS} \]

\[ V_{DSO} \cdot V_{DS\mu} \]

\[ V_{DS} = V_{DS} + \Delta V_{DS} \]

\[ V_{DSS} = V_g \left[ 1 - \left( \frac{\varepsilon_{si} d_0 h_0}{4 \varepsilon_{ox}} \right)^{1/4} \right] \]

\[ k = \left[ \frac{9 \varepsilon_{si} L d_0 h_0}{4 \varepsilon_{ox}} \right]^{1/3} \]

\[ \Delta \ell = k \left( \frac{V_{SD}}{V_{DSS}} - 1 \right)^{2/3} \]

\[ I_{DSS} = C_{oxn} \mu \frac{Z}{2L} \left( \frac{V_{DSS}^2}{1 - \frac{K}{L} \left( \frac{V_{DS}}{V_{DSS}} - 1 \right)^{2/3}} \right) \]
\[ I_{DS} = C_{ox} \mu \frac{L}{W} \left[ V_g - \frac{V_{DS}^2}{2} \right] \]

\[ X_0, X_m \]

\[ X = X + \Delta X \]

\[ X_s = L/2 \]

\[ \Delta X = 0 \]

\[ P_v(X) = \frac{\sigma I_{DS}^2}{(C_{ox} \mu Z)^2 \left[ V_g^2 - \left( \frac{2I_{DS}}{C_{ox} \mu Z} \right) X \right]} \]

\[ E_X(X) = \frac{I_{DS}}{C_{ox} \mu Z \sqrt{V_g^2 - \left( \frac{2I_{DS}}{C_{ox} \mu Z} \right) X}} \]

\[ T(X) = T_0 + \frac{d_x P_v(x)}{\alpha \rho \cdot C_1} H \]

\[ T_s(X) = T(X) \left[ 1 + \left( \frac{E_X}{E_C} \right)^a \right] \]

\[ V_X = V_g \left[ 1 - \sqrt{1 - \left( \frac{V_{DS}}{V_g} \right)^2 \frac{X}{L}} \right] \]

\[ \Delta \Phi = \frac{\varepsilon_s}{2} \frac{kT}{q} \frac{C_{ox}}{d_x n_i} \left( V_g - V_X \right) \]

\[ P_{inj} = \left[ 2 + \frac{\Phi_B}{kT_e + \Delta \phi} \right] \exp \left[ -\left( \frac{\Phi_B + \frac{d_x}{\ell_f} + \frac{\lambda_o}{\ell_{ox}}}{kT_e} \right) \right] \]
Fig. (4.17)
Oxide Activity Program.
The methods and algorithms used to study and analyze the experimental results and exercise comparison between them and their related theory using computer-aided facilities have also been given. Special powerful programs (using basic and Pascal languages) have been elaborated and demonstrated as major and most effective computer-aided analysis tool.

Important precautions and new techniques have been considered on the level of sample preparation, the packing and capsulation and, finally, on the level of printed circuit boards and have manifested a very good potentiality in compensating parasitic and leakage currents and lead to greater sensitivity and better accuracy.

Details of X-ray and UV properties and their interaction with the material can be obtained [103,104].

It must be pointed out also that sometimes measurements are compared to simulation using special manipulation techniques (fitting, regression, ... etc.) to extract the practical values of parameters which were not known before.
5.1 INTRODUCTION

In previous chapters the measurements to be carried out have been annotated together with an explanation of the technique of measurement and the experimental set-up and apparatus. For reasons of accuracy, improvement, and sensitivity enhancement, some practical constraints and important precautions have been introduced. Some details about the background theory of each measurement have also been given. Finally, computer-aided analysis programs with illustrative flow diagrams have been presented.

In this Chapter, the experimental and simulation results will be demonstrated with explanation of how results were obtained, the significance of these results and how the various simulations are compared to experiment. Each will indicate where the results came from, whether they are measured or derived from other measurements and which samples were used.

Attention will be focused on measurements related to activities in: the channel, the oxide, the substrate, the gate form and its effect in noise cancelation, irradiation by X-ray and UV and finally the magnetic properties.

5.2 CHANNEL ACTIVITIES

The main parameters to be investigated here are the channel depth $d_o$ and the pinch-off region length $\Delta l$. The measurement procedure is as follows: for a certain device the $\Delta l$ experimental points (see chapter 3) are deduced from the $I/V$ MOSFET characteristics. Since this method is suitable only in the saturation region of operation, as explained in chapter 3, then alternative method based on the hot carrier gate current measurements is used to complete the characterisation of $\Delta l$ over a wider range of biasing voltages $V_{DS}$ and $V_{GS}$. The $d_o$ experimental points are deduced thereafter.
from the $\Delta l$ characteristic curves and by using the model developed in Chapter 3 for $d_o$. To characterise $\Delta l$ and $d_o$ in terms of $L, Z, h_o$ different geometry devices were used. The experimental set-up of Fig. (4-1) is used for related measurements.

Figure (5-1) shows the measured variation of $d_o$ with $V_{DS}$ for different values of $V_{GS}$. It is observed that $d_o$ remains negligibly smaller as long as $V_{DS}$ is smaller than a certain value of $V_{DS}$ depending on the operating value of $V_{GS}$. For larger values of $V_{GS}$ it is noticed that $d_o$ increases abruptly with $V_{DS}$ until a certain peak is reached. Thereafter it decreases smoothly with further increasing the value of $V_{DS}$. $d_o$ becomes larger for the smaller values of $V_{GS}$. This behavior can be explained as follows: as $V_{DS}$ increases, the channel field $E_x$ increases and accelerates the electrons and drags them along the channel to the drain. This mechanism tends to decrease the period of time during which the electrons are pushed upward by the gate-electrode induced normal-field $E_y$ which consequently leads to deeper channel depth $d_o$. When $V_{DS}$ exceeds a certain critical value, carrier heating takes place. The energetic carriers bombard the Si-SiO$_2$ interface randomly, and create traps in it. These traps enhance the attraction of electrons towards the Si-SiO$_2$ interface, which tends to reduce the channel depth. The degradation of the hot carrier mobility also tends to elongate the period of time during which electrons are pulled upward by the gate-electrode induced-field $E_y$ which enhances the reduction of the channel depth $d_o$. This behavior becomes more important as $V_{DS}$ increases.

Figure (5-2) illustrates the measured variation of $d_o$ with $V_{DS}$ for different values of the channel length $L$. It is observed that $d_o$ undergoes the same behavior with $V_{DS}$ as explained above. It becomes more appreciable with longer channels. As the longitudinal dragging force induced by $V_{DS}$ towards the drain decreases, the electrons will be exposed for longer periods of time to the normal force created by the action of the gate electrode potential. As $L$ decreases, stronger carrier heating takes place, which enhances the trap generation in the Si-SiO$_2$ interface and leads, as explained above, to stronger normal dragging and stronger mobility degradation which
Fig (5-1)
Variation of $d_0$ with $V_{DS}$ for different values of $V_{GS}$ (measured).

Fig (5-2)
Variation of $d_0$ with $V_{DS}$ for different values of channel length $L$ (measured).
causes $d_o$ to shrink down.

Figure (5-3) shows the measured variation $d_o$ with $V_{GS}$ for different values of $V_{DS}$. The figure shows that $d_o$ decreases as $V_{GS}$ increases. $d_o$ becomes larger for smaller values of $V_{DS}$. Such behavior is consistent with the explanation given for Figs. (4-8) and (4-9). The increase of $V_{GS}$ inhibits the growth of $E_s$ as increasing $V_{DS}$, which damps the carrier heating and trap creation phenomena. Therefore we observe a tendency toward saturation of $d_o$ with $V_{GS}$ (more important at $V_{DS} = 12V$).

The solid lines here are not simulation curve. It is plotted here to clarify the behaviour of $d_o$ in function of $V_{DS}$ and $V_{GS}$.

Figure (5-4) illustrates the measured variations of the pinch-off region length $\Delta l$ (as experimentally determined from the I/V characteristics of a MOSFET in saturation) with $V_{DS}$ for different values of $V_{GS}$. It is observed that $\Delta l$ increases proportionally as $V_{DS}$ increases over its saturation value and becomes larger on decreasing the value of $V_{GS}$.

5-3 OXIDE ACTIVITIES

Here the parameters and variables related to the oxide activities which have to be measured and characterised. This was achieved by computer aided simulation of the hot carrier gate current $I_{g_h}$ and $I_{g_p}$ in terms of these parameters, and comparing thereafter these results with those obtained from experimental measurements. The characterization of the channel and carrier temperatures $T$ and $T_s$ are firstly required simulate and characterize the hot carrier injection probability $P_{w}$. This latter needed to evolute the hot electron, the hot hole and the total gate currents $I_{g_h}$, $I_{g_p}$, and $I_g$, respectively. The variations of the threshold voltage $V_T$ observed in the presence of these currents can also be studied and phenomenologically explained. The
Fig (5-3)
Variation of $d_0$ with $V_{GS}$ for different values of $V_{DS}$ (measured).

Fig (5-4)
Variation of the pinch-off region length $\Delta l$ with $V_{DS}$ for different values of $V_{GS}$ (measured).
experimental set-up of Fig. (4-1) was used to achieve these measurements.

5.3.1 Simulation Results

Figure (5-5-a,b) shows the simulation results of the variation of the channel temperature $T$ and the carrier temperature $T_r$ with the drain-to-source and gate-to-source voltages $V_{ds}$ and $V_{gs}$ for different values of the device geometric ratio $Z/L$. Here the average value of $T$ and $T_r$ occurring at mid-distance between the source and drain ($X = L/2$) is considered. Smaller values were expected to be obtained at $X < L/2$ while greater values were obtained at $X > L/2$. It was observed that $T$ and $T_r$ increase as $V_{ds}$ and/or $V_{gs}$ are increased. This is because the channel current $I_{ds}$ and consequently the volume power-density dissipated in the channel $P_v$ increase as $V_{ds}$ and/or $V_{gs}$ increase. It was also seen that $T$ and $T_r$ were higher for smaller MOSFET length $L$. This is accounted for by the greater carrier heating occurring in the shorter channels and the greater volume power-density associated with it.

The squares, circles and crosses are used to distinguish between the different values of $V_{gs}$.

Figures (5-6-a,b) present the simulation results concerning the variation of the injection probability $P_{ij}$ with position $X$ and its dependence on the device biasing voltages $V_{ds}$ and $V_{gs}$ and channel length $L$. The figure shows that $P_{ij}$ increases exponentially with $X$ and acquires greater values with shorter channel lengths. The sensitivity of $P_{ij}$ to $V_{ds}$ variations is seen to be smaller the longer the channel length $L$. When the MOSFET is switched into saturation or near-saturation ($V_{ds} \geq V_{gs}$) the rate of change of $P_{ij}$ with $X$ is increased near the drain and strongly decreased near the source. This is referred to the channel potential distribution $V_x$ which is depressed during saturation so as to correspond to elevated potential near the drain and reduced potential elsewhere.
Fig (5-5-a,b)
Simulation of the variation of the channel temperature $T$ and the electron temperature $T_e$ with $V_{DS}$ for different values of $V_{GS}$ and the device geometric $Z/L$ ratio [89].
Simulation of the dependence of the injection probability $P_{ij}$ on the position $x$, the biasing voltages $V_{DS}$ and $V_{GS}$ and the channel length $L$ [89].
Figures (5-7-a,b) investigate the simulation results of the dependence of the hot-carrier gate-current density $I_s / ZL$ on the position $X$ for different biasing conditions ($V_{DS}, V_{GS}$) and channel lengths $L$. The current density increases with $X$ and becomes greater with shorter channel lengths. The sensitivity of the current density to variations $V_{DS}$ and $V_{GS}$ increases as $L$ is reduced. This is referred to the reduction of $P_{inj}$ occurring when $L$ is increased.

5.3.2 Experimental Results

Figures (5-8-a,b,c) and (5-9) show the simulation and experimental results of the hot carrier gate current $I_s$ as a function of the device biasing and geometry. It may be seen that $I_s$ remains null as long as $V_{DS}$ is smaller than a certain critical value $V_{DS1} = LE_C$ below which no carrier heating occurs. As $V_{DS}$ exceeds $V_{DS1}$, appreciable carrier heating takes place and $I_s$ is created and begins to increase proportionally with $V_{DS}$, becoming larger when the value of $V_{GS}$ increases and/or with shortening the channel length $L$. This is because the oxide field $E_{ox}$ increases (as $V_{GS}$ is increased) and leads, therefore, to decreased oxide trapping. This latter causes the rate of increase of $I_s$ with $V_{GS}$ to be greater with greater values of $V_{GS}$. On the other hand, the channel field $E_x$ is increased (on reducing the channel length) and consequently enhances the channel-carrier heating. As $V_{DS}$ continues to increase ($V_{DS} - V_{GS} - V_T$), $I_s$ begins to saturate and to decrease thereafter as $V_{DS}$ is increased further. This is attributed to the creation of the pinch-off region, where the normal oxide field reverses its polarity, which stops the hot electron injection and favours instead the injection of hot holes. It is observed that the values of $V_{DS}$ at which the $I_s$-peaks occur, become higher with increasing values of $V_{GS}$, which ensures that this $I_s$ behavior is related to the channel pinch-off. Excellent agreement between the measurements and modelling are observed. However, a small inconsistency appears when the channel length is smaller than 1.4μm. This is referred to the uncertainty in the pinch-off region length $\Delta l$, which appears here to be greater than the value given by the model. This problem, does not appear with longer channel MOSFETs ($L >$
Simulation of the dependence of the hot-carrier gate current density $J_g$ on the position $x$, the biasing voltages $V_{ds}$ and $V_{gs}$ and the channel length $L$ [89].
Fig (5.8-a,b,c)
Measured variation of the $I_g$ with $V_{DS}$ for different values of $V_{GS}$ and channel length $L$ [89].
Fig (5-9)
Measured variation of $I_g$ with $L$ for different values of $V_{gs}$ and $V_{ds}$ [89]
More accurate modelling of $\Delta I$ necessitates a precise modelling of the channel depth $d_o$ which, up till now, has not been given sufficient attention. This point is very important for submicronic MOSFET devices and applications. In Fig. (5-9), $I_g$ is seen to increase as the value of $L$ decreases. $I_g$ begins to saturate at $L \sim 1.4 \mu m$ and to decrease thereafter as the value of $L$ is decreased further. This is due to the reduction of the gate surface area and to the hot hole injection occurring over the pinch-off region which becomes comparable in area to that of the gate.

Simpler $I_g$ modelling has been adopted and caused the simulation to be inconsistent with measurements. Aiming at removing this inconsistency we modified the model by adding new perturbation terms (see chapter 3) which gives a good fitting between the measurements and the simulations. This method helped to determine some device parameters which have not been determined before. The mean value of the hot carrier energy $e$ at the Si-SiO$_2$ interface, the carrier mobility $\mu_{ox}$ inside the oxide layer, the critical value of the oxide field $E_{oxc}$ at which carrier heating starts are examples of these parameters.

Figure (5-10-a,b) shows the measured variation of $I_{gs}$ and the corresponding variations of $V_T$ with the injection time $t$. It is observed that $I_{gs}$ decreases ($V_T$ increases) exponentially with $t$. This behavior is attributed to the carrier trapping inside the oxide layer and the consequent building up of an oxide charge $Q_{ox}$ (see chapter 2 section (2-6)). This charge gives rise to a counteracting oxide field $E_{oxr}$ which inhibits the hot carrier transport through the oxide layer, and therefore makes $I_{gs}$ to decrease with time, while the growth of $Q_{ox}$ with time makes $V_T$ to increase proportionally with time. Straightforward analysis, based on measurement of the decay time constant of $I_{gs}$, showed that the capture cross section $\sigma_n$, $\sigma_p$ of electrons and holes respectively inside the oxide decreases as $V_{DS}$ is increased ($\sigma_n$ varies from $2\times10^{-17} cm^2$ to $0.004\times10^{-17} cm^2$ for $V_{DS}$ variation from 7V to 12.5V).

The solid lines are simulation results. The fitting of them to the experimental results
Fig (5-10-a,b)
Variation of $I_g$ (a) and corresponding variations of $V_T$ (b)
with the injection time $t$ for different values of $V_{DS}$.
helps to experimentally determine the capture cross-section area of SiO₂ (σₐ and σₚ) and characterise its dependence on the device biasing and geometry.

5.4 SUBSTRATE ACTIVITIES

The main parameters and variables relating to the substrate activities which are to be evaluated and characterised are: the hot carrier substrate current Iₛ and its related effects on the threshold voltage shift and instability ΔV₉, on the back bias effect ΔV₉, on the hot carrier distribution in MOSFET surface n(y) and on the enlargement of the channel depth dₖ. Here Iₛ is first experimentally characterised in terms of biasing voltages V₉ₛ, V ço and channel length L. ΔV₉ is also measured at different values of V₉ₛ, V ço and L by comparing I₉ₛ of long and short channel devices having the same Z/L ration. Finally ΔV₉ is deduced from ΔV₉. The ΔV₉/Iₛ curves is stablished and used to determine the substrate resistance Rₛ.

5.4.1 Experimental Results

Figure (5-11) shows the measured variation of the substrate current Iₛ with the drain to source voltage V₉ₛ for different values of the gate to source voltage V ço and channel length L. It is observed that Iₛ increases as V₉ₛ increases and Iₛ becomes larger when the value of V ço decreases and/or shorter channel length L is used. This is because mobile carriers in the channel source-region and/or those in the pinch-off region are strongly energised and undergo more impact ionization processes. At a certain V₉ₛ value, the channel field Eₓ and Eₓ in the pinch-off region increases as the channel length L is decreased, thus enhancing the ionisation constant α and leading to greater carrier multiplication. On the other hand it is found that Eₓ and Eₓ are enhanced by decreasing the channel population through decreasing the value of V ço. Figure (5-11) shows also that the rate by which Iₛ increases becomes larger at greater values of V₉ₛ. This is because the electron-hole separation caused by the surface fields
Fig (5-11)
Variation of the substrate current $I_B$ with $V_{DS}$ for different values of $V_{GS}$ and channel length $L$ (measured).

Fig (5-12)
Variation of $I_B$ with $V_{GS}$ for different values of $V_{DS}$ and $L$ (measured).
$E_x$ and $E'_x$ is enhanced at greater values of $V_{ds}$ and tends, therefore, to reduce the recombination and/or trapping probabilities in the MOSFET surface. Since the ionisation constant $\alpha$ is seen to have a greater value in the pinch-off region than in the source-region of the channel, it is expected that the rate at which $I_g$ increases with $V_{ds}$ should jump up as the device is switched from the ohmic to the saturation region of operation. This is occurring at $V_{ds} = 3V$ and $4V$ when $V_{gs} = 4V$ and $10V$ respectively as shown in Fig. (5-11).

Figure (5-12) presents the measured variation of $I_g$ with $V_{gs}$ for different values of $V_{ds}$ and $L$. It is noticed that $I_g$ increases, first, as increasing $V_{gs}$. It tends to saturate at a certain peak and begins, thereafter, to decrease as $V_{gs}$ increases further. $I_g$ is seen to be larger for increased values of $V_{ds}$ and/or for the shorter channel length $L$. Increasing $V_{ds}$ enhances the carrier multiplication by increasing the channel fields, while decreasing the channel length assists the enhancement of these fields. The increase of $I_g$ occurring first as $V_{gs}$ increases is attributed to the fact that the increase of the channel conductivity is still so small that it does not cause inhibition of the channel fields or channel carrier multiplication. Under these conditions, increase of $V_{gs}$ enhance the normal field $E_x$ which more efficiently accelerates the secondary holes towards the bottom of the depletion region where they are collected by the substrate. As $V_{gs}$ is increased further, the channel conductivity is appreciably increased so that it inhibits the channel fields $E_x$ and $E'_x$ thus weakening the ionisation and carrier multiplication. This effect of $V_{gs}$ dominates over the acceleration of holes towards the substrate, and the subsequent collection of them into the substrate.

Fitting of simulation results with measurements was done with considering the collection efficiency $\eta_b$ giving by the model elaborated in chapter 3 as fitting parameter.

Figure (5-13) shows the measured threshold voltage shift $\Delta V_T$ as a function of $V_{ds}$ for different values of $V_{gs}$ and $L$. It is clear that $\Delta V_T$ increases as $V_{ds}$
Fig (5-13)
Threshold voltage shift $\Delta V_T$ as a function of $V_{DS}$ for different values of $V_{GS}$ and $L$ (measured).

Fig (5-14)
Simulation results of the variation of $\Delta V_B$ with $V_{DS}$ for different values of $V_{GS}$ and $L$. 
increases. The rate of increase of $\Delta V_T$ with $V_{DS}$ jumps to greater values when $V_{DS}$ exceeds a certain threshold depending on the values of $V_{GS}$ and $L$. $\Delta V_T$ is also seen to be increase for smaller values of $V_{GS}$ and/or for shorter channel length $L$. The increasing of the back-bias voltage $\Delta V_R = I_b R_s$, caused when $I_b$ is increased, has the effect of decreasing the reverse biasing $V_R$ of the substrate with respect to the drain ($V_R = V_{DS} - \Delta V_B$) and channel ($V_R = \Phi_s - \Delta V_B$). It tends, therefore, to reduce the depletion-layer width $W_d$ and the charge $Q_s$ accommodated inside it. This leads to a reduced value of the device threshold voltage $V_T$. As $V_{DS}$ reaches the value at which the device is biased into its saturation region of operation, where greater ionisation and carrier multiplication is established, the rate of increase of $\Delta V_T$ as a function of $V_{DS}$ jumps to greater values. As $L$ is reduced, the channel field is enhanced which increases this rate further. These effects are also observed at smaller $V_{DS}$ values when shorter channel devices are examined.

Good selection of the capture cross-sections $\sigma_n$ and $\sigma_p$ achieve fitting of theoretical models (see chapter 3) and measurements. Other values of $\sigma_n$ and $\sigma_p$ shifts up or down the experimental points of theory.

5.4.2 Simulation Results

Figure (5-14) shows the simulation results concerning the variation of the back bias voltage $\Delta V_B = I_b R_s$ with $V_{DS}$ for different values of $V_{GS}$ and $L$. These results are deduced as explained in Chapter 3 (see eq. (3-97)) from the experimental results of Fig. (5-13). The figure shows that $\Delta V_B$ increases proportionally with $V_{DS}$ and becomes larger for smaller values of $V_{GS}$ and/or for shorter channel length $L$. This is because $I_b$ becomes larger with shorter channel devices particularly if they are biased by small gate voltages $V_{GS}$. The rate at which $\Delta V_B$ increases with $V_{DS}$ attains greater values for larger values of $V_{DS}$. This refers to the increased rate of ionisation and carrier multiplication established when the MOSFET is switched into its saturation region (by increasing $V_{DS}$ and/or decreasing $V_{GS}$). The reduction of $L$ enhances this
Figure (5-15) shows the simulation results concerning the variation of $\Delta V_B$ with $I_B$ for different values of $V_{GS}$ and channel lengths $L$. These results are deduced from Figs. (5-11) and (5-14). It is observed that the results of each channel length coincide regardless of the values of $V_{GS}$. The slopes of these curves are calculated and are used to determine the substrate bulk resistance $R_s$ as well as the reduction factor $K_r$, which is seen to agree very well with the model presented in section 3-5-2-b, ($k_r = 33\%$). However, some inconsistency between the model and measurements is observed at $I_s$ values smaller than $4 \times 10^{-7}$ A. This is because at small levels $\Delta V_B$ becomes negligibly smaller and suffers from unavoidable measurement errors resulting from the indirect technique used for the characterisation of $\Delta V_B$.

Figure (5-16) shows the surface carrier distribution $n(y)$ without taking into account the effect of the back-bias $\Delta V_B$, for two different values of $V_{GS}$ (4V and 10V). Using the same analysis we deduce the new $n(y)$ distribution when considering the presence of $\Delta V_B$. Applying the old criteria ($n (y = d_0) = n_s / 10$; with $d_0$ being the channel depth) the channel depths $d'_0$ and $d_0$ in the absence and presence of $\Delta V_B$ are determined respectively.

It is observed that $d'_0$ is always larger than $d_0$. The difference between $d'_0$ and $d_0$ shrinks with increasing $V_{GS}$. It should be pointed out here, that $n_s = n (y = 0)$ and $n (y = w_d)$ remain constant while $n(y)$ in between, increases. This leads to a modified $n(y)$ distribution which is less steep than that obtained in the absence of $\Delta V_B$. As $V_{GS}$ increases, the channel conductivity increases. This inhibits the carrier multiplication and leads to negligibly smaller values of $\Delta V_B$ which render $d_0$ not appreciably different from $d'_0$.

The circles, squares and crossing have been plotted in Figs. (5-14, 5-15 and 5-16) to distinguish between the different conditions (biasing voltage $V_{GS}$ and $V_{DS}$...
Fig (5-15)
Simulation results of the variation of $\Delta V_B$ with $I_B$ for different values of $V_{GS}$ and $L$.

Fig (5-16)
Variation of the surface carrier distribution caused due to the back bias voltage $\Delta V_B$ (simulation).
device geometry \( L, z, h_0 \), \( \ldots \) of measurements.

5.5 TRAPEZOIDAL GATE MOSFET (TG-MOSFET) CHARACTERIZATION

This section is dedicated to verifying the models which have been established in chapter 3 for the TG-MOSFET operation, and to investigating its performance. The distributions of the channel potential \( V_x(x) \), the channel field \( E_x(x) \) and the channel lateral potential \( V_z(x) \) are required to qualify the device capabilities in the cancellation of noise, leakage currents, and the effects of parasitic elements. These parameters were computer-aided characterised using simulation program designed in basic language and based on the model elaborated in Chapter 3.

5.5.1 Simulation Results

Figure (5-17) shows the simulation results of channel potential \( V_x \) as a function of distance \( x \) for different values of the channel steepness \( \beta \) (with \( V_{os} \) equal to 15V). It is observed that the \( V_x \) curve is depressed below that which corresponds to the RG MOSFET. Its depression increases as the channel steepness \( \beta \) is increased. The channel potential besides the source is consequently decreased, which results in a smaller channel current and device dissipation.

Figure (5-18) shows the simulation results of channel field distribution \( E_x \) as a function of the position \( x \), for different values of \( \beta \) and \( V_{os} \). It may be seen that \( E_x \) increases with distance \( x \). It is enhanced near the drain and increased over the value which is expected to be obtained with an RG MOSFET. The field enhancement becomes larger for increased values of the steepness \( \beta \). This field enhancement causes greater carrier heating. It results therefore in a gate current \( I_g \) which is more than two decades greater than that which could be obtained with an RG MOSFET of the same dimensions operated under the same biasing conditions. However, the
Fig (5-17)
Variation of the channel potential $V_x$ with distance $x$ for different values of the channel steepness $\beta$ (simulation).

Fig (5-18)
Variation of the field $E_x$ with the position $x$, for different values of $\beta$ and $V_{GS}$ (simulation).
The simulation results of Fig.(5-17) and (5-18) are necessary for the evaluation and characterisation of the distribution of the lateral potential $V_z$ and field $E_z$.

Figure (5-19) presents the simulation results of $V_z$ versus distance $x$ at different values of steepness $\beta$. The Figure shows that $V_z$ increases with the distance $x$. It is increased for larger values of $\beta$ and/or $V_{GS}$.

### 5.5.2 Experimental Results

Figure (5-20) shows the measured variation of the leakage current $I_L$ with the gate voltage $V_{GS}$ for different values of steepness $\beta$. It is observed that $I_L$ increases as $V_{GS}$ increases. This is because increasing $V_{GS}$ enhances the normal field $E_y$ and causes injection of secondary holes, created due to multiplication, into the substrate, which increases the device leakage current. Larger values of $\beta$ cause the channel barrier-well due to gate steepness to increase which reduces the injection of secondary holes and causes $I_L$ to decrease. However, increasing $\beta$ means smaller drain and channel geometries. These reduced geometries lead to smaller value of $I_L$ even when carrier multiplication is not dominant.

The solid lines are not simulation results and they are plotted only to clarify the direction of variation of $I_L$.

Figure (5-21) shows the variation of the gate current density $J_g$ with the steepness $\beta$ for different values of channel length $L$ and gate voltage $V_{GS}$. It is observed that $J_g$ increases as $\beta$ increases. $J_g$ is larger for shorter channel lengths and/or increased gate voltages. This is caused by a stronger field enhancement, which
Fig (5-19)
Simulation results of $V_Z$ versus distance $x$ at different values of $\beta$. 

Fig (5-20)
Variation of the leakage current $I_L$ with $V_{GS}$ for different values of $\beta$ (measured).
Fig (5-21)
Variation of the gate current density $J_g$ with $\beta$ for different values of $L$ and $V_{GS}$ (measured).

Fig (5-22)
Variation of $J_g$ with $L$ for different values of $V_{GS}$ (measured).
occurs in shorter channels at greater gate voltages. Increased gate voltages also decrease the oxide trapping and leads, therefore, to a greater value of $J_g$. It is also observed that the rate at which $J_g$ increases with $\beta$ is smaller in shorter-channel MOSFETs. This is owing to the background carrier heating occurring in short channels even if these channels are not trapezoidal. The carrier heating in short-channel, TG MOSFETs ($L \leq 2\mu m$) is due to the short-channel effect together with the channel steepness. Where it is attributable to channel steepness in the long-channel TG MOSFETs ($L \geq 5\mu m$), then $J_g$ increases more steeply with $\beta$.

Figure (5-22) shows the measured variation of $J_g$ versus the channel length $L$ for different values of gate voltage $V_{GS}$. It is seen that $J_g$ increases as $L$ decreases. $J_g$ increases for larger values of $V_{GS}$. This is because greater carrier heating and smaller oxide trapping are maintained in these devices.

The difference between simulation and measurements of Figs.(5-21 and 5-22) shrinks to less than 2% because proper device parameters values are used ($\mu_{oxp}=4cm^2/V.Sec$, $\mu_{oxn}=41cm^2/V.Sec$, $E_{oxc}=2.1\times10^8$ V/m and the hot carrier mean energy $\epsilon=4.2$ ev).

5.6 NOISE REDUCTION

Numerous measurements and simulations have been performed to specify and evaluate the device noise level and to qualify the reduction capability and dependence of its potential on the device gate form (topological). Here the attention is focussed on the noise reduction factor $\chi$ (see theory of Chapter 3). The solid lines on simulation curves are used as guide while those noticed on the experimental curves represent the theoretical evaluation. In this latter complete fitting is observed because proper values of the fitting parameters have been used.
5.6.1 Simulation Results

In all following simulation curves, circles, triangles and crosses are used to distinguish between the different measurement conditions.

Figure (5-23) shows the simulation results (related to trapezoidal gate device) of variation of the trans-conductance-reduction factor $\chi$ with the ratio $Z_d/Z_0$ with different values of $n$ ($n$ is the index of steepness). It is observed that $\chi$ decreases as $Z_d/Z_0$ increases (in other words as the gate-sides steepness increases). It is also noticed that $\chi$ decreases when the value of $n$ increases. This is due to the reduction of the channel width caused by the increase of the pinch-off region length $\Delta l$, which becomes more appreciable with larger values of $n$ and/or $Z_d/Z_0$ ratio.

Figure (5-24) shows the simulation results of the dependence of $\chi$ on the gate biasing-voltage $V_{GS}$, the ratio $Z_d/Z_0$ and the index of the gate sides steeping $n$. It reveals that $\chi$ decreases as $Z_d/Z_0$ and/or $n$ are increased and $\chi$ becomes smaller for smaller values of $V_{GS}$ (and/or the greater the value of the drain biasing voltage $V_{DS}$). This is due to the fact that with smaller values of $V_{GS}$ the pinch-off region length $\Delta l$ becomes greater and tends to reduce the width $Z_L$ of the channel near the drain, thus corresponding consequently to smaller values of $Z_d/Z_0$. The increase of $V_{DS}$ assists this behavior and reduces $Z_L$ further.

Figure (5-25-a,b,c,d) show the simulation results of the variation of $\chi$ with the channel length $L$ at different values of the ratio $Z_d/Z_0$ and the index of the gate sides steeping $n$. These results reveal that $\chi$ decreases as the channel length $L$ is decreased. It becomes smaller with larger values of $n$ and/or smaller values of $Z_0$ (when $Z_L$ is kept constant). This new feature makes the MOSFET absolutely compatible with the scaling-down trends from the noise-level point of view, a factor which has, for a long time, been a serious limitation restricting the device geometry.
Fig (5-23)
Variation of transconductance $\chi$ with $Z_L/Z_0$ at different values of the index of steepness $n$ (simulation).

Fig (5-24)
Shows the dependence of $\chi$ on $V_{GS}$, $Z_L/Z_0$ and the index of steepness $n$ (simulation).
Fig (5-25-a,b,c,d)
Variation of $\chi$ with $L$ at different values of $Z_L/Z_0$ and $n$ (simulation).
scaling-down below certain dimensions. In the case of the device geometry being reduced too far, the noise-level increases too much and the device becomes non-operational and cannot be used any more for most applications. However, the trapezoidal gate form successfully solves this problem and makes it possible to realise submicronic MOSFETs \( L \sim 0.1\mu m \) associated with negligibly small noise levels (compared to traditional MOSFETs having the same channel length).

Figure (5-26) shows the simulation results of the variation of \( \chi \) with the ratio \( Z_L/Z_0 \) at different values of the channel length \( L \) and the gate sides steepness index \( n \). From this it may be observed that \( \chi \) undergoes the same behavior explained by Fig. (5-25-a,b,c,d). In addition, it shows that \( \chi \) increases as decreasing \( Z_L \) (\( Z_0 \) kept constant) until it attains its maximum value \( \chi_{\text{max}} = 1 \) when \( Z_L \) becomes equal to \( Z_0 \) (i.e.; when the device becomes a rectangular gate MOSFET). On the other hand, when \( Z_L \) is kept constant, \( \chi \) decreases as \( Z_0 \) increases, which means that complicated technology of fabrication is needed.

Figure (5-27) demonstrates the simulation results of the variation of \( \chi \) with \( Z_L \) at different values of \( Z_0 \). It is observed that \( \chi \) decreases as \( Z_L \) increases and \( \chi \) becomes smaller with smaller values of \( Z_0 \). This may be attributed to the increased gate side steepness which consequently renders the channel width reduction near the drain \( \Delta Z_L \) more sensitive to the variations of the pinch-off region length \( \Delta l \).

This results of simulation indicate that the new technique completely cancels the channel-length modulation noise (CLM) and reduces the \( I/f \) and thermal noise by at least a factor of 100. This factor may be increased as further geometry scaling-down is adopted.
Fig (5-26)
Variation of $\chi$ with $Z_L/Z_0$ at different values of $L$ and $n$.

Fig (5-27)
Variation $\chi$ with $Z_L$ at different values of $Z_0$ (simulation).
5.6.2 Experimental Results

Figure (5-28-a,b) shows the measured variation of the transconductance \( g_m \) with the gate voltage \( V_{gs} \) at different values of \( V_{ds} \) and \( \beta \). It is observed that in both cases of \( \beta = 2.5 \) (TG-MOSFET) and \( \beta = 0 \) (RG-MOSFET) \( g_m \) increases first, as \( V_{gs} \) is increased until a certain critical value of \( V_{gs} \) (\( V_{gsc} \)) is reached, at which \( g_m \) saturates and begins to decrease thereafter when \( V_{gs} \) is increased further. The value of \( V_{gsc} \) depends on the value of the applied drain voltage \( V_{ds} \) (\( V_{gs} \) increases as \( V_{ds} \) increases). This behavior is attributed to the initial increase of the channel conductivity with \( V_{gs} \) (\( V_{gs} < V_{gsc} \)). However the subsequent reduction of the channel conductivity occurring when \( V_{gs} \) exceeds the critical value \( V_{gsc} \) is referred to the following mechanisms.

a) The mobility degradation due to the gate electrode effect. This effect becomes smaller the greater the value of \( V_{ds} \), which explains why \( V_{gsc} \) increases as \( V_{ds} \) is increased and why \( g_m \) becomes bigger with increased values of \( V_{ds} \).

b) When the mobile carrier density \( n \) in the channel increases over a certain value \( n_c = 10^{18}/\text{cm}^3 \), carrier-carrier collisions become appreciable and momentum exchange between carriers is enhanced. The process decreases further the channel mobility and leads to a decreasing channel conductivity.

It was also observed that \( g_m \) of the TG-MOSFET of, \( \beta = 2.5 \) is more than one decade smaller than that of the RG-MOSFET of \( \beta = 0 \), which appears to agree closely with the theory.

The solid lines are not simulation results and are only drawn to study the behaviour of \( g_m \) variation. However the experimental points gives a very good qualitative agreement with the MOSFET theory.

Figure (5-29) investigates the I/V characteristics of the test devices having \( \beta \) equals to -2.5 (reversed TG-MOSFET), to zero (RG-MOSFET) and to 2.5 (proposed
Fig (5-28-a,b)  
Variation of the transconductance $g_m$ with $V_{GS}$ at different values of $V_{DS}$ and $\beta$ (measured).
Fig (5-29)

$I_{DS}/V_{DS}$ characteristics of the test devices.
TG-MOSFET) with \( n = 1 \) for all. The Figure shows that \( I_{DS} \) becomes very smoothly constant, in the saturation region \( V_{DS} \geq V_{DSS} \) and independent of the \( V_{DS} \) variations in the last one, since the channel length modulation caused by the gate voltage fluctuations has been completely cancelled by the induced counteracting fluctuations of the channel width near the drain \( Z_L \) owing to the trapezoidal form of the gate. However, no drain-current fluctuations take place even with high level \( V_{GS} \) fluctuations. On the other hand, \( I_{DS} \) in the RG-MOSFET (second case) increases appreciably with \( V_{DS} \), which means that \( V_{GS} \) fluctuations are transferred to the channel and cause \( I_{DS} \) to undergo a proportional fluctuation. However, \( I_{DS} \) in the reversed TG-MOSFET ( \( \beta = -2.5 \) ) acquires a greater rate of increase with \( V_{DS} \) because additional mechanisms interact (impact ionisation and subsequent carrier multiplications), thus causing \( I_{DS} \) to be severely sensitive to the \( V_{GS} \) fluctuations.

At smaller values of \( V_{GS} \) with the device biased in the ohmic region, \( I_{DS} \) of the reversed TG-MOSFET ( \( \beta = -2.5 \) ) remains smaller than \( I_{DS} \) of both RG and TG-MOSFETs. When \( V_{GS} \) is increased an appreciable channel field enhancement has occurred, which causes the carrier heating in the channel. In this case carrier multiplication by impact ionisation is also enhanced (during the operation of the device in the ohmic region), which pushes \( I_{DS} \) over that value observed in the RG-MOSFET.

The solid lines here are simulation except near multiplication regions (triangles at \( V_{DS} \geq 14V \)) where the I/V device model becomes no longer valide. Fitting of the experimental points with theory helps to extract the proper device parameter values (\( \mu_n = 600 \text{ cm}^2/\text{V} \cdot \text{Sec} \), \( \mu_p = 400 \text{ cm}^2/\text{V} \cdot \text{Sec} \), \( V_T = 3V \) for rectangular devices, \( 3.5V \) for trapezoidal with narrow width at the drain and \( 2.5V \) trapezoidal with wide width at the drain). When very great number of devices are examined, nominal values and standard deviations of parameters can be specified.

Figures (5-30-a,b) show the gate voltage noise spectrum \( S_{V_g} \) and the
Fig (5-30-a,b)
The gate-voltage noise-spectrum $S_{V_g}$ and the drain current noise spectrum $S_{i_{DS}}$ in both RG and TG MOSFET's.
corresponding drain current noise spectra \( S_{I_{ds}} \) um in both RG and TG-MOSFETs. It is observed that the TG-MOSFET (\( \beta = 2.5 \) and \( n = 1 \)) is associated with a 1/f noise spectrum which is about two decades weaker than that of the RG-MOSFETs. Greater reduction of the 1/f and thermal noise can be achieved when optimising \( \beta \) and \( n \) to their most desirable values. However, no CLM noise was observed even at high drain biasing voltages (\( V_{ds} \sim 6 \) to 14V, \( V_{gs} = 4V \)).

The solid lines in Fig. (5-30-a,b) are not simulation and are drawn to study the behaviour of \( S_{V_{g}} \). \( S_{V_{g}} \) have been measured by short circuiting the device gate to source leads and measuring the resulting drain voltage after being amplified by a noise free high gain amplifier in conjunction with a spectrum analyser.

5.7 X-RAY AND UV IRRADIATION

The following results are all experimental and solid lines are only used to clarify the behaviour of variation. All experimental details and background theory have been given in Chapter 4. A great number of devices have been examined and showed very good consistency. As will be shown below the behaviour of these results is very useful in declaring the role of action of X-ray and UV on the MOSFET characteristics and performance related to the interface and oxide defects generation and kinetics. It should be pointed out here that all irradiation measurements were performed at room temperature and all devices were not biased during irradiation.

5.7.1 Stressing by X-Ray Irradiation

Figs.(5-32) show the measured variations of the threshold voltage \( V_T \) for test devices irradiated by X-ray. \( V_T \) is shown to increase to a saturated value as the stressing time \( t \) increases and the threshold voltage shift \( \Delta V_T \) becomes greater the
Fig (5-32)
Variation of the threshold voltage $V_T$ with the stressing time $t_{st}$ at different X-ray radiation levels (measured).
greater the level of the X-ray power.

Figs. (5-33-a,b,c,d) present the measured variations of the channel mobility \( \mu_{st} \) caused by stressing and show that \( \mu_{st} \) first increases, as the stressing time \( t' \) increases, until \( \mu_{st} \) attains a maximum value at a certain value of \( t' \) (depending on the X-ray power). Afterwards \( \mu_{st} \) begins to saturate or to decrease as increasing further \( t' \).

Fig. (5-33) shows the dependence of the stressed mobility \( \mu_{st} \) on the value of the drain voltage \( V_{DS} \) at which \( \mu_{st} \) is measured after stressing by different X-ray beam power (0.2 and 0.4kVA). It was observed that the peak value of \( \mu \) occurs at shorter stressing time as the value of \( V_{DS} \) increased. This is explained as follows: When \( V_{DS} \) increases the surface state energy levels are shifted below the quasi-fermi level which depopulate it from carriers \( (dQ_p/d\Phi \) decreases) which corresponds to a greater value of \( \mu \) (see model of section 3.8).

Fig. (5-34) shows the measured variation of the device \( 1/f \) noise with the stressing time \( t' \).

Since the variation of the channel mobility and the generation of the \( 1/f \) noise relates to the interaction of the channel mobile carriers with fast states (see section 3.8), then it can be concluded from these results that the X-ray and the UV stressing adds fast surface states besides the introduction of the slow states. The introduced fast states tends to increase the noise with \( t' \) as experimentally investigated. It is also noticed a tendency of saturation of the noise with \( t' \) which indicates that all available bonds are defected.

5.7.2 Stress by UV Irradiation - Experimental Results

This section explains the effects of UV irradiation on MOSFET performance
Fig (5-33-a)
Variation of the channel mobility μ with the stressing time \( t_{st} \) at different x-ray radiation levels (measured).

Fig (5-33-b)
Variation of μ with \( t_{st} \) at different values of the drain voltage \( V_{DS} \) at 0.6 KVA X-ray radiation level (measured).
Variation of $\mu$ with $t_{st}$ at different values of the drain voltage $V_{DS}$ at 0.4 kVA X-ray radiation level (measured).

Variation of $\mu$ with $t_{st}$ at different values of the drain voltage $V_{DS}$ at 0.2 kVA X-ray radiation level (measured).
Fig (5-34)
Dependence of the noise voltage and current spectrums $S_{Vg}$ and $S_{Ig}$ on the stressing time $t_{st}$ (measured).
and operation and also presentation of new theoretical modelling. The matching of this theory with experimental results helps to characterise the behaviour of the MOSFET parameters under the influence of the UV radiation.

Figure (5-35) shows the variation of the threshold voltage $V_T$ with time during annealing by UV irradiation. Three different radiation intensities are considered, 30mW/cm$^2$, 90mW/cm$^2$ and 180mW/cm$^2$. It is observed that $V_T$ decreases exponentially with time. The decay time-constant $\tau$ becomes shorter as the UV radiation intensity $I_r$ is increased. This is because a greater number of photons and/or a greater energy carried by each photon are expected to be obtained as increasing $I_r$. Also the energy capture cross-section area of broken or dangling bonds becomes greater the greater the photon energy and/or the number of photons. The steady state value of the annealed $V_T$ is seen to be smaller the greater the value of $I_r$. This is because a greater number of broken and dangling bonds retain their steady state energy and those carriers which were trapped have been excited out of these bonds. These measurements have been performed on many of test samples (TG MOSFET of 4$\mu$m channel length).

Fig (5-36) shows the variation of $V_T$ with the time $t$ when the test samples are stressed by X-ray radiation and subsequently annealed through exposure to UV radiation. Three successive cycles are considered.

It is observed that the rate at which $V_T$ strains is greater during the first cycles and gets smaller thereafter. This is related to the dangling bonds whose number increases as the number of cycles is increased and which need greater photon energy to be cured.

It is also noticed that $V_T$ changes its initial value at an exponential rate which is seen to be nearly constant irrespective of the number of cycles. However, $V_T$ attains
Fig (5-35)
Variation of the threshold voltage $V_T$ with time during annealing by UV irradiation at different values of $I_r$ (measured).
Fig (5-36)
 Variation of $V_T$ with time $t$ and number of stressing (by X-ray) / annealing (by UV) cycles $n$ (measured).
a residual value $\Delta V_T$ which is seen to increase with the number of cycles and indicates the fact of creation and increasing of the number of dangling bonds.

5.8 MAGNETIC PROPERTIES

The magnetic properties of MOSFETs can be investigated through measurements of the reduction in the channel current caused due to lateral leakage occurring due to the transversal magnetic force. Samples which are shown in Figs. (4-14-a,b) is used to perform these measurements. To increase the sensitivity and accuracy to this feature, the splitted drain MOSFET shown in Fig. (4-15) is used. Hall voltage and magnetoresistance measurements are also performed on $p$ type GaAs thin films (Fig. (4-13)). The magnetic properties of RG- and TG MOSFETs will be considered. Fig. (4-10) shows the experimentaly set-up.

In what follows all the results obtained are experimental and solid lines are used to clarify the behaviour of variation and to enable to affect some regression and deduce values of new unknown parameters (reduction time $\tau$, trapping capture cross section $\sigma$ are examples of parameters).

5.8.1 Thin Films

Some thin films of amorphous GaAs were investigated as offering some guidance as to what may be expected with MOS configured silicon devices.

Figure (5-37-a,b) shows the variation of the Hall voltage with the longitudinal current $I_x$ for different values of the magnetic current $I_m$, with and without light exposure (light intensity $I_r=0.9\text{mW/cm}^2$). It is observed that $V_H$ first increases linearly with $I_x$. When $I_x$ exceeds a certain value (depending on the operating magnetic field) $V_H$ begins to saturate. $V_H$ becomes larger with an increased magnetic current $I_m$. The value of $I_x$ at which $V_H$ begins to saturate increases as $I_m$ is increased. The observed
<table>
<thead>
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<th>$V_H$ (mV)</th>
<th>Dark</th>
<th>$a$-GaAs</th>
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<td></td>
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Fig (5-37-a,b)

Variation of the Hall voltage $V_H$ with the longitudinal current $I_x$ for different values of the magnetic current $I_m$ with and without exposure (measured).
saturation may be attributed to the increased conductivity due to appreciable carrier injection. Under this condition, charge separation fails and carriers can flow easily from points of greater accumulation to those of smaller accumulation which inhibit $V_H$ from increasing linearly with $I_x$. It should also be pointed out that the carrier lifetime is greatly shortened under high current injection into the test sample (high injection lifetime $\tau_{ih}=10^{-9}$ Sec) while the low injection level lifetime $\tau =10^{-9}$ Sec. This important reduction of $\tau_{ih}$ enhances the occurrence of carrier disappearance in recombination and trapping thus inhibiting further the increase of $V_H$ with $I_x$. On the other hand $I_m$ enhances the increase of $V_H$ which manifests itself in shifting up the value of $I_x$ at which $V_H$ begins to saturate.

Figure (5-38-a,b) presents the variation of $V_H$ with the magnetic current $I_m$ for different values of $I_x$ with and without light exposure. It will be noticed that $V_H$ first increases proportionally with $I_m$ as long as $I_m$ is smaller than a certain value (which is not dependent on the value of $I_x$). Over this limit $V_H$ begins to attain some tendency towards saturation. This phenomena may be related to the internal magnetisation of the thin film and the consequent reduction of the effective value of the applied magnetic field density. It should also be noticed that the interaction of the strong magnetic field with the thin film spatial lattice generates a greater number of optic and acoustic phonons (field induced lattice vibrations). The interaction of these phonons with the mobile carriers reinforces the disappearance of these carriers in recombination and trapping which assist the saturation of $V_H$ with $I_m$. On the other hand, the strong magnetic field shifts the carriers more strongly towards the sample edge where greater densities of the structural defects and broken bonds exist, and provide a media in which greater recombination and trapping is expected.

Figure (5-39-a,b) investigates the dependence of $V_H$ on the light exposure. It is observed that $V_H$ becomes smaller when the sample is exposed even to white light. The amount of reduction of $V_H$ is seen to be larger for smaller values of the magnetic
Fig (5-38-a,b)
Variation of $V_H$ with the magnetic current $I_m$ for different values of $I_x$ with and without light exposure (measured).
Fig (5-39-a)
Variation of $V_H$ with $I_x$ at different values of $I_m$ with and without light exposure (measured).

Fig (5-39-b)
Variation of $V_H$ with $J_m$ at different values of $J_x$ with and without light exposure (measured).
field \( B \) (\( I_m \) is taken as a measure of \( B \)) and/or for larger values of the longitudinal current \( I_x \). This behavior may be attributed to the photo-generation of carriers and the consequent reduction of the sample resistivity. This tends, in turn, to inhibit the charge separation and to excite more trapping and recombination. This last effect regeneratively decreases the charge accumulation and gives rise to a smaller Hall voltage \( V_H \).

As \( I_m \) decreases the charge separation capability decreases which upsets the balance in favour of trapping and recombination. On the other hand greater values of \( I_x \) lead (for constant \( I_m \)) to greater accumulation capability.

Figure (5-40) illustrates the decay of \( V_H \) with time for different values of the magnetic field density \( B \) (as indicated by the corresponding magnetic current \( I_m \)) with \( I_x \) as a parameter. It will be noticed that the decay of \( V_H \) with time becomes larger for increased values of \( I_x \) and/or the smaller values of \( I_m \). This is due to the increase of \( I_x \), which means an enlarged level of carrier injection causing in turn a shorter lifetime \( \tau \), and greater capture cross section \( \sigma \). Both of these effects allows \( V_H \) to decay more rapidly with time. On the other hand the decrease of \( I_m \) leads to smaller charge separation capability which means greater probability of recombination and trapping.

Figure (5-41) shows the decay of \( V_H \) with time \( t \) in the absence of light source. In comparison with Fig. (5-40), it is observed that \( V_H \) decays more rapidly with \( t \) in the presence of a light source due to the photogeneration of carriers and the consequent reduction of the lifetime \( \tau \). Also random collisions between carriers, enhancing their number by the irradiation process, increase also the probability of trapping and recombination.

Fig. (5-42-a,b) presents the magneto-conductivity \( \sigma_m \) as a function of \( I_x \) and \( I_m \). It is observed that \( \sigma_m \) increases as \( I_x \) and/or \( I_m \) increases. The rate of increase of
Decay of $V_H$ with time for different values of the magnetic field density $B$ with $I_x$ as a parameter.

Decay of $V_H$ with time $t$ for different values of $I_x$. 

Fig (5-40)

Fig (5-41)
Fig (5-42-a,b)
Dependence of the magnetoconductivity $\sigma_m$ on $I_x$ and $I_m$. 

$\sigma_m (\mu / \text{cm})$

GaAs
$\sigma_0 = 25.6 \mu / \text{cm}$

$I_m$: 5 A, 2 A, 1 A

$I_x$: 70 mA

$I_m$: 60 mA

$I_m$: 50 mA

$I_m$: 40 mA
σ_m with \( I_x \) increases for larger values of \( I_x \) and/or smaller values of \( I_m \). This is because the increase of \( I_x \) gives rise to a greater charge separation force which accelerates the carriers more rapidly in the transversal direction. On the other hand the increase of \( I_m \) shifts the carriers more strongly towards the sample edges where the densities of structural defects and broken bonds are greater. The trapped charge establishes a counteracting transversal field which pushes back the magnetically accelerated carriers, and therefore decreases the rate of increase of \( \sigma_m \) with \( I_m \).

Figure (5-43) shows the variations of the capture cross section area \( \sigma \) of the trapping centres as a function of the transversal current density \( J_x \) for different values of the magnetic current \( I_m \) and longitudinal current \( I_x \). These results are deduced from Figs. (5-41) and (5-42). It is observed that \( \sigma \) decreases as \( I_x \) and/or \( I_m \) increases. This is because the transversal magnetic force, which separates the carriers far from the positive charge of traps or far from the potential wells of the empty traps, increases proportionally with \( I_x \) and/or \( I_m \). This leads to smaller probability of trapping and recombination. It leads, in other words, to much a longer lifetime which corresponds to much smaller values of \( \sigma \). The longitudinal electric field caused by the longitudinal current \( I_x (E_x = \rho J_x) \) plays the same part in separating the charge and lengthening the lifetime.

Figure (5-44) shows the global behavior of the \( V_H \) variation with \( I_x \) for different values of \( I_m \). It will be noticed that \( V_H \) first increases proportionally with \( I_x \) and continues to increase up to a certain value of \( I_{xsa} \) above which it begins to saturate then decreases thereafter when increasing further \( I_x \). This value \( I_{xsa} \) increases as increasing the value of \( I_m \). \( V_H \) saturation is referred to the charge accumulation and the consequent shortening of the carrier lifetime. These reduced values of \( \tau \) lead to a larger number of recombination processes owing to which the carrier accumulation rate is inhibited. On the other hand the decrease of \( V_H \) with \( I_x \) is caused by the ohmic potential difference \( \Delta V_x \) between the two Hall contacts (as pointed out in chapter 3
Fig (5-43)
Capture cross section area $\sigma$ of the trapping centers as a function of the transversal current density $I_y$ for different values of $I_m$ and $I_x$. 

GaAs
$t=1.5 \mu m$
$w=4 \text{ mm}$
$I_r=0.9 \text{ mw/cm}^2$
Fig (5-44)
Global variation of $V_H$ with $I_x$ for different values of $I_m$. 
section 3.9). This potential, which increases linearly with $I_x$, should be subtracted from the value of $V_H$.

It is also observed that, for a larger value of $I_x (I_{rel})$, the variation of $V_H$ curves with $I_x$ is no longer linear. It is noticeable that $V_H$ decreases more rapidly with $I_x$ than may be expected. In other words $I_x$ acquires values which are smaller than those which we expect to obtain at the same $V_H$ values. In this case $I_x$ decreases due the deviation of the $I_x$ current stream and the escape of a fraction of ($I_y$) in the transversal direction. This effect is termed magneto-conductivity (the conductivity in the transversal direction $\Delta \sigma_m$ caused by the magnetic force). The difference $\Delta I_x$ between the actual and expected values of $I_x$ increases as $I_m$ increases. This is due to the fact that larger values of $I_m$ cause more transversal current $I_y$ to escape upward.

5.8.2 MOSFETs

Figure (5-45) shows the reduction $\Delta I_{DS}$ in the drain current $I_{DS}$, caused by the influence of the transversal magnetic force, as a function of the drain voltage $V_{DS}$ for different values of the magnetic current $I_m$ and the gate voltage $V_{GS}$. These results were obtained using the experimental set-up shown in Fig. (4-1).

It is observed that $\Delta I_{DS}$ decreases first with increasing $V_{DS}$ and attains its minimum value at a certain value of $V_{DS}$. When increasing $V_{DS}$ further over this value $\Delta I_{DS}$ begins to increase proportionally with $V_{DS}$. $\Delta I_{DS}$ tends to saturate as $V_{DS}$ gets much larger. It is also noticed that $\Delta I_{DS}$ increases for larger values of the magnetic current $I_m$ and/or the gate voltage $V_{GS}$.

The valley-like variation of $\Delta I_{DS}$ with $V_{DS}$ is related to the variation of the channel depth $d_0$ with $V_{DS}$ (see Figs. (5-1) and (5-2)). The saturation of $\Delta I_{DS}$ is due to the increased acceleration of the carriers towards the drain and the reduction of
Drain variation of $\Delta I_{DS}$ caused due to the transversal magnetic force, with the voltage $V_{DS}$ for different values of $I_m$ and $V_G$. 

Fig (5-45-a,b)
their flight time through the channel where the transversal magnetic force is acting. In this case only a smaller fraction of $\Delta I_{DS}$ is transversally shifted and succeeds in escaping from the channel well. On the other hand this fraction increases as $I_m$ increases. The effect of $V_{GS}$ can be explained as follows: as $V_{GS}$ increases $d_s$ decreases and leads to greater values of $\Delta I_{DS}$. On the other hand, the increase of $V_{GS}$ leads to an increased channel population which allows larger values of $\Delta I_{DS}$.

Figure (5-46-a,b) presents the drain current reduction $\Delta I_{DSR}$ and $\Delta I_{DST}$, respectively for the rectangular and trapezoidal gate MOSFET (RG-MOSFET and TG-MOSFET), with $I_{DS}$ for different values of $V_{GS}$ ($I_m$ maintained constant and equal to 18 A). Here the values of $V_{DS}$ are so chosen that the longitudinal channel field exceeds a critical value $E_c$ over which carrier heating takes place ($E_s > E_c$, $E_c = 1.5 \text{ V/\mu m}$ for electrons and $2\text{ V/\mu m}$ for holes).

It is noticed that both $\Delta I_{DSR}$ and $\Delta I_{DST}$ decreases as $V_{DS}$ increases. They become larger for larger values of $V_{GS}$. However, for all values of $V_{GS}$ and $V_{DS}$, $\Delta I_{DST}$ is seen to be about two times smaller than $\Delta I_{DSR}$.

The decrease of $\Delta I_{DSR}$ and $\Delta I_{DST}$ is attributed to the reduction and degradation of the carrier mobility caused by the high field carrier heating. This effect reduces the response of carriers to the applied magnetic field and decreases the angle of deviation during carrier transport from the source to the drain.

The creation of the lateral channel field $E_s$ (pointing into the interior of the channel well) in the TG-MOSFET (see chapters 3) makes it more difficult for the electron to escape from the channel. This effect makes $\Delta I_{DST}$ appear to be smaller than $\Delta I_{DSR}$.

The increase of both $\Delta I_{DSR}$ and $\Delta I_{DST}$ with $V_{GS}$ is due to the greater population
Fig (5-46-a,b)

Variation of $\Delta I_{DS}$ respectively in the rectangular and trapezoidal gate MOSFET's with $V_{DS}$ for different values of $V_{GS}$. 

RG MOSFET
$Z = 250 \mu m$
$L = 4 \mu m$
$h_o = 450 \mu A$

TG MOSFET
$Z_0 = 250 \mu m$
$L = 4 \mu m$
$h_o = 450 \mu A$
of the channel and the resultant greater number of carriers which may probably escape from the channel.

These results have been obtained from measurements performed on a large number of TG and RG MOSFET samples using the experimental setup shown in Fig. (4-14).

Figure (5-47) shows the variation of the Hall voltage \( V_H \) caused by deviation of the two drain currents of a split MOSFET \( D_1 \) and \( D_2 \) with \( V_{GS} \) for different values of the gate voltage \( V_{DS} \) (at a magnetic current \( I_m = 18 \) A). These results are obtained using the experimental set-up of Fig. (4-15). It is observed that \( I_{DS1} = I_{DS2}/2 \) when \( I_n = 0 \). As \( I_n \) increases, \( I_{DS1} \) increases while \( I_{DS2} \) decreases. The amounts of variation for \( I_{DS1} \) and \( I_{DS2} \) become larger as the value of \( I_n \) increases. Both \( I_{DS1} \) and \( I_{DS2} \) increase proportionally with \( V_{DS} \). At very small values of \( V_{DS} \) no reproducible difference between \( I_{DS1} \) and \( I_{DS2} \) is observed.

This behavior of \( I_{DS1} \) and \( I_{DS2} \) causes one split (see Fig. (4-15)) to accumulate a greater number of electrons than the other, thus generating a potential difference between the two splits. This potential, \( V_H \), is amplified and measured. It is observed that \( V_H \) increases as \( V_{GS} \) increases and becomes larger with smaller values of \( V_{DS} \). This is due to the fact that the electron drift increases with \( V_{DS} \) and tends therefore to reduce the probability of deviation in response to the Hall force. However, at very small values of \( V_{DS} \) (smaller than 8V) the gate electrode effect further decreases the deviation (in response to the Hall force) of electrons.

5.9 CONCLUSIONS

The experimental and simulation results concerning the characterisation of RG and TG MOSFETs as well as those of thin films have been presented. Very good
Variation of $V_H$ with $V_{GS}$ for different values of $V_{DS}$. 

Fig (5-47)
qualitative and quantitative agreement have been observed between theory and measurements. Simulation programs have been used which have taken into account the effects of the device geometry, the biasing conditions and the technology of fabrication. The measurements have been performed on a number of test samples (a-GaAs thin films and Si MOSFETs). A-GaAs thin films of 1.5 μm thickness and 4 mm lengths were used, and RG and TG MOSFET samples of lengths L, widths Z and oxide thickness h₀ ranging respectively from 0.5 to 4 μm, 3 to 250 μm and 450 to 1200 A₀ were used. Also, short channel MOSFETs of L, Z and h₀ ranging respectively from 10-0.5μm, 100-3μm, 1200-450 A₀ have been used to perform the carrier heating measurements. Very interesting results have been obtained with regard to the carrier heating phenomena and their effect on the hot carrier energy distribution and its dependence on the electric and magnetic fields in MOSFET VLSI. A new type of study has been carried out involving stressing and/or annealing by the use of X-ray, UV radiation as well as high voltages. All the proposed theoretical models have been successfully verified by experiments.
CHAPTER 6
GENERAL CONCLUSIONS
The research described in this thesis represents a new contribution to the formulation and modelling of the different phenomena related to the carrier heating and its effects on RG and TG MOSFET devices. In order to remove many discrepancies between theory and experimental data a perturbation term had to be added to the expression of the energy distribution. Herewith, the observed hot-carrier heating phenomena could be adequately described.

The work of the thesis shows a great need for precise evaluation of the channel depth $d_0$ and pinch-off region length $\Delta l$ otherwise serious discrepancies will arise between theory and measurements. Values of $d_0$ and $\Delta l$ given by literature are much smaller than those which were experimentally investigated in this work. To perform phenomenological simulations, two models based on channel and oxide activities have been elaborated and used to evaluate and predict the values of $d_0$ and $\Delta l$.

An accurate modelling and characterization of the channel, the oxide and the substrate activities in MOSFET have been given in Chapter 3. The channel activities are related to the channel current and the threshold voltage and their dependence on biasing conditions. The latter two activities are related to the hot carrier gate and substrate currents.

Related measurements revealed that a gate current $I_g$ ranging from $10^{-14}$ to $10^{-9}$ A may be obtained with MOSFET of channel lengths as small as $2\mu$m. Channel depth $d_0$ varying from 30 to 200 Å has also been investigated. Moreover the measurements concerning the substrate activities have demonstrated that a substrate resistance $R_s$ equal to 37 kΩ, 82 kΩ and 166 kΩ have been respectively measured at MOSFET channel lengths $L = 5\mu$m, 3 $\mu$m and 1.4 $\mu$m. It was also shown that the resulting substrate back bias $\Delta V_b$ increased from 60 mV at $I_g = 10^{-7}$ A to 600 mV at $I_g = 10^{-5}$ A. The evolution $\Delta V_T$ of the threshold voltage caused by $I_g$ over this range has been shown to vary from 1 mV to 800 mV.

A new model for the hot-carrier substrate current and its effect on the device reliability and stability has been established. A study and investigation of the noise sources and origins in MOSFET were examined. This has led to the identification and formulation of a new type of noise that results from the channel length modulation (CLM noise).
The modification by accelerated stressing of the RG and TG MOSFET parameters (mobility $\mu$, conductivity $\sigma$, surface quality and recombination $S$, threshold voltage $V_T$, noise level $e_n$ etc.) have been reported. In order to obtain improved stressing times (shorter duration) X-ray radiation (20 KeV) was used. We observe that the mobility $\mu$ in both cases increases first with stressing time $t_s$ till a certain maximum where $\mu$ saturates and begins thereafter to decrease with $t_s$ toward a certain lower limit where it becomes constant and independent of $t_s$. This strange behaviour of mobility $\mu$ has been explained in terms of formation of fast and slow states. The behaviour of the device noise showed a good agreement with this assumption. A model has been presented to explain this observed behaviour of $\mu$. Another modelling is given for the device noise. We also noticed that, after a certain stressing time, although the mobility reaches an equilibrium position, $V_T$ continues to increase. This later behaviour has been explained in terms of slow state formation.

UV irradiation experiments (254 nm) showed that $V_T$ can be reduced and that the final level of $V_T$ depends on the irradiation power, which suggests that different trap levels contribute to the overall values of $V_T$. Experiments in which the two types of stressing, X-ray followed by UV, were carried out showed that the induced defects can be subsequently repaired by one method or the other. This behaviour has been qualitatively related to the physical and chemical structure and structural defects of the SiO$_2$ and the Si-SiO$_2$ interface. It was found that the induced radiation changes in the MOSFET devices were permanent (tested over a period of two years) but could subsequently be changed again by either UV or X-ray irradiation. This fact has led to the proposal that these two irradiation techniques can be used to tune the MOSFET for particular applications.

The effect of the magnetic field on MOSFETs was studied and analysed. The Hall voltage and magnetoresistance were adopted as a tool to study and investigate the magnetic properties. It has been shown that these latter effects are very sensitive to the sample parameters: mobility $\mu$, conductivity $\sigma$, doping level $n$. The structural quality which may be manifested in enlarged defect densities ($N_{as}$, $N_{ox}$) and carrier trapping and recombination are also sensitive to the operating conditions.

A Hall voltage of ~2mV was obtained with MOSFETs. However, appreciable transversal MOSFET currents caused due to the Lorentz force ($\Delta I_{RS}$ ~
7 μA) have been observed. It has also been revealed that both the magnetoresistance and the ohmic voltage introduced (due to the Hall contacts displacement) strongly influenced the behavior of the Hall voltage $V_H$.

It proved impossible to detect the effect of the Lorentz force and the Hall voltage in a clear way in a MOSFET because we can only observe $\Delta I_{DS}$. Therefore, a new design MOSFET with a split drain was used in combination with operational amplifiers. This device, (making use of the Lorentz force) can be used as a very high sensitive magnetosensor.

The theoretical and experimental work presented in this thesis has many potential industrial applications. The novelty of some aspects of this thesis are being used for a patent application via an industrial partner. In the near future, the noise reduction proposal will be realised in device form and tested. The realisation of such device will allow us to obtain chemically identical thin films resembling the active part of the MOSFET device. This will allow us to test and quantify the physical model for the irradiation processes using the appropriate spectroscopic techniques. The magnetosensor device will be tested in connection with reliability studies etc., and could have a huge industrial potential. This work is at present underway.
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