Energy-efficient SOC design technology and methodology

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FOR REFERENCE ONLY
Energy-efficient SOC design technology and methodology

by

David Walter Flynn

Doctoral Thesis

Submitted in partial fulfilment of the requirements for the award of

Doctor of Engineering of Loughborough University

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System-On-Chip Technology Demonstrators
Developed within the EngD Research Programme

SOC#1 TSMC 180nm G
Standard Low-Power

SOC#2 TSMC 130nm G
Dynamic Voltage Scaling

SOC#3 UMC 130nm SP/LL
Dynamic Voltage Scaling

SOC#4 TSMC 65nm LP
Dynamic Voltage Scaling & Leakage Management

SOC#5 TSMC 90nm G
Enhanced Leakage Management
Energy efficient SOC design technology and methodology

Abstract

This thesis covers the portfolio of research projects addressing dynamic and static power reduction applicable to mass-market designs. It covers work over the period 2001-2006 while employed in the Research and Development Group at ARM Ltd in Cambridge, UK, and seconded during 2005 to ARM Inc in Sunnyvale, California, USA.

The Research Programme has been focused on developing design styles and methodologies for synthesizable microprocessor and support Intellectual Property (IP) to address energy-efficient chip implementation using both dynamic and static power reduction while minimizing changes required to tools and library components. A canonical System-On-Chip (SOC) design, representative of portable battery powered low-power customer designs, was specified and developed in the first year of the research project and has been extended and developed over the five years. This has resulted in 5 technology demonstrator chips and evaluation platforms successfully being implemented and fabricated successfully. The author developed the evaluation platforms and demonstration software have been developed by the author to serve as technology demonstrators for the product groups in ARM to showcase new licensable control software and hardware IP as well as new power management standard library cells and multi-voltage components.

ARM Ltd has a number of advanced technology licensees and partners who have built tools, proprietary design flows and their own memory and library technology. Addressing the significant customer base of less expert licensees who do not have such in-house expertise has been the primary requirement for this research in order to equip them with EDA tools from partner companies and Physical IP building blocks from ARM that allow advanced dynamic and static power management techniques to be applied to synthesizable designs.

This EngD thesis covers the public material in relation to the technical innovation, the real-world engineering challenges, the subset of the Patents filed that have been granted or have received notice of acceptance, and the published results and conferences and publications. The “Intelligent Energy Manager” control software, the ARM1176-family DVFS-ready CPUs, the Intelligent Energy Controller, and the baseline specifications for the “Multi-Voltage Kits” and “Power Management Kits” are all ARM licensable products that have been developed from this research project.

Finally, the major achievement of the programme has been the invitation to contribute as a primary author to “The Low Power Methodology Manual”, published by Springer 2007, aimed at practical real-world engineering application of the methodology developed.
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  - Implementation lead on the DVS926 project and test-shuttle liaison

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  - 65nm silicon evaluation support and leakage modelling
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**Energy Efficiency Challenges**

Managing the power dissipation of complex System-On-Chip (SOC) designs has been a prime design consideration of ARM-based product designers for some years now. It is well understood that reducing both the peak and average power consumption will reduce the manufacturing and packaging costs as well as improve the reliability and battery life. However, the thriving market for ever more sophisticated mobile wireless devices such as cell phones, media players, Personal Digital Assistants and cameras is placing ever increasing demands on the battery. Consumers want more and more features in their mobile devices but still demand a convenient form factor and long battery life. Unfortunately battery technology is not developing fast enough to meet this demand and this short-fall is relentlessly driving the demand for cheap, low power, energy efficient SOCs with ever greater integration.

**CMOS Power Dissipation Fundamentals**

There are three major sources of power dissipation in digital CMOS circuits and they can be broken down in to:

- dynamic power dissipation from the switching activity to charge and discharge capacitive loads, the transitory short-circuit power caused when CMOS output drivers switch (*P*<sub>switching + Pshort-circuit</sub>)
- and leakage power dissipation (*P*<sub>leakage</sub>) due to the fact that the transistors are not perfect switches and do leak some current when logically “off”

\[
P_{\text{average}} = \alpha C_L \frac{V_{DD}^2 f_{\text{clk}}}{P_{\text{switching}}} + \frac{V_{DD} I_{\text{SC}}}{P_{\text{short-circuit}}} + \frac{V_{DD} I_{\text{leak}}}{P_{\text{leakage}}} \quad (1)
\]

**Addressing Dynamic Power**

In order to minimise the dynamic power dissipation term of equation (1) then not only should the clock frequency (*f*<sub>clk</sub>) be lowered but also the switching activity (*a*) and where possible ideally reducing the supply voltage (*V*<sub>DD</sub>). One of the simplest ways to reduce the switching activity is to inhibit registers from being clocked when it is known that their output will remain unchanged. In a typical SOC as much as 30% of the switching power is dissipated in the clock tree so this technique, known as Clock Gating (CG), can yield a significant saving in both power dissipation and energy consumption.

As power is the rate of doing work then the average power dissipation of a system can be reduced by slowing the rate at which work is done. In practice this means lowering the clock frequency (*f*<sub>clk</sub>) when the maximum system performance is not required. This technique, known as Dynamic Frequency Scaling (DFS), leads to a linear reduction in average power dissipation.
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Figure 0.1A– Leakage and Dynamic power trends from ITRS roadmap


![Graph showing gate length, normalized total chip power dissipation, and possible trajectory if high-k dielectrics reach mainstream production.]

Figure 0.1B– Leakage and Dynamic power trends from ITRS roadmap

![Diagram showing leakage components: $I_{LEAK} = I_{SUB} + I_{GATE} + I_{GIDL} + I_{REV}$.]
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However DFS does not reduce the energy consumption for a given task as the work done remains a constant. For some very "leaky" processes, the total energy consumption may in fact increase due to spending longer in active mode.

Real energy savings can however be achieved when at the same time as reducing the clock frequency, the voltage is also reduced to a level that is just high enough to support this lowered clock frequency. This results in less work to do in charging the internal capacitances to the supply voltage (VDD) and so less energy is consumed. This technique, known as Dynamic Voltage and Frequency Scaling (DVFS), leads to a quadratic reduction in energy consumption and a cubic reduction in average power dissipation. It should be noted that, as it is not possible to dynamically scale the voltage and frequency instantaneously, there is some energy overhead in moving between the various performance levels. And there is a technology dependent "floor" below which voltage scaling becomes unsafe and logic may behave unreliable or be subject to soft-errors.

Addressing Leakage Power

The other source of power dissipation is leakage power which is predominantly due to the fact that transistors are not perfect switches and so can never be completely turned off.

Although leakage power used to be considered insignificant when compared to dynamic power at 180 and 130nm technology, it has become significant at 90nm, and potentially dominant at 65nm and below, so can longer be ignored.

Figure 0.1A shows the trend projections for leakage power in relation to dynamic power for projected technology scaling from the International Technology Roadmap for Semiconductors (revised annually).

Leakage power is dissipated in both active mode and standby mode and the currents which go to make up the total leakage are increasing fast (Figure 0.1A). In some applications, it may be more energy efficient to run fast and stop rather than to lower the voltage and frequency due to the high active leakage currents.

There are four main sources of leakage currents in a CMOS transistor shown in Figure 0.1B

1. Sub-threshold Leakage (I_{SUB}) the current which flows from the drain to the source current of a transistor operating in the weak inversion region.
2. Gate Leakage (I_{GATE}) the current which flows directly from the gate through the oxide to the substrate due to gate oxide tunneling and hot carrier injection.
3. Gate Induce Drain Leakage (I_{GIDL}) the current which flows from the drain to the substrate induced by a high field effect in the MOSFET drain caused by a high VDG.
4. Reverse Bias Junction Leakage (I_{REV}) caused by minority carrier drift and generation of electron/hole pairs in the depletion regions.
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Of the various components which go to make up the total leakage current \( I_{EAK} \) it is currently the sub-threshold leakage \( I_{SUB} \) which is dominant. However, the gate leakage \( I_{GATE} \) is becoming significant but may yet be mitigated by high K dielectric materials in future (the lower dotted projection in Figure 0.1A).

The most effective techniques for mitigating sub-threshold leakage are Power Gating (often but confusing called Multi-Threshold CMOS, MTCMOS) and Back-bias (a form of what is often named Variable Threshold CMOS, VTCMOS) described below.

For the

Sub-threshold Current \( I_{SUB} \)

The MOSFET is said to be in the weak inversion region when the \( V_{GS} \) is below \( V_{th} \). In this region the \( V_{DS} \) drops across the reverse bias substrate drain junction. Hence the electric field along the channel is small. Since the electric field is small the drift component of the current in the channel is small and the current is dominated by diffusion. The carriers move by diffusion along the channel similar to charge transport across the base of bipolar transistors. Weak inversion dominates modern device off-state leakage due to the low \( V_{th} \). The sub-threshold current can be expressed as shown in the equations below.

Sub-threshold leakage occurs when a CMOS gate is not turned completely off. Its value is given by

\[
I_{SUB} = I_0 e^{(V_{GS} - V_T)/(\alpha V_{th})}
\]

where \( V_T \) is the device threshold voltage, \( V_{th} \) is the thermal voltage \( kT/q \) (25.9 mV at room temperature), \( V_{GS} \) is the gate source voltage, \( I_0 \) is the current when \( V_{GS} = V_T \). The parameter \( \alpha \) is a function of the device fabrication process and ranges from 1 to 2.5.

\[
I_{SUB} = \mu C_{ox} V_{th}^2 W \frac{V_{GS} - V_T + \eta V_{DS}}{2nV_{th}} \cdot \left( 1 - e^{\frac{-V_{DS}}{nV_{th}}} \right)
\]

(2)

- Where \( V_T \) is the threshold voltage
- \( \eta = kT/q \) is the thermal voltage
- \( C_{ox} \) is the gate oxide capacitance
- \( \mu \) is the zero bias mobility
- \( m \) is the sub-threshold swing coefficient (also called the body effect coefficient)

And \( W \) and \( L \) are the Width and Length parameters for the transistor. The \( V_{DS} \) dependence is prominent in short channel devices. In long channel devices the sub-threshold current is independent of the drain voltage for \( V_{DS} \) larger than a few \( V_T \).
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Dynamic and Leakage Power Mitigation Approaches

ARM licenses and delivers both Synthesizable components (CPUs and System level components and Interconnect) and Physical "Standard Cell" and Memory library components. The research programme in this Thesis has been driven by the requirements to allow the benefits and dynamic and leakage power management to be applied with as few requirements to change the Electronic Design Automation (EDA) tools and flows that customers acquire or internally develop.

Dynamic Voltage and Frequency Scaling (DVFS)

Dynamic power management has been addressed by developing cell-level hardware components, design and implementation methodologies to address the voltage-scaled timing relationships, and all built within a licensable Operating System software component. The voltage-scaled power and energy savings are only realized by a high-level set of performance monitoring and predicting policies that determine the real-time processing workload and build the knowledge to set the operating performance levels just high enough to allow task deadlines to be met and the frequency and voltage to be scaled effectively. (Described in detail in Appendix B papers, pages B3-B93)

DVFS is a system level design challenge, and a Performance setting and monitoring control approach has been taken to abstract the ARM control functions as licensable Intellectual Property hardware and software components, abstracting away the customer-specific voltage scaling and power supply management details.

Leakage mitigation using State-Retention Power-Gating (SRPG)

Although analogue techniques such as Dynamic Threshold Scaling or adaptive well bias schemes appear attractive, the requirement to provide reliable portable Physical IP components that are free from production complexities (to avoid device latch-up for example) provided a focus for the research work to focus on extensions to standard logic cell libraries to support effective leakage mitigation.

Building on a foundation of power gating switch cells, isolation cells and retention registers the challenge was to build a standard-cell abstraction extension to standard synthesis and place-and-route implementation flows to allow design and verification without having to dive down to transistor level views and analysis (something that is possible for expert companies with their own transistor level design expertise, but not appropriate for licensable Physical IP to less expert design teams and customers).

A State-Retention paradigm that allows seamless state saving and restoring before and after power gating respectively has been chosen and developed that can be applied transparently to RTL design and support very energy efficient state retention and restoration appropriate for fast real-time responsive systems.
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**Industrial State-of-the-Art at the start of the EngD Research Programme**

A clear distinction has to be drawn at the outset of this thesis between cutting-edge academic research and the realities of commercially viable and re-usable solutions that can be widely licensed and deployed

- **Academic research – university (including some industrial collaboration)** research that has driven forward the techniques and theoretical benefits of a variety of low power and high performance techniques applicable to micro-processors, multi-media systems or cell library designs. The primary references for the power management techniques adopted for this research are introduced and discussed in this section

- **‘Expert’ Industrial Usage** – where Integrated Device Manufacturers (IDMs) apply some of the academic research work to key market/application areas using their detailed knowledge and access to in-house wafer fabrication data, internal and pre-production external design automation tools, and source-level IP, libraries, memories etc to support transistor level analysis and sign-off of complete solutions. ARM has the privilege of delivering synthesizable processor and system IP to such customers and gains visibility of the techniques and challenges presented and the bespoke solutions often adopted for in-house design flows. Understanding approaches but steering clear of proprietary or potentially patented techniques is important, the references are typically to publicly announced products and lag behind the early confidential material. The leading-edge industrial references that were public at the time are introduced below. Interaction with such advanced designed groups also has the benefit that early visibility of the EDA tools enhancements influenced by such cutting-edge groups

- **Mainstream deployment** – requiring widely-available synthesizable and physical IP together with mainstream EDA tools and methodology. This is ARM’s primary business and is the focus of the “applied research” covered in this thesis. The process technology often lags behind that of the leading-edge IDMs and relies on design tools that help abstract the detailed transistor problems away from designer/implementer such that the methodology and tools are as close as possible to the synthesis/place-and-route/timing analysis flows they are familiar with. The abstraction away from transistors and the commercially sensitive/valuable design data then supports licensing to end designers through Foundry models where the implementation flows rely solely on “front-end” views and abstracted models, and the transistor-level back-end internals are merged in the licensed Foundry

One key reference used to plan the technology demonstrators was the International Technology Roadmap for Semiconductors. The ITRS2001 roadmap [1] was the starting reference for this thesis focussing on the 90nm and 65nm technology schedules. This full roadmap is updated every two years (2003, 2005) with an intermediate update published in the even years

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**Academic Prior Art for Dynamic Voltage Scaling**

A comprehensive survey of low power design techniques was published in IEEE transactions VLSI Systems by Benni, Bogliolo and DeMicheli [2]. This usefully applied voltage scaling to Intel ARM StrongARM SA1100 processor as one of the primary low power design examples.

The author’s research builds largely on work that ARM initiated and supported at Berkeley Wireless Research Center, University of Berkeley, California [3], [4]. An ARM810 cached microprocessor design was made available to Thomas Burd and team and used as the reference design for dynamic voltage and frequency scaling. The hardware control techniques focused on a ring-oscillator approach, the frequency of operation varying with the voltage[5]. The research for the DVFS work covered in this thesis has focused on the alternative approach of setting a target frequency (better understood by conventional static timing analysis tools) and then supporting table look-up or adaptive dynamic voltage control schemes.

In order to offer a licensable system level solution a major component is the algorithms to set and monitor deadlines in order to exploit the potential for reduced frequency and hence reduced headroom power rail control. The research behind the software control techniques has been built on the work at the University of Michigan, under Prof Trevor Mudge’s research group [6], notably by Krisztian Flautner’s PhD research [7], [8] (Dr Flautner was recruited to ARM in 2000 and ARM licensed the technology to use in hardware and software products subsequently).

**Commercial Prior Art for Dynamic Voltage Scaling**

A number of companies had worked on chip level voltage scaling where the entire design inside the pad-ring could be voltage scaled, and the level shifters in the input/output pads provide the analogue voltage interfacing from the core chip voltage to the IO pad voltages.

For example Intel had published the design challenges from their perspective in 1999[9] and announced a 1GHz Mobile Pentium III processor with SpeedStep proprietary frequency/voltage scaling technology in 2001[10]. Transmeta had announced their low-power Crusoe processor with “LongRun” dynamic voltage and frequency scaling technology [11], [12].

The primary ARM licensee working on delivering products with DVFS was Texas Instruments, the OMAP1510 application processor plus DSP for wireless applications was unveiled in 2001 [13] and DVS control support was unveiled in 2002 [14]. The ARM925 CPU used in this product was a derivative of the ARM926EJ-S CPU that has been used for all but the first of the research projects undertaken by the author in this research programme.

As the projects developed the adaptive voltage scaling work grew out of work at University of Boulder, Colorado [15] which were subsequently exploited jointly with National Semiconductor Inc.
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Academic Prior Art for Power Gating and State Retention

Power-gating is the preferred name used in this thesis for the less descriptive Multiple Threshold CMOS, “MTCMOS” used in academic research. The original technique was proposed as early as 1993 by Mutoh et al applied to 0.5 micron technology [16]. Subsequently techniques for preserving the state of registers while logic was power gated was described by the same team at NTT Labs as applied to DSP subsystems [17].

Kao and Chandrakasan at MIT published a paper at the Design Automation Conference in 1997 dealing with the issue of designing and sizing MTCMOS switch transistors [18]. A follow-on paper that described the system issues to be addressed to make MTCMOS work practically without sneak leakage paths was presented at the European Solid-State Circuits Conference, ESSCIRC 2001[19]. This paper outlines the practical application of Hi-Vt switches to both combinational logic and sequential circuits.

Stan at University of Virginia described the concept of “Multi-Voltage” CMOS, MVCMOS, as an enhancement over logic-level MTCMOS, where gate control voltages above and below the standard supply rails, in a paper published at ISLPED in 1998[20].

Run-time power gating is a technique to dynamically switch off functional sub-systems to cut leakage power while some of the design remains active, described at MICRO-35 conference in 2002 by a group from University of Rochester [21][21].

Commercial Prior Art for Power Gating and State Retention

Research work published by NTT from 1996 at ISSCC is definitive starting point for the power gating work [17] and introduces the concept of “balloon latches” to preserve state and the application of high-Vt MTCMOS (header) switches to isolate leak logic on a virtual power rail.

In 2002 Zyuban from IBM published a study of retention register designs [22] and although this is largely focussed on a preference for level-sensitive scan latch design, it provided a thorough review of the area cost impact of different retention latch designs and control alternatives. Zyuban was one of the group who also contributed to an ISLPED paper in 2004 that described run-time power gating applied to the Power-4 CPU architecture [23].

From a generic cell library perspective Virtual Silicon Inc announced libraries with internal power gating and support for gate negative-bias [24] under the “Mobilize™” brand (Virtual Silicon was subsequently acquired by MOSAID Inc in 2005). The approach of delivering a “fine-grain” leakage controlled library was commercially interesting as it sought to re-use standard EDA synthesis flows as near as possible, but at the expense of larger cell area and reduced performance. The ability to characterize the switch I Ron-drop effects entirely within the cell were highly attractive compared to the complexities of requiring instance-based library cells with shared power gating.

Sequence Design was the first of the EDA companies to announce tools to support designing with shared power switch component “cells” in 2004 [25].

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RTL Design for Low Power Prior Art

Many of the preceding techniques focus on the low-level technology components and circuits, or higher-level system design approaches and methods. But for the purposes of this thesis the Register-Transfer Level, RTL, of coding is that of most relevance as this applies to both the synthesizable IP that ARM licenses and must be cleanly and efficiently supported by EDA tools and “standard cell” library components and abstractions.

Because a lot of the dynamic power is dissipated in the clock tree in high-speed designs, designers often code in a level of Architectural Clock Gating where clocks to subsystems are gated explicitly. By carefully ensuring that synthesizable RTL coding of clock enable functions is carefully constrained the clock gating can be automated the principles were outlined back in 1994 by Benini et al. [26] Such techniques are now supported widely by EDA synthesis and optimization tools.

RTL coding is fundamentally built on the concepts of “global” power that is implicitly always on, and “ideal” clocks that have zero latency. Multi-voltage approaches, whether they are based on dynamic voltage scaling or power-rail gating for reducing leakage power however require careful management of explicit power rails and clock tree latencies that vary with voltage.

Power Formats that can annotate the multi-voltage intent on to standard synthesizable RTL design are finally starting to become industry-standardized in early 2007 [27], [28].
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[10] "Intel unveils 1GHz Mobile Pentium III", http://www.findarticles.com/p/articles/mi_m0EKF/is_12_47/ai_72068750


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1. Eng-D Context

Introduction
The focus of this research and development program is to understand and improve what is required for effective and successful IP deployment and re-use in system level design. This requires identifying, documenting, and where possible, solving problems with the IP or working with Electronic Design Automation, EDA, companies to improve their tools and data representations. A primary output is that of defining and documenting best practices.

Background
ARM primarily designs and licences processors for embedding in chip designs supported with development tools and bus technology and peripheral IP. Key attributes to the commercial success involve not only the obvious hardware characteristics such as performance, power and area but also less tangible criteria such as clean product integration, systems level software modelling and design partitioning (aspects that all lead to better time-to-royalty).

Commercial Environment
ARM has grown considerably as an organization, survived a major industry down-turn in 2002 and diversified into new product areas largely due to a number of acquisitions. The author's role has changed a number of times in particular leading technical due diligence on potential acquisitions, only some of which have been successful.

Despite this the author has been able to maintain a role within the Research and Development group although with a focus often on shorter-term advanced product development rather than actual research.

The ARM business model is built on partnership with leading technology companies and, with a significant portion of licensing business based on synthesizable IP, the need to work closely with EDA companies has required ARM to build collaborative projects with EDA partners. Synopsys Inc was chosen as the collaborative partner in the work described in this portfolio report as the majority of ARM's customers use front-end synthesis tools from this company.

Project Team and Management Responsibilities
As an "ARM Fellow" in the R&D group the author's responsibilities essentially have been technical but include line management responsibility for a small group and a mentoring role for a series of engineers seconded to the research group for periods of 6 months to 2 years. In order to take on the chip developments that have run over the duration of the Eng-D projects the author has also had the responsibility to negotiate with EDA and Foundry partners to build collaborative virtual teams to see through both the implementation and the successful evaluation of the technology demonstrators that have been demonstrated to customers.
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Figure 1.1A – Technology Demonstrator Research Vehicles

sARS2 180nm (2001-2)

DVSS926 130nm (2002-3)

ULTRA926 130nm (2003-4)

ATLAS926 65nm (2005-6)

Figure 1.1B – IP Creation/Implementation/Integration model

Core-based design: Integration focus

HDL

LOGICAL

PHYSICAL

Creation (IP Provider)

Implementation (IP Licensee)

Integration (IP End User)

Requirements

GDSII

DF EngD ARR01

Figure: 1

1-2
Low power, battery-power end market focus research collaborations

The most important market for ARM is in licensing microprocessors and support fabric and peripherals into the very cost sensitive battery power product area. Energy efficiency is in fact the primary metric for this market area rather low power consumption per-se so the application of techniques to minimize dynamic energy consumption and standby or leakage power consumption have remained the primary R&D goals and context for the work over the last 5 years. As the technology has advanced the R&D focus has moved to real-world deployment of voltage scaling for the 0.18μ and 0.13μ technology nodes, and then leakage management techniques for 90nm and 65nm.

The basic canonical design taken as the starting point for the Eng-D in 2001 has proved a valuable starting point. Every year a low-power technology demonstrator chip has been designed, developed and manufactured that has been used to build credibility with end customers.

Representative low-power silicon developed and evaluated (Fig 1.1A):

- 2001-2: TSMC 180nm 1.8V ARS2 (ARM946) embedded SOC design
- 2002-3: TSMC 130nm-G 1.2V DVS926 Dynamic Voltage Scaling
- 2003-4: UMC 130nm-HS/LL 1.2V ULTRA926 optimized Dynamic Voltage Scaling
- 2005-6: TSMC 65nm-LP 1.2V Fine-Grain Leakage + Dynamic Voltage Scaling
- 2005-6: TSMC 90nm-G 1.0V Coarse-Grain Power Gating Leakage Control

Widely (re) licensable IP and partnership model

There are a number of licensing models that are supported on different commercial terms and conditions that affect visibility of certain design data when it comes to integrating a core in a system. In simple terms the key license agreements are:

- Architectural License – rights to design and implement new micro-architectures subject to compliance with Architectural Validation Suites provided by ARM.
- Technology License – the rights to design and manufacture a specified micro-architectural implementation typically of a synthesizable core (or a hard macro).
- Single-Use/Multi-Use Design License (SUDL/MUDL) – the rights to design with a pre-qualified core with a licensed semiconductor Foundry partner using only abstracted model views, where the physical layout of the core is merged before fabrication.

Design for re-use techniques and the low-power methodologies developed as part of the Eng-D portfolio have had to address the diversity of partners and design flows in order to ensure that customers both of synthesizable and pre-hardened (and pre-verified) IP components have all the design views required to integrate in a timely and risk-managed way.

One of the technology demonstrators used a foundry core (UMC 130nm ARM926EJ) while the rest have all focussed on synthesizable RTL IP (again ARM926EJ). Synthesizable processor development is now the primary focus for ARM and the deployment of soft cores is illustrated in Fig 1.1B
Fig 1.2A – 2002Q3 Announcement

02 October 2002

ARM Holdings plc Q3 Trading Update


In our Quarter 4 2001 earnings announcement in January 2002, we indicated that if the downturn in the semiconductor industry persisted our visibility could be affected. In our second quarter earnings announcement in July, we referred to continued challenging market conditions in the industry. These conditions have deteriorated further in the third quarter, resulting in the deferment of investment decisions by our partners and therefore a slowdown in licensing activity. At the same time, the weakening US dollar is also impacting our reported results.

As a consequence, revenues for the three months to 30 September 2002 are expected to be approximately £33 million. The foreign exchange impact on reported revenues is expected to amount to £2 million. Pre-tax profit for the period is expected to be approximately £8 million.

The company continues to generate cash with cash balances likely to increase to approximately £121.7 million at the period end, compared with £115.4 million at 30 June 2002. We continue to manage our working capital rigorously and accounts receivable is projected to fall to approximately £28.1 million at 30 September 2002 from £40.2 million at 30 June 2002.

The slowdown in licensing activity in the third quarter has given rise to a reduction in the backlog at the end of September. Deferred revenue, being that portion of the backlog that has been invoiced to partners but not yet recognised in the profit and loss account, is projected to decrease, as expected, from £17.4 million at 30 June 2002 to approximately £13.8 million at the end of September.

Whilst our sales pipeline and backlog of signed contracts give us reasonable visibility in our business, the persistent difficult market conditions mean that the timing of the closure of licensing deals is unpredictable. Although the fourth quarter is usually stronger than the third quarter, we do not anticipate any significant upturn in business activity before next year.

Key long-term growth indicators for the company remain healthy, supported by our partners’ commitment to ARM’s product roadmap and extensive third party network which supports ARM technology. New and existing partners continue to choose the ARM architecture for increasing numbers of projects. In addition some partners who are taking action to reduce their R&D costs have taken decisions to support only one architecture, being ARM. OEMs adopting the ARM architecture as their platform of choice are also driving ARM’s position, which is expected to increase significantly in the fourth quarter.

Fig 1.2B – 2002Q3 Announcement and Share-price impact
Satisfying design integration views for the single-/multi-use design environment is the most challenging and is of immediate use to technology licensees. In figure 1.1B the implementation flow for ARM (or architectural licensees) is shown in the left column, that of the semiconductor licensee in the middle and the system integrator on the right. ‘Brick walls’ are effectively enforced at the boundaries to ensure that only pre-verified IP views are provided to the next column together with sufficient support to allow the next stage implementation to be verified successfully.

**IP security requirements and the need for abstract models**

The ARM business model as depicted in Fig 1.1B requires customers who are only licensed to integrate ARM CPU cores to work with abstracted model views in order to prevent the synthesizable technology-independent CPU designs from being inadvertently or maliciously copied or distributed. Implementation licensees take on the legal responsibility for protecting synthesizable deliverables under the terms of their license; integrators are often much smaller companies or sub-contractors who do not necessarily have the financial resources or established relationship to take on the “crown-jewels” RTL and validation suites. Therefore the need to ensure that abstract models hide the detailed IP design and implementation is a requirement of the methodologies and best-practice developed under this research programme. In particular the models need to include:

- **Functional model(s)** – for simulation. These range from high-level behavioural models that simply generate realistic bus traffic through to implementation-specific models that are cycle accurate and contain both functional and, for example, scan-test accurate models to allow detailed macro-cell integration in a larger SOC device.

- **Timing models** – for synthesis constraints, static timing analysis (STA) and timing accurate simulation. Abstracted models need to hide the internal paths but provide accurate context-dependent timing such that input ramp times and load-dependent output transitions are handled accurately.

**Commercial and business cycles (2002 downturn, subsequent growth)**

When embarking on the Eng-D programme in 2001 the basic research and development direction had been agreed and established between ARM and Loughborough. Commercial realities have meant that the author has been called upon to help support other parts of the organisation and work flexibly with both the product and business development teams. The research agenda has in fact remained largely unchanged from the company perspective and the research projects have moved into mainstream engineering and products over the last three years.

The industry downturn – ARM 2002Q3 (see Fig 1.2A, 1.2B) resulted in some lay-offs and serious cost-cutting and re-focussing on core business strengths. From a research programme perspective this drove me deeper into collaborations with EDA and foundry licensees and partners to maximise the benefits for ARM while minimizing the financial burden. As mask and fabrication costs rise relentlessly it has proved invaluable to have forged relationships with other companies to share the costs and derive mutual value.
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Fig1.3A – 2004 Announcement to acquire Artisan Components from 2005

ARM And Artisan Combine To Deliver System-On-Chip IP Solutions
CAMBRIDGE, UK and SUNNYVALE, CALIF. - Aug. 23, 2004 - ARM Holdings plc (LSE: ARM; (Nasdaq: ARMK)) and Artisan Components, Inc. (Nasdaq: ARTS) today announced that they have entered into a definitive agreement under which ARM will acquire Artisan.

Highlights
- Under the terms of the agreement, Artisan stockholders will receive $8.60 in cash and ARM stock equivalent to 0.41 ARM ADSs for each outstanding Artisan share. Based on closing prices for ARM ADSs as of August 20, 2004, the implied value is $33.89 per Artisan share, representing an aggregate consideration of approximately $913 million.

This transaction represents an excellent strategic combination:
- Enables the combined company to deliver one of the industry's broadest portfolios of system-on-chip (SOC) intellectual property (IP) to their extensive, combined customer base.
- Better positions the combined company to take advantage of growth opportunities across multiple industries as system design complexity increases in the sub-micron age.
- Highly complementary sales channels combining ARM’s channel to more than 130 silicon manufacturers, with Artisan’s channel to more than 2,000 companies.
- Strengthens the links between key aspects of SoC development, enabling the combined company to deliver solutions that are further optimized for power and performance.

Warren East, Chief Executive Officer of ARM will continue as Chief Executive Officer of the combined companies, with Lucio L. Lanza, Chairman of Artisan, and Mark R. Templeton, President and Chief Executive Officer of Artisan, joining the Board of Directors of ARM as a non-executive director and an executive director, respectively, on completion of the transaction.

Directors and executive officers of ARM and Artisan have agreed to vote in favor of the acquisition in respect of shareholdings amounting to an aggregate of approximately 2.7 percent of ARM’s outstanding shares and 4.6 percent of Artisan’s outstanding shares.

The completion of the transaction is expected to occur in the fourth quarter of 2004 and is subject to ARM and Artisan stockholder and regulatory approvals and other customary closing conditions.

Artisan is a leading provider of physical IP components for the design and manufacture of complex SOC integrated circuits (ICs). The company’s comprehensive product portfolio includes standard cell libraries, embedded memories, input/output cells, analog functions and high-speed interface IP. Artisan’s products are optimized for performance, density, power and yield and are available in support of process technologies at many of the world’s leading semiconductor manufacturers. Artisan has licensed its IP components to thousands of IC design teams at more than 2,000 companies worldwide.

Fig1.3B – 2003 PowerWise DVS collaboration with National Semiconductor Inc

National Semiconductor and ARM Release PowerWise Interface Open-Standard Specification

SANTA CLARA, CALIF. AND CAMBRIDGE, UK - October 6, 2003 - National Semiconductor Corporation (NYSE:NSM) and ARM (LSE: ARM; (Nasdaq: ARMK)) today released PowerWise™ Interface (PWI) technology, jointly promoted as an open standard interface for system power management. PWI technology enables rapid deployment of advanced power management solutions in handheld electronic devices by providing an open, industry-wide standard for the interconnect between digital processors and power management integrated circuits.

Today’s portable electronic devices such as mobile phones, hand-held gaming consoles and portable media players offer a host of new benefits for consumers. However, these benefits place a significant strain on the power budget. Designers now face the dilemma of having to reduce the power consumption of digital processors while simultaneously maximizing battery life. This dilemma has led to the development of more advanced power management solutions that dynamically reduce power consumption based on the application software workload and environmental conditions. PWI technology provides the hardware interconnect standard for universal deployment of such solutions.
EngD Context

The author has been asked to take on extra responsibilities of the last five years which have certainly broadened commercial and technical experience

- technical due diligence for several potential acquisitions in the USA that ARM considered but chose not to acquire (in the case of a DSP company) or was out-bid by a competitor (in the case of the configurable logic company, Triscend\(^1\), where a number of months were spent working in California in late 2003 before the company was acquired by Xilinx in March 2004\(^2\))
- integration and building communication channels in subsequent acquisition (see next sub-section) where the author was seconded to California for 6 months and now continues to support remotely from Cambridge.

These have all had a significant effect on the timescales to complete the work toward the Eng-D portfolio, but thankfully these have all been technically well aligned to the underlying low power and IP deployment brief for my research.

2005 acquisition of Artisan Components and new Physical IP business

The decision to acquire Artisan Components Inc\(^3\), (see Fig 1.3A) headquartered in Sunnyvale, California was a major one and the author became involved in helping understand the technology and low power specific product portfolio. The scrutiny of investors and analysts was intense and resulted in a six month secondment to the “ARM Physical IP Division” as Artisan had become from July 2005.

This was an intense learning experience but being located in the midst of a number of major ARM customers and close to the headquarters for both Synopsys Inc and Cadence Inc, the major EDA partners used by the majority of ARM customers did have significant benefits.

The opportunity to live in a different country has been an enriching experience but not an easy one from the point of view of personal commitments. Although this delayed the Eng-D completion further it provided a whole new layer of data and resources once the Standard Cell and Memory Physical IP was all part of the broader ARM portfolio – and now are a part of ARM’s problems that could not be blamed on a third party!

Collaborative Partnership relationships built up

ARM has given the author the freedom and responsibility to build up the external relationships to support the multi-way R&D projects. The key people and organizations worked with include:

Synopsys Inc – Michael Keating, VP Engineering and now Synopsys Fellow in Advanced Technology Group, Rich Goldman VP Strategic Alliances, Alan Gibbons Principal Engineer. The partnership has helped sponsor design tools and the Synopsys-hosted secure “DesignSphere Access” web-based design cluster that has been used to great benefit for the Synopsys projects that underpin this research.

\(^1\) http://www.arm.com/news/4741.html
\(^2\) http://www.xilinx.com/prs_rips/xil_corp/0435_triscend_acquisition.htm
\(^3\) http://www.arm.com/news/6015.html
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Fig1.4A – 2006 Collaboration success announcement with TSMC

**ARM in the News**

18 July 2006

**TSMC & ARM Team On 65nm Low Power Test Chip**

Taiwan Semiconductor Manufacturing Company (TSMC) and ARM have confirmed that collaboration on a 65-nanometer (nm) low-power test chip has resulted in dramatic reductions in both dynamic and leakage power.

The year-long collaboration resulted in a 65nm test chip based on the ARM926EJ-S processor demonstrating advanced power management technologies. By applying dynamic voltage and frequency scaling techniques, the test chip provides the ability to operate at the lowest possible power level for each mode of operation. In this case, the ARM test chip achieved a dynamic power reduction of over 60 percent. Significantly, even on this TSMC 65LP low leakage process, advanced power-gating technology further reduced standby leakage by a factor of 6 times, the companies said.

"Power efficiency is the most important challenge facing the semiconductor industry as mobile devices exploit advanced processes to deliver greater functionality and performance," said David Finn, ARM Fellow. "ARM and TSMC are partnering on 65nm and 40nm technology development, and this project demonstrates the significant leakage and dynamic power reductions that we can achieve through close technical collaboration and implementation of fully functional silicon."

"One of TSMC's key differentiators is our insistence on proving our services and those of our partners in silicon, before bringing them to the design community," said Ed Wan, senior director of Design Services Product Marketing, TSMC. "Our collaboration with ARM demonstrates beyond doubt that advanced process technologies, combined with innovative design techniques, and process-targeted libraries, can achieve distinct and significant power savings, which is absolutely vital to companies on the technological leading edge."

The test chip incorporates low-power memory macros, level shifters, retention flip-flops, and isolation cells in the library, which is characterised for multiple voltages.

**Fig1.4B – 2006 Collaboration announcement with ArchPro Design Automation**

**ARM AND ARCHPRO VERIFY 65-NANOMETER MULTI-VOLTAGE SOC BEFORE SILICON**

Joint project results in verification solution for multi-voltage power management

SAN JOSE, CA AND CAMBRIDGE, UK – July 24, 2006 – ARM ([LSE:ARM]; Nasdaq: ARMHY] and ArchPro, today announced success in a joint R&D project to validate advanced multi-voltage power management design techniques. Employing ARM® Intelligent Energy Manager (IEM™) technology and validated with ArchPro’s Multi-Voltage Simulator Tool (MVSIM) resulted in an EDA tool for pre-tapeout verification of power-managed designs. The project produced working 65-nanometer (nm) silicon for a complex reference system-on-chip (SoC) design jointly verified by the two companies. The SoC used an ARM processor with IEM technology demonstrating a number of active and sleep modes, to vary power and performance.

"MVSIM has proven its ability to verify sophisticated voltage schemes prior to tapeout and is verification solution applicable to a wide range of multi-voltage designs including power-managed systems," said Steve Smith, Director of Business Development, ArchPro.
National Semiconductors Inc – PowerWise\textsuperscript{4} DVFS announced October 2003 (see Fig 1.3B) as part of the consortium required to build credibility to the ARM Intelligent Energy Manager IEM\textsuperscript{5,6}, hardware and software products that grew out of the R&D group work from 2001. Gordon Mortensen, the Engineering Manager, and Ravi Ambatipudi, the Product Manager have been the primary points of contact.

United Microelectronics Corp, Taiwan – collaboration relationship built with Dr Patrick Lin, Chief SOC Architect\textsuperscript{7} and his team at UMC resulting in the ULTRA926\textsuperscript{8} silicon announced in November 2004. (Dr Dar-Sun Tsien, Ming Hsu in particular)

Taiwan Semiconductor Manufacturing Corporation – collaboration relationship built with Dr Cliff Hou\textsuperscript{9} and the Design Services team at TSMC on the ATLAS\textsuperscript{10} project announced in June 2006 (see Fig 1.4A) (Dr LC Lou, Ken Wang and Helen Chang in particular)

ArchPro Design Automation\textsuperscript{11}, an EDA start-up based in California and India and which resulted in collaborative work on the 65nm Multi-voltage (ATLAS) project verification\textsuperscript{12} announced in July 2006 (see Fig 1.4B). The author was invited to join the Technical Advisory Board at ArchPro in August 2004, with permission granted by ARM. The primary relationship has been built up the founder and CTO, Srikanth Jadcherla from the inception of the company.

\textsuperscript{4} http://www.arm.com/news/3800.html
\textsuperscript{5} http://www.arm.com/products/esd/iem_home.html
\textsuperscript{6} http://www.ieee-socc.org/SOC2003/Program/Saturday/saturday.html
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Energy efficient SOC design technology and methodology
2. Canonical SOC Design – 5 generations

As part of the R&D work on advanced core deployment flows an initial test chip has been developed as a baseline 'canonical' design. This test-case integrates a hardened CPU and Tightly-Coupled Memories, TCMs, (with associated high-speed CPU clock domain) with representative system blocks (system bus clock domain) and basic peripherals

Requirements

ARM has traditionally built test chips in order to verify IP in silicon. The focus is on a vehicle to run validation suites for a specific core processor and implements test co-processors and 'trick-boxes' in hardware together with minimal memory controller interface for code and data.

The requirements specification drawn up for the first SOC, “Reference System Design #1”, RSD1, are driven by methodology and best practice system reuse criteria rather than by an actual product design, but the underlying design has been chosen to be representative of real-world problems and complexities:

- Real-time system design requiring careful hardware and software partitioning. The project is primarily hardware focussed to start with but with the ability to run audio synthesis or decompression algorithms.
- Multiple clock domains, including semi-synchronous CPU and bus clocks, and asynchronous subsystems. Typically ARM processor test chips have focussed on the CPU clock domain but the design challenges for system integrators are those of integrating, verifying and testing designs on a derived system bus clock.
- Hardened IP deployment – ensure integration at 'black-box' level only, not using internal views. This “core-based” design approach matches well that of licensees that work with Foundry pre-qualified IP, and many partner companies that license RTL but have specific internal groups that harden particular cache configuration cores for wider deployment by product groups.
- Rapid-prototyping environment supporting early functional testing and software development in FPGA. The aim here is to ensure that the design practices target both FPGA and SOC tools.
- Design taken to layout and extracting timing – with a potential for test shuttle fabrication run where sponsored, or “virtual tape-out” to ensure the back-end flow and parasitic extraction are fully understood – rather than optimistic layout estimates.
- Derive best-practice guidelines for test integration for the hardened IP within the system.
- Sufficiently small die-area and pad-count to target single “shuttle” die size and low-cost plastic BGA packaging. (408-pin BGA developed for this program used for initial four technology demonstrators, a pre-existing 388-pin BGA for the fifth in the series.)
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Figure 2.1A – 180nm sARS2 ARM946 Reference Design

Figure 2.1B – 180nm sARS2 ARM946 Reference Design

Memory Map

Simple efficient decode

ROM

0x00000000

IO space

[AHB and APB]

Privileged access

Expansion space

ABORT if unused

RAM

Off-chip SRAM

On-chip TCRAM

0x00000000

2-2


The first project was a single-voltage "standard" low power design. To minimize board-level hardware complexity, a software-controlled audio playback system was chosen as a reasonably demanding real-time application target (Fig 2.1A)

- ARM946 CPU with dual 8Kbyte Instruction and Data caches
  - 200MHz CPU clock target
- AMBA AHB on-chip interconnect clocked at 100MHz
  - 32-bit SDRAM interface off chip for 32Mbyte+ bulk memory
  - 16-bit Flash EPROM interface for external ROM boot
  - 32-bit Synchronous SRAM fast memory interface
  - "Software-DMA" interface to audio subsystem
- AMBA APB on-chip peripheral bus clocked at 50MHz
  - Interrupt controller and System counter timers
  - Programmable UART for terminal interfacing
  - GPIO to support LEDs/Switches and other interfaces
- Dual PLL design
  - Dual crystal clock provision
  - 400MHz System PLL for CPU and bus IP with external divider control to control CPU in 12MHz steps from 84MHz to 264Mhz
  - 384MHz fixed rate PLL for reference clock dividers to Audio (48MHz) Timers (1MHz) UART (3 84MHz)
- JTAG serial debug agent connection
  - Support external debugger connection and memory-mapped diagnostics
  - Support on-board flash programming
- Audio subsystem
  - Stereo subsystem to merge up to 8 sound streams in hardware with hardware stereo image positioning
  - Support for 16-bit PCM or 8-bit log format audio data
  - Over-sampling digital anti-alias filtering
  - Digital pulse-density modulation drive of standard output pads
  - 2-pads per channel support for simple R-C off-chip filtering

The design was kept small enough to target onto single Xilinx XCV2000E device to support functional verification, albeit at 1/10th of the target CPU performance but enough to write basic waveform generation algorithms in C, using the SSRAM interface rather than the full SDRAM/Flash memory controllers

A simple memory map was used as the starting point (Fig 2.1B)

The project was used to develop best practice Test/Reset/Clock domain controllers, investigate multiple domain clock gating in the EDA implementation flows and to get the basic FPGA and SOC design flow and verification infrastructure in place
Energy efficient SOC design technology and methodology

Figure 2.2A - 130nm DVS926 Reference Design

Figure 2.2B - 130nm DVS926 Reference Design
Canonical SOC Design – 5 generations

**SOC#2 – the DVS926 Dynamic Voltage Scaling Demonstrator**

The research group had completed a software-based dynamic voltage-and-frequency control demonstration system and the canonical design was enhanced to become a vehicle for evaluating both the design and technology implications for dynamic energy management using DVFS. The target technology for the project was TSMC 130nm "G" process (1.2V nominal). The "Intelligent Energy Manager (IEM)" platform needed a Linux operating system environment for real-world benchmarking so the CPU was upgraded to one with MMU and caches large enough to run operating systems such as Linux efficiently:

- ARM926EJ CPU with dual 16Kbyte Instruction and Data caches
  - 240MHz CPU clock target
- AMBA AHB on-chip interconnect clocked at 120 (and 60) MHz
  - 32-bit SDRAM interface off chip for 32Mbyte+ bulk memory
  - 16-bit Flash EPROM interface + expansion banks
  - Audio subsystem reused but with hardware DMA
- AMBA APB on-chip peripheral bus clocked at 60MHz
  - Interrupt controller extended to match Linux environment
  - 1MHz System counter timers and 1KHz Real-Time-Clock
  - Dual UARTs to support both console and diagnostic channel
  - 48 GPIO to support wide expansion interfacing
- Dual PLL design (Re-using the Reference Clock generator from sARS2):
  - 480MHz System PLL for CPU and bus IP with external divider control to control CPU in 12MHz steps from 160 to 300Mhz
- JTAG serial debug agent connection (with rigorous validation)
- Dynamic Voltage Scaling CPU support
  - Analogue level shifters on system bus interface
  - Digital clock generation scheme to dynamically modulate CPU clock and manage DVFS phase alignment
  - Four performance levels: 240/180/120/60MHz (worst case)
  - Transparent latch based retiming to guarantee bus hold times
- Hardware API support for abstracting system-specific interfaces:
  - Fractional dynamic performance setting interface
  - Fractional accumulator dynamic performance counters
- Prototype National Semiconductors "Adaptive Voltage Scaling" control

The memory map was enhanced to be closely compatible with Intel StrongARM-1100 ASIC in order to simplify the Linux operating system porting to this platform. The project was used to specify EDA tools for "standard-cell" dynamic voltage scaling implementation and static timing analysis and verification requirements, to understand clock latency variation with DVS, and to prototype the basis of the ARM "Intelligent Energy Controller (IEC)" product development.
Energy efficient SOC design technology and methodology

Figure 2.3A - 130nm ULTRA926 Reference Design

Figure 2.3B - 130nm ULTRA926 SOC Design
SOC#3 – the ULTRA926 DVFS reference system design

UMC offered silicon to ARM based on their 130nm “Fusion” process that supports mixing of dual threshold “Low Leakage (LL)” and “High Speed(HS)” transistors. ARM had already qualified a “Foundry” ARM926EJ core with dual 16K caches on the HS process (pre-hardened and optimized for 288MHz worst case).

The opportunity was taken to approach this as a true reference design with considerable work going into transistor level simulation to understand the limits of voltage scaling, the predicted clock and I/O latency across the voltage boundaries.

The author was responsible for assembling a five-way consortium to implement the design:

- UMC financed the project and fabricated/packaged the ULTRA926 silicon
- ARM enhanced the reference canonical design, the CPU characterized for voltage scaling, and optimized clock generators to provide finer performance control, and had a production-quality IEC controller design ready to integrate
- Artisan Components provided the low power libraries and TCM memories, and designed the level shifters and isolation cells to ARM’s requirements, plus new low-power PLLs and standard 3.3V IO cells.
- National Semiconductors contributed production quality “PowerWise” Adaptive Voltage Scaling IP and serial power control interface.
- Synopsys Professional Services took on the SOC implementation, timing sign-off and chip finishing (with ARM support)

The design was kept software-compatible with the DVS926 design, apart from enhancements to the IEC API and the dynamic voltage scaling. The only noteworthy differences in the hardware design were:

- ARM926EJ CPU optimized to 288MHz worst case (1.08V)
- More optimal dynamic CPU performance scaling frequencies:
  - 100% (288MHz worst case)
  - 83% (240MHz)
  - 67% (192MHz)
  - 50% (144MHz)
- Dual PLL system clock generator (576MHz + 480MHz)
  - Configurable PLL dividers support up to 360MHz on the CPU
- Register-based retiming interface (latches removed)
  - Dynamically advances reduced speed CPU clock wrt AHB
  - Improved timing analysis and sign-off
  - New level shifters with integrated isolation clamp functionality

The project was used to improve both the voltage scaling control and the design methodology considerably compared to the original DVS926 development which required many iterations of layout to close timing. The project also helped finalize the specification of the first DVS-enabled ARM CPU product – the ARM1176EJ-S with IEM support.
Energy efficient SOC design technology and methodology

Figure 2.4A – 65nm ATLAS926 Reference Design

Figure 2.4B – 65nm ATLAS926 SOC Design
SOC#4 – the ATLAS926-65LP Leakage & DVFS demonstrator

TSMC offered ARM R&D early technology access to their 65nm “LP(Low Power)” process. This is in fact a process that has greatly reduced leakage compared to the 65nm Generic technology but the different gate-oxide material used requires a 1.2V nominal power supply. The low leakage characteristics are great for standby battery life but the dynamic power is higher due to the 1.2V supply rail compared to 1.0V “G” process (nominally 1.44 x the dynamic power), and the transistors are inherently slower so cannot hit the same peak performance of 65G. Although 65LP is a low leakage process to start with the project was approached as a test case for comparing leakage management techniques, but the DVFS architecture from the ULTRA926 design was extended to support voltage scaling of the CPU standard cell logic with level-shifted interface to all the cache RAMs; the High-Vt RAM cells were predicted to have no safe voltage scaling headroom below the 10% tolerance on the 1.2V supply. The chip was designed to allow limited experimental voltage scaling of the RAM supply to confirm this in silicon.

The leakage techniques evaluated in the project included:

- Multiple Vt cell library implementation
- On-chip power gating (MTCMOS switched cells)
- On-chip state retention registers (with automatic save and restore)
- Off-chip power gating (with scan-based IP state save and restore to memory)

The "Intelligent Energy Controller" hardware API was enhanced to provide four levels of leakage management to support transparent operation through the software Wait-For-Interrupt mechanism.

The author was responsible for RTL design and verification of the design and hand-off with synthesis constraints to an implementation team in Taiwan that also provided an early “Fine-Grain” MT-CMOS power-gated library for the joint project.

The design was kept software-compatible with the ULTRA926 design, apart from further enhancements to the IEC API and re-designing the dynamic voltage scaling frequency syntheses around a new PLL.

- ARM926EJ CPU with voltage scaled standard-cell region
  - A complex task handling level shifters on time critical cache RAM interfaces
- More optimal dynamic CPU performance scaling frequencies:
  - 100% (240MHz worst case)
  - 80% (192MHz), 60% (144MHz), 40% (96MHz), 20% (48MHz) steps
- Single high-speed PLL system clock generator (1GHz)
  - 20-slot shift register architecture to allow 65LP implementation
  - Synchronous pre-compensated CPU-to_AHB re-timing

The project proved an excellent opportunity to understand 65LP technology and to understand and compare the relative real-time and leakage power cost functions for the basic approaches to leakage mitigation. Subsequently this chip became an important technology demonstrator for The Design Automation Conference in 2006.
Energy efficient SOC design technology and methodology

Figure 2.5A – 90nm SALT926 Reference Design

Figure 2.5B – 90nm SALT926 Reference Design
**Canonical SOC Design – 5 generations**

**SOC#5 – the SALT926-09G Leakage and physical IP demonstrator**

Many customers require "G(Generic)" technology rather than the "LL/LP" variants in order to achieve sufficient CPU performance for high-end products. Addressing the significant leakage power on 90nm and below is of significant interest in order to weigh up the relative merits of active versus standby power for G versus LP.

ARM had acquired Artisan Components at the end of 2004 and needed to showcase new low-power cell libraries and leakage management components that were in development for what has become the “PMK (Power Management Kit)” product add-on to standard cell libraries.

TSMC 90G is an industry standard technology reference point so was chosen for the project. As a 1.0V nominal voltage process and with power-gating responsible for reducing headroom by an appreciable degree at the Standard Cell devices, all Dynamic Voltage Scaling was removed from the design and attention focussed on aggressive leakage management to showcase the relative merits of various leakage mitigation techniques:

- Clock-Gating (restart within clock cycles)
- State-Retention Power-Gating (restart within a microsecond)
  - Keep register state powered in high-Vt “balloon”, power gate logic
- Scan-based state save to on-chip or external memory (10's microseconds)
  - Some energy save/restore cost, VDDCPU leakage cut to zero
- Software-activated cache clean (millisecond restart)
  - Power down cache and logic, energy cost to reload cache

A number of Physical IP customers have requested worked examples of back-bias and dynamic threshold scaling, the academic analysis\(^1\) and modelling have always looked attractive but typically only IC companies that own wafer fabrication facilities are able to reach production with threshold scaling. Support was added to the system architecture to support implementation on Triple-Well technology to support:

- Reverse bias – for leakage characterisation
  - plus experimental reduced performance operating mode named “Long-Life”
- Experimental forward bias operating mode named “Turbo”

Because currently no timing models support both power rail and threshold voltage scaling concurrently the CPU is stopped whenever changing threshold voltages.

This project again reused the canonical design and extended the ATLAS design where possible to maintain software compatibility. Synopsys also wanted to understand and evaluate power gating of peripheral IP and contributed a USB OTG MAC and PHY to the project, so the Sound/DMA system was stripped out and replaced in the address map by the USB block. The base-line Linux OS port should be unaffected, ready to allow for new USB device drivers to be developed and added.

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Energy efficient SOC design technology and methodology

Figure 2.6 Summary by SOC Design Generation

<table>
<thead>
<tr>
<th>SOC</th>
<th>Name</th>
<th>CPU</th>
<th>Target MHz</th>
<th>Technology</th>
<th>Low Power Management</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>sARS2</td>
<td>ARM946</td>
<td>200</td>
<td>180nm</td>
<td>Clock Gating</td>
</tr>
<tr>
<td>#2</td>
<td>DVS926</td>
<td>ARM926</td>
<td>240</td>
<td>130nm</td>
<td>DVFS+CG</td>
</tr>
<tr>
<td>#3</td>
<td>ULTRA926</td>
<td>ARM926</td>
<td>288</td>
<td>130nm</td>
<td>DVFS+CG</td>
</tr>
<tr>
<td>#4</td>
<td>ATLAS926</td>
<td>ARM926</td>
<td>250</td>
<td>65nm(LP)</td>
<td>DVFS+Fine-Grain Leakage</td>
</tr>
<tr>
<td>#5</td>
<td>SALT926</td>
<td>ARM926</td>
<td>300</td>
<td>90nm</td>
<td>VTCMOS + Coarse-Grain Leakage</td>
</tr>
</tbody>
</table>
This turned out to be a highly complex project to complete and tape out

- Experimental power gating and retention standard cell library
  - Derived from exiting library plus extended characterization work
- CPU performance tuned around special 1.2GHz PLL clock synthesis
  - 133% (400MHz) "Turbo" forward bias VTCMOS experimental mode
  - 100% (300MHz) worst case standard sign-off
  - 66% (200MHz) "Long-Life" back-bias VTCMOS experimental mode
  - 33% (100MHz) Bus-speed operating mode (suits scan save/restore)
- SOC integration with power-gated USB controller and OTG PHY macro
- Switch to a 388-pin BGA package
  - In order to re-use a tester and load board in ARM Austin design centre

Summary

Figure 2.6 summarizes in tabular form the five generations of reference system-on-chip design developed over the research programme lifetime. Although the 90nm design appearing after the 65nm project may appear out-of-order from a process technology road-map perspective the SALT926 chip is the most advanced from an aggressive leakage power management perspective. The techniques and design methodologies are the primary driver for the order in which the projects were developed.
Energy efficient SOC design technology and methodology
3. Low Dynamic Power Design - DVFS

Technology Dependent Design Constraints

The available voltage scaling range and associated safe operating frequencies are highly technology dependent and to support AVS need to understand the typical process characteristics as well as worst case conditions.

All the EDA tools and models expect to calculate delay (and hence operating frequency) by being given an appropriate set of Process/Voltage/Temperature conditions. For a dynamic performance scaling system design the requirements start from establishing a range of useful operating frequencies and then determining how low the voltage can be reduced at these operating points in order to calculate the predicted power and energy savings.

Frequency is linearly proportional to dynamic power at a given voltage, reducing frequency results in timing slack that can be made use of by voltage scaling - which reduces dynamic power by a square-law function. However supply voltage cannot be reduced safely below a certain point where RAMs and registers start to become unreliable.

This chapter documents the extended range characterization and analysis for the ULTRA926 DVFS project using the "LF027" UMC L130E HS FSG ARM926EJ foundry core with dual 16Kbyte caches implemented by ARM Ltd and supplied as a pre-verified hard-macro CPU core.

Standard Operating Conditions

Two port-level extracted timing models are provided with the standard Foundry design kit for the LF027 core.

'Worst case' – for static timing analysis of input setup times and output settling times (design critical paths)

- 1.2V - 10% = 1.08V
- 125 degrees C (commercial grade hot)
- slow-slow process corner

'Best case' – for static timing analysis of input and output hold times (to fix any race conditions)

- 1.2V + 10% = 1.32V
- -40 degrees C (commercial grade cold)
- fast-fast process corner

Due to the wide spread in both timing characteristics and buffer tree latencies the "typical" process, room temperature and nominal 1.2V operating voltage are useful to understand for voltage scaling.
Energy efficient SOC design technology and methodology

Figure 3.1A – Standard Voltage Characterization for clock period and latency

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Latency-max (ns)</th>
<th>Latency-min (ns)</th>
<th>Latency spread (ns)</th>
<th>Fmax (MHz)</th>
<th>Latency/Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.080</td>
<td>slow/slow</td>
<td>3.472</td>
<td>1.741</td>
<td>1.531</td>
<td>0.210</td>
<td>288.0</td>
<td>0.501</td>
</tr>
<tr>
<td>1.200</td>
<td>typ/typ</td>
<td>2.075</td>
<td>1.064</td>
<td>0.939</td>
<td>0.125</td>
<td>481.9</td>
<td>0.513</td>
</tr>
<tr>
<td>1.320</td>
<td>fast/fast</td>
<td>1.468</td>
<td>0.733</td>
<td>0.649</td>
<td>0.084</td>
<td>681.2</td>
<td>0.499</td>
</tr>
</tbody>
</table>

Figure 3.1B – Extended Voltage Characterization for clock period and latency

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Latency-max (ns)</th>
<th>Latency-min (ns)</th>
<th>Latency spread (ns)</th>
<th>Fmax (MHz)</th>
<th>Latency/Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.660</td>
<td>typ/typ</td>
<td>6.172</td>
<td>2.973</td>
<td>2.654</td>
<td>0.319</td>
<td>162.0</td>
<td>0.482</td>
</tr>
<tr>
<td>0.730</td>
<td>typ/typ</td>
<td>4.803</td>
<td>2.360</td>
<td>2.100</td>
<td>0.260</td>
<td>208.2</td>
<td>0.491</td>
</tr>
<tr>
<td>0.800</td>
<td>typ/typ</td>
<td>3.920</td>
<td>1.962</td>
<td>1.748</td>
<td>0.214</td>
<td>255.1</td>
<td>0.501</td>
</tr>
<tr>
<td>0.940</td>
<td>typ/typ</td>
<td>2.896</td>
<td>1.483</td>
<td>1.316</td>
<td>0.167</td>
<td>345.3</td>
<td>0.512</td>
</tr>
<tr>
<td>1.200</td>
<td>typ/typ</td>
<td>2.075</td>
<td>1.064</td>
<td>0.939</td>
<td>0.125</td>
<td>481.9</td>
<td>0.513</td>
</tr>
<tr>
<td>1.320</td>
<td>typ/typ</td>
<td>1.882</td>
<td>0.960</td>
<td>0.844</td>
<td>0.116</td>
<td>531.3</td>
<td>0.510</td>
</tr>
</tbody>
</table>

Figure 3.1C – Extended Voltage Delay behaviour for typical silicon

![Voltage Delay Graph](image)

The graph shows the Relationship between Voltage (V) and Delay (ns) using the equation:

\[ y = -24.193x^3 + 84.707x^2 - 100.41x + 42.447 \]

y = Delay (ns)

Voltage (V)
Fig 3.1A tabulates the results of full transistor-level characterization for the standard library operating conditions (±10% voltage tolerance).

Clock tree latency is combinational delay of the clock tree from input port to the best/worst of the final register cell clocks in the layout. The period measurement is determined from the worst case register-to-register paths in the design.

For voltage scaling systems design the clock tree latency scaling with voltage is a key concern as this affects the macro-cell interface timing for SOC integration. The spread in clock buffer tree latency was extracted (determining the earliest and latest flip-flop in the entire core to be clocked) and the "spread" expressed as a proportion of the minimum clock period in the right-most column.

In terms of analysis the typical silicon at room temperature and nominal voltage is predicted to run at about 1.7 times as fast as the worst case corner where the SOC design must be signed-off to guarantee to meet timing.

Extended Range Operating Conditions – typical silicon

A series of extended characterization points were generated below 1.08V. Two linear steps of 0.94 and 0.80V were used as the starting point and then half steps at 0.73V (predictably a limit for the technology) and 0.66V (where RAM model reliability is potentially extrapolated beyond operational limit).

All the extended range analysis was performed with Synopsys NanoSim\(^1\) fast HSPICE simulator on a transistor level model of the cached processor core with extracted parasitic load extraction.

The clock tree latencies appear to scale linearly with voltage (close to the 50%). See Fig 3.1B.

Graphical Analysis of typical-corner process

The first stage of analysis focuses on typical silicon for the initial analysis at this reflects behaviour of the majority of the production manufactured silicon. Fig 3.1C illustrates graphically the timing characteristic for both the worst case register-to-register path time and the underlying clock buffer tree latency. Both are monotonically and show unexpectedly good tracking (latency consistently of the order of 48% to 51% of the cycle time).

Extended Range Operating Conditions – slow silicon

For design sign-off with reduced voltage rail the worst case timing analysis also needs to be performed with a timing model that accurately reflects the delays and latency for slow corner silicon worst case conditions.

A series of extended characterization points were generated below 1.08V. Two linear steps of 0.94 and 0.80V were used as the starting point and a further half step at 0.73V were used: See Fig 3.2A.

Energy efficient SOC design technology and methodology

Figure 3.2A – Extended Slow-corner Voltage PFC for clock period and latency

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Latency(max) (ns)</th>
<th>Latency(min) (ns)</th>
<th>Latency(spread)</th>
<th>Fmax (MHz)</th>
<th>Latency/Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.730</td>
<td>slow/slow</td>
<td>7.721</td>
<td>3.626</td>
<td>3.237</td>
<td>0.389</td>
<td>304.2</td>
<td>0.505</td>
</tr>
<tr>
<td>0.800</td>
<td>slow/slow</td>
<td>6.198</td>
<td>2.963</td>
<td>2.636</td>
<td>0.327</td>
<td>288.0</td>
<td>0.501</td>
</tr>
<tr>
<td>0.940</td>
<td>slow/slow</td>
<td>4.442</td>
<td>2.187</td>
<td>1.931</td>
<td>0.256</td>
<td>225.1</td>
<td>0.492</td>
</tr>
<tr>
<td>1.080</td>
<td>slow/slow</td>
<td>3.472</td>
<td>1.741</td>
<td>1.531</td>
<td>0.210</td>
<td>191.8</td>
<td>0.480</td>
</tr>
<tr>
<td>1.320</td>
<td>slow/slow</td>
<td>2.645</td>
<td>1.333</td>
<td>1.162</td>
<td>0.171</td>
<td>161.3</td>
<td>0.478</td>
</tr>
</tbody>
</table>

Figure 3.2B – Extended Fast-corner Voltage PFC for clock period and latency

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Latency(max) (ns)</th>
<th>Latency(min) (ns)</th>
<th>Latency(spread)</th>
<th>Fmax (MHz)</th>
<th>Latency/Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.730</td>
<td>fast/fast</td>
<td>3.287</td>
<td>1.660</td>
<td>1.485</td>
<td>0.175</td>
<td>304.2</td>
<td>0.505</td>
</tr>
<tr>
<td>0.940</td>
<td>fast/fast</td>
<td>2.100</td>
<td>1.079</td>
<td>0.960</td>
<td>0.119</td>
<td>476.2</td>
<td>0.514</td>
</tr>
<tr>
<td>1.320</td>
<td>fast/fast</td>
<td>1.468</td>
<td>0.733</td>
<td>0.649</td>
<td>0.084</td>
<td>681.2</td>
<td>0.499</td>
</tr>
</tbody>
</table>
Extended Range Operating Conditions – checking fast corner linearity

The only sign-off library required is the standard 1.32V/fast-fast/-40C model provided in the standard design kit but for completeness a couple of low voltage characterizations were performed to check the behaviour was still monotonic and followed the same basic curve as the slow and typical analysis. See Fig 3.2B.

Caveats

The low voltage figures will need to be de-rated further to cope with the effects of degraded transition times across the buffer tree boundary between the 1.2V SOC domain and the scaled voltage CPU domain.

All the analysis of the core is performed on the macro-cell in isolation. With careful power ring design and attention to package and PCB design outside the SOC the effects of voltage drop due to IR must again be factored into appropriate de-rating of the ‘ideal’ PFC modelling.

In both cases the careful choice of master clock frequency may be used to set the maximum operating frequency level safely for the less than ideal voltage delivered to the DVS subsystem on-chip.

Performance Scaling Design Requirements

The data from the technology-specific voltage and frequency range analysis described in the previous section are used to drive the decisions over which performance points are energy efficient. The final frequencies selected need to be carefully chosen for a CPU such as the ARM926EJ where the bus interface must be synchronous to the core clock. The bus is typically clocked using a divided-down version of the CPU clock but all transfers between the bus and core domain occur on the CPU clock edge when a clock qualifier (HCLKEN) is asserted to indicate that this CPU clock edge captures input signals and updates output signals.

NOTE: future IEM-enabled CPU cores will manage asynchronous bus interfaces and allow arbitrary CPU and interface clock relationships. However a synchronous relationship between bus and CPU at maximum clock rate is still highly desirable to ensure the maximum communication bandwidth without the overheads of synchronization protocols that are required for the generic case of asynchronous clocking.

Frequency Range and ‘Granularity’

The technology demonstrator is required to allow evaluation of both the worst case guaranteed frequency (288MHz CPU) but also typical silicon which will operate up to 480+ MHz.

The IEM technology treats the CPU maximum frequency as 100% performance and under software control may reduce and adjust the required performance level dynamically. Although simple clock division by 2 and 4 is easy, more complex clock frequency generation is required to exploit energy efficient performance points over the voltage scaling range; for this specific technology operation below 144MHz looks to be at the edge of safe operating margins.
Energy efficient SOC design technology and methodology

Figure 3.3A – Synchronous performance ratios for a 12X PLL Clock

<table>
<thead>
<tr>
<th>Bus = 66MHz</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/Bus ratio</td>
<td>Perf</td>
<td>MHz</td>
</tr>
<tr>
<td>6</td>
<td>100.0%</td>
<td>400.00</td>
</tr>
<tr>
<td>4</td>
<td>66.7%</td>
<td>266.67</td>
</tr>
<tr>
<td>3</td>
<td>50.0%</td>
<td>200.00</td>
</tr>
<tr>
<td>2</td>
<td>33.3%</td>
<td>133.33</td>
</tr>
</tbody>
</table>

Figure 3.3B – Synchronous performance ratios for a 12X and 10X PLL Clock

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/Bus ratio</td>
<td>Perf</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>100.0%</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>83.3%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>66.7%</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>50.0%</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>33.3%</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.3C – Voltage Scaling Range – slow silicon

<table>
<thead>
<tr>
<th>Interpolated [SS] latencies</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Period (ns)</td>
<td>Voltage (V)</td>
<td>Latency (ns)</td>
<td>Bus Ratio</td>
</tr>
<tr>
<td>3.571</td>
<td>1.050</td>
<td>1.786</td>
<td>6</td>
</tr>
<tr>
<td>4.286</td>
<td>0.950</td>
<td>2.143</td>
<td>5</td>
</tr>
<tr>
<td>5.357</td>
<td>0.850</td>
<td>2.679</td>
<td>4</td>
</tr>
<tr>
<td>7.143</td>
<td>0.750</td>
<td>3.571</td>
<td>3</td>
</tr>
<tr>
<td>10.714</td>
<td>(unsafe?)</td>
<td>(unsafe?)</td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 3.3D – Energy saving estimates from slow-corner analysis

<table>
<thead>
<tr>
<th>Estimated [SS] energy calculations</th>
<th>Energy Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq(MHz)</td>
<td>Voltage</td>
</tr>
<tr>
<td>280.00</td>
<td>1.05</td>
</tr>
<tr>
<td>233.33</td>
<td>0.95</td>
</tr>
<tr>
<td>186.67</td>
<td>0.85</td>
</tr>
<tr>
<td>140.00</td>
<td>0.75</td>
</tr>
</tbody>
</table>

Figure 3.3E – Energy calculations for standard voltage operation

<table>
<thead>
<tr>
<th>Estimated [SS] energy calculations</th>
<th>Energy Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq(MHz)</td>
<td>Voltage</td>
</tr>
<tr>
<td>288.000</td>
<td>1.080</td>
</tr>
<tr>
<td>288.000</td>
<td>1.200</td>
</tr>
<tr>
<td>288.000</td>
<td>1.320</td>
</tr>
</tbody>
</table>
In an IEM system the decision to run the processor at a lower frequency (say 66%) results in efficient operation so long as the power consumed by the task running for (1.5x) longer (100%/66%) is reduced.\(^2\) Given a working voltage range in the order of 0.75 to 1.32 volts there is no advantage in supporting frequencies below those which can operate in this range. The Granularity definition refers to the number of performance steps available. From evaluation work this matters especially within the range 50-100% of max performance.

The approach adopted in the case of a synchronous interface to the CPU is to treat the operating performance levels as multiples of the bus and memory controllers in the system. In order to ensure that the wide frequency range does not exceed the memory controller interface this is limited to a maximum bus frequency of 75MHz.

To address fine granularity of control, a master clock division ratio of 12 is adopted which gives easy derivation of half/third/quarter/sixth/twelfth divider ratios. The worst case CPU performance target is 288MHz but to evaluate silicon that is likely to be typical process rather than worst case the design frequencies should be configurable faster on the bench. For 400MHz operation the clock frequency sub-multiples that can be directly synthesized are shown in Fig 3.3A.

**Improving performance control granularity**

All the above frequency ratios can be produced from a master clock in the range 550-800 MHz. Because voltage scaling is most efficient close the 100% level the introduction of second clock source phase-locked to 10x the bus frequency facilitates the provision of a performance point at 5x the bus frequency. The additional complexity in clock generation is deemed worth the design effort to produce the extra precision in clock generation – see Fig 3.3B.

**Voltage/Frequency scaling range**

By interpolating from the maximum-frequency period graphical analysis of the slow process corner (and in this case simply multiplying by 50% for the estimate of clock tree latency) the following range of voltage/frequency operating points are estimated – see Fig 3.3C.

Below the 50% performance scaling point there is no more voltage scaling headroom left for safe extrapolation.

**Energy saving estimates from slow-corner analysis**

By factoring into account the square of the voltage, the relative frequency and extended durations at the proposed operating frequencies the relative energy savings with frequency and voltage scaling are tabulated in Fig 3.3D.

For normal usage a nominal power supply of 1.2V would be specified so the basic reference point is calculated – in this case for the characterized PVT for 288MHz (not 280MHz) by scaling the duration to complete the work is shown in Fig 3.3E.

\(^2\) For dynamic power consumption this is proportional to the CV\(^2\)f term. As long as voltage can be lowered such that V\(^2\) reduction outweighs the 1/f factor in extended duration of the workload. In summary there is no energy efficiency to be won when the voltage can no longer be reduced proportionally.
Figure 3.4A – Voltage Scaling Range – slow silicon

<table>
<thead>
<tr>
<th>Interpolated [Typ] latencies</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Period (ns)</td>
<td>Voltage</td>
</tr>
<tr>
<td>2.500</td>
<td>1.050</td>
</tr>
<tr>
<td>3.000</td>
<td>0.920</td>
</tr>
<tr>
<td>3.750</td>
<td>0.830</td>
</tr>
<tr>
<td>5.000</td>
<td>0.770</td>
</tr>
<tr>
<td>7.500</td>
<td>(unsafe)</td>
</tr>
</tbody>
</table>

Figure 3.4B – Energy saving estimates from typical-corner analysis

<table>
<thead>
<tr>
<th>Estimated [Typ] energy calculations</th>
<th>Energy Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq (MHz)</td>
<td>Voltage</td>
</tr>
<tr>
<td>400.00</td>
<td>1.05</td>
</tr>
<tr>
<td>333.33</td>
<td>0.92</td>
</tr>
<tr>
<td>266.67</td>
<td>0.83</td>
</tr>
<tr>
<td>200.00</td>
<td>0.77</td>
</tr>
</tbody>
</table>

Figure 3.4C – Energy saving estimates for standard voltage conditions

<table>
<thead>
<tr>
<th>Estimated [Typ] energy calculations</th>
<th>Energy Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq (MHz)</td>
<td>Voltage</td>
</tr>
<tr>
<td>420.000</td>
<td>1.080</td>
</tr>
<tr>
<td>420.000</td>
<td>1.200</td>
</tr>
<tr>
<td>420.000</td>
<td>1.320</td>
</tr>
</tbody>
</table>
Design for Low Dynamic Power- DVFS

These must be treated as rough work estimates but there is certainly the potential for halving the energy when not running in peak conditions for the CPU portion of the CPU design.

Energy saving estimates from typical process analysis

Typical silicon is estimated to run at about 420MHz at a voltage of 1.08V. Taking a 400MHz master clock to exercise typical silicon to the same analysis is performed to confirm estimates – see Fig 3.4A, Fig 3.4B, Fig 3.4C.

The theoretical energy savings are slightly lower between nominal and 50% (8.23:3.55 compared to 8.40:3.38) but again confirm the performance levels are a useful working set.

Variable Clock latency management

The CPU presents a wide (Harvard) bus interface which presents a design challenge with both the frequency (and SOC control) and the inherent clock buffer tree delays vary with voltage.

Synchronous approach

Only (pseudo-) synchronous multiples of the bus clock are used in this design:

- In DVS-emulation mode, 6 x AHB clock rate (and stopped).
- In DPS, DVS and AVS mode, 6 x, 5x, 4x and 3x AHB clock rate (and stopped).

Pre-compensation of the CPU clock in relation to the system bus clock is used such that the processor is run at "early" with respect to the system interface timing reference (AMBA HCLK rising edge) in preparation for reduced voltage operating points. The cost is a slightly tighter input setup constraint on all inputs sampled from the system bus but because the system bus is run at one sixth of the processor clock frequency the constraint is of the order of 4 CPU cycles compared with 6 in the non pre-compensated case.

To indicate the active processor clock edge in which transfers between the HCLK and CPUCLK domains are initiated the HCLKEN qualifier must be asserted on the processor preceding the active clock edge when HCLK rises.\(^3\)

Hold-time management at the AHB interfaces

The SOC interface to the AHB interface on the CPU is entirely referenced to the rising-edge of HCLK.

In this design the CPU is clocked sufficiently early with respect to HCLK to guarantee that input hold times to the CPU are never violated at the lowest voltage operating point.

In order to make sure the interface timing to the SOC is never violated a set of registers is added to the interface outputs from the voltage scaling domain: Outputs from the CPU domain have a rising-HCLK register added such that output transitions are only enabled when HCLK is high. This guarantees that "early" clocking of the CPU domain can never cause early output changes that could violate the AHB timing relationship to HCLK for the SOC voltage domain.

\(^3\) And this HCLKEN qualifier must be pre-compensated earlier for reduced performance points, as must nRESET.
### Figure 3.5A – Latency Pre-compensation for reduced voltage/frequency operation

<table>
<thead>
<tr>
<th></th>
<th>Freq (MHz)</th>
<th>Ratio</th>
<th>Period (ns)</th>
<th>Precomp (ns)</th>
<th>Latency (ns)</th>
<th>AHB target (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 100%</td>
<td>288.00</td>
<td>6</td>
<td>3.47</td>
<td>5.21</td>
<td>1.79</td>
<td></td>
</tr>
<tr>
<td>CPU 83%</td>
<td>240.00</td>
<td>5</td>
<td>4.17</td>
<td>5.21</td>
<td>2.14</td>
<td></td>
</tr>
<tr>
<td>CPU 66%</td>
<td>192.00</td>
<td>4</td>
<td>5.21</td>
<td>5.21</td>
<td>2.68</td>
<td></td>
</tr>
<tr>
<td>CPU 50%</td>
<td>144.00</td>
<td>3</td>
<td>6.94</td>
<td>5.21</td>
<td>3.57</td>
<td></td>
</tr>
<tr>
<td>PLL:</td>
<td>576.00</td>
<td>12</td>
<td>1.74</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus:</td>
<td>48.00</td>
<td>1</td>
<td>20.83</td>
<td></td>
<td>15.63</td>
<td>64.00</td>
</tr>
</tbody>
</table>
Latency pre-compensation specification

Analysing the worst case latency at reduced voltage provides the basic pre-compensation timing by which the CPU clock domain must be advanced. At higher voltages the latencies all decrease so there is no danger of invalidating interface timing.

The requirement to run the x10 PLL as well as the x12 PLL complicates the design. Although on the same process voltage and temperature (on the fixed power 1 2V SOC domain) the outputs relationships are such that even locked to the same bus clock the handover between PLL sources must be handled by synchronization handshake. As such there will be an uncertainty of one clock period at the 83% (240MHz) in the CPU waveform so a conservative pre-compensation by 3 cycles of the x12 PLL clock is chosen.

The AHB timing constraints must therefore be set to 9/12 of the clock period (i.e. the AHB target frequency must be constrained to meet 12/9 of the actual frequency i.e. 64 MHz for the 48MHz worst case design target. See Fig 3.5A.

The highlighted latency figure for the 83% performance point is in fact a minimum figure with up to one clock cycle of "uncertainty" due to the requirement to synchronize the secondary PLL clock divider to the HCLK waveform produced by the of the primary PLL clock. This is still guaranteed to be less than the 5.21ns pre-compensation specified.

Debug clock domain synchronization with variable latency

Debug signals are synchronized to HCLK (not CPUCLOCK) and then qualified with HCLKEN at the core to ensure valid state advance clocking. Limiting the debug synchronization frequency to AHB HCLK rate causes minimal synchronization timing penalty (HCLK >> TCK frequency for the debug agent) and avoid the expensive requirement for clock-tree balancing of the debug clock synchronizer to the variable voltage VDD_CPU domain.4

4 The Debug domain TCK must be synchronized using HCLK and generates RTCK, the return TCK handshake to support DPS or DVS/AVS, especially when PLL clock resynchronization delays may be introduced.
Energy efficient SOC design technology and methodology

Figure 3.6A – Power-Test-Reset-Clock control structuring
Design for Low Dynamic Power- DVFS

Power/Test/Reset/Control Requirements in detail – see Fig 3.6A

- Top-level module of the SOC design
- Contains the high-frequency state machine used to derive the reference clocks to the system
- Designed to be synthesized and placed as a 'pseudo-hardened' block to constrain the timing of the clock generation and ensure low-skew and cleanly defined clock and reset sources – to ensure clock tree buffering and balancing start from known relationship.
- Subsequently this can be black-boxed as a LIB component for chip-level STA if required – but the netlist is usable by the STA and ATPG tools
- Instantiate independently for each power domain and control the clocks and associated resets to this domain as well as controlling test configuration
- Support development of each sub-system with independent power domain in isolation – providing resets and clocks to each domain suitable for standard RTL development and verification. The expertise necessary to balance clocks, and manage buffer tree latencies on clocks and resets of hardened subsystems, is encapsulated in the PTRC design and implementation
- Assumed to be powered at all times that the SOC but support handling of switching voltage rail(s) to subsidiary voltage domains
- When domains are to be powered off active low resets shall be asserted and clocks then clamped to zero
- When domains are to be powered up, once the voltage rail is stable and safe then the clock shall be started and the (active-low) resets de-asserted
- All clocks identified with "clk_" prefix
- Resets to be asynchronously asserted and synchronously de-asserted from the domain clock for the appropriate domain
- All resets identified with "rst_" prefix and where all resets are conventionally active-low assertion ("_n" postfix)
- All clocks and resets fully controllable from SOC pins to ensure clean test and timing analysis flows
- Testability control – support fully controllable clocks and resets
  - testmode forces all clocks to be multiplexed to externally controllable (crystal) clock input
  - testmode forces all resets to multiplexed to externally controllable active-low reset input
  - pll_bypass forces internal clock to be multiplexed to externally controllable (crystal) clock input not the PLL synthesized clock
  - pll_bypass forces 'PLL locked' signal to be overridden (as PLL switched out)
Energy efficient SOC design technology and methodology

Figure 3.7A – PLL configuration for 12X PLL

<table>
<thead>
<tr>
<th>Xtal (MHz)</th>
<th>12</th>
<th>13.33333</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ratio = x36</td>
<td>480.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x42</td>
<td>504.00 560.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x48</td>
<td>576.00 640.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x54</td>
<td>648.00 720.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x60</td>
<td>720.00 800.00</td>
<td></td>
</tr>
</tbody>
</table>

CPU 100% performance (MHz)

<table>
<thead>
<tr>
<th>Xtal (MHz)</th>
<th>12</th>
<th>13.33333</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ratio = x36</td>
<td>240.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x42</td>
<td>252.00 280.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x48</td>
<td>288.00 320.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x54</td>
<td>324.00 360.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x60</td>
<td>360.00 400.00</td>
<td></td>
</tr>
</tbody>
</table>

AHB/SDRAM frequency (MHz)

<table>
<thead>
<tr>
<th>Xtal (MHz)</th>
<th>12</th>
<th>13.33333</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ratio = x36</td>
<td>40.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x42</td>
<td>42.00 46.67</td>
<td></td>
</tr>
<tr>
<td>Ratio = x48</td>
<td>48.00 53.33</td>
<td></td>
</tr>
<tr>
<td>Ratio = x54</td>
<td>54.00 60.00</td>
<td></td>
</tr>
<tr>
<td>Ratio = x60</td>
<td>60.00 66.67</td>
<td></td>
</tr>
</tbody>
</table>
Design for Low Dynamic Power - DVFS

- Static Timing Analysis support
  - `pll_bypass` allows controllable clock path visibility for all derived SOC clocks without the STA tools needing to understand the 'black-box' functionality of the PLL components
- Simple static case analysis using externally controlled clocks and `testmode`
- Identified clocked state machine register outputs for synchronized resets and all derived clocks to allow named ports to be controlled with STA clock forcing

CPU Subsystem Clock Specifications (PLL_IEM domain)

The following clocks and clock generation protocols are required

- Free running AMBA clocks for AHB HCLK (also serves as APB PCLK in this design) This runs continuously and the processor and debug clocks are phase-aligned to this primary clock. All the synthesizable memory controllers and peripherals use this primary clock in the SOC design.

- Independent target processor clock frequency required to support Adaptive Power controller module with the frequency under the control of an external (asynchronous) dynamic power controller. This target frequency is set by the Intelligent Energy Controller to the desired processor frequency and used as part of the voltage control feedback loop to determine if the voltage is sufficient to safely support operation at this target performance level.

- Dynamically switching, glitch-free CPU clock carefully controlled to align with AHB transfer HCLK edges using HCLKEN enable. The CPU frequency is independently switched in frequency under control of the Intelligent Energy Controller in a phase-aligned manner to the free-running.

- Power management protocol support for isolation (interface signal clamping) and CPU sequencing and synchronous de-assertion of reset. Addition support is added to ensure that the CPU is always clocked for a minimum of three cycles after power-down prior to reset de-assertion – to meet the clock gating specifications on the CPU subsystem.

- Instantiate independently for each power domain and control the clocks and associated resets to this domain as well as controlling test configuration.
Energy efficient SOC design technology and methodology

Figure 3.8A – PLLx12 Clock generation:

```
clk_pll12
Q1 (:= Q6)
Q2 (:= Q1)
Q3 (:= Q2)
Q4 (:= Q3)
Q5 (:= Q4)
Q6 (:= Q5)
CPUx6 [100%]
HCLKENx6
CPUx4 [66%]
HCLKENx4
CPUx3 [50%]
HCLKENx3
```

Figure 3.8B – PLLx10 Clock generation:

```
clk_pll10
Q1 (:= Q5)
Q2 (:= Q1)
Q3 (:= Q2)
Q4 (:= Q3)
Q5 (:= Q4)
CPUx5 [83%]
HCLKENx5
```
Design for Low Dynamic Power- DVFS

**Detailed IEM System Clock Generation: CPU Clock Generator (a): CLKGEN_IEMx12**

When Dynamic Voltage Scaling is enabled the CPU clock must be dynamically reprogrammable to the supported frequencies between 0 and 100%. The primary clock generation for Maximum, Minimum and the bus clock rates is provided by CPUCLOCK1. This is clocked by the CPUPPLL1 (12x bus speed) clock.

To ensure the clock generator is fast and efficient the underlying divider is based on a 6-stage "twisted-ring counter" – a simple shift-register structure with inverted feedback loop (Referred to as a "Johnson Counter"5). Q1 to Q6 reflect the underlying HCLK bus frequency and can be tapped off for clock balancing for both the AHB IP and the SDRAM memory controller external device clock in particular.

This clock generator is able to produce the following CPU clock ratios:

- 6 x bus speed (6/6 = 100%, max performance)
- 4 x bus speed (4/6 = 66% of max performance)
- 3 x bus speed (3/6 = 50% of max performance)

At each frequency point the appropriate HCLKEN signal timing is generated which is the qualifier to indicate that the next rising edge of CPUCLOCK is aligned to the external HCLK bus IP transfer edge. See Fig 3.8A.

**Detailed IEM System Clock Generation: CPU Clock Generator (b): CLKGEN_IEMx10**

For energy efficiency at reduced performance and voltage an extra dynamic performance setting of 5/6 of maximum operating frequency is highly desirable. A second PLL clock at 10x the bus clock frequency is more power efficient than a single, much higher frequency, master PLL clock.

Again, for efficiency the clock generator is fast and efficient the underlying divider is based on a 5-stage Johnson counter (twisted ring counter). Q1 to Q5 reflect the underlying HCLK bus frequency and are synchronized to the master clock generator clock described in the previous section.

This clock generator is able to produce the following CPU clock ratios:

- 5 x bus speed (5/6 = 83% of max performance)

HCLKEN signal timing is generated which is the qualifier to indicate that the next rising edge of CPUCLOCK is aligned to the external HCLK bus IP transfer edge. See Fig 3.8B.

---

Energy efficient SOC design technology and methodology

Figure 3.9A – Latency Precompensation

DVS dependent clock latency

CPUCLK rising

HCLKEN active

re-clock outputs

sample inputs

AMBA HCLK

latched outputs
to AMBA
inputs from
AMBA

AHB cycle synthesis constraints

fixed length AMBA AHB cycle period
(Pre-)Compensating for DVS Clock Tree Latency variation

When scaling the voltage of a sub-system with an SOC not only do the set-up and hold times degrade with lower voltage but also the clock tree (clock enable, reset, etc.) latencies all scale in a non-insignificant manner.

Because the ARM926EJ CPU core used in this design has a synchronous bus interface this creates a challenge to ensure the rest of the SOC design can be completed with standard static timing analysis methodologies. The hardened processor core has a deep internal clock buffer tree and it is necessary to align the clocks for the maximum frequency (at worst case process and temperature and worst case max voltage) in order to meet performance at 100%, but avoid having to compensate for significant negative set-up times on inputs at lower voltages.

The approach adopted in this design is to advance the clock to the CPU sufficiently to guarantee that the CPU worst case latencies at the lowest reduced voltage and frequency operating point are met in advance of the AMBA HCLK rising edge.

All outputs from the DVS domain are guaranteed to be set up in advance of the rising edge of HCLK by design. A set of registers clocked by rising-HCLK are added on the 1.2V VDD SOC domain side of the level shifters that bridge the interface between the dynamic voltage scaled domain and the standard SOC design implementation for the rest of the chip.

This is shown in Fig 3.9A.

- In summary, the DVS-domain CPU is clocked in advance of HCLK rising by an amount guaranteed to exceed the worst-case low voltage latency and hold times.
- The AHB SOC subsystem is constrained to a tighter frequency to guarantee that all inputs to the DVS-domain CPU are valid for the worst-case low voltage latency and set-up times. This is not a difficult constraint to meet because the HCLK domain is run at the low-frequency of 1/6th of the primary CPU sign-off frequency [Normally the IP is synthesized for 133MHz HCLK and SDRAM controller clock rates].
- The addition of the retiming registers clocked by the rising edge of HCLK then guarantee there are no output hold time violations to the AMBA subsystem HCLK domain. These add minimal delays to the significantly slower low-to-high voltage level shifters.

The pre-compensation times for the CPU were determined from the worst-case latency analysis tabulated in Figure 3.2A.
Energy efficient SOC design technology and methodology

Figure 3.10A – Fmax Timing ‘strobes’ for AHB subsystem

Constrain AHB to CPU Fmax/4

Figure 3.10B Fmax DVS-mode Timing ‘strobes’

Constrain AHB to CPU Fmax/6

Figure 3.10C Fmin DVS-mode Timing ‘strobes’

Constrain AHB to CPU Fmin/2
Static Timing Analysis strategy

With CPU, RAM and SOC domains all set to standard voltage/dereating corners the timing analysis must be verified at CPU at Fmax

Then sign off the timing with new extended low-voltage slow-slow corner with CPU at Fmin

Current and Target clock generation

- **Figure 3.10A** shows the primary interface clock relationship with the CPU clock to the AHB bus clock in order to constrain bus read and write data access times correctly
  - The AHB clock period must be over-constrained to 4/6 of the cycle time in order to ensure input data (and read data in particular) will be valid and setup to the CPU edge that samples the data (when the HCLKEN qualifier is active)

- **Figure 3.10B** shows the primary interface clock relationship with the CPU clock enable in advance of each active (nsing-) edge of the AHB bus clock when the CPU is run at full voltage and at maximum frequency (6 x bus clock)

- **Figure 3.10C** shows the primary interface clock relationship with the CPU clock enable in advance of each active (nsing-) edge of the AHB bus clock when the CPU is run at lowest voltage and at reduced frequency (2 x bus clock)

With Dynamic Voltage Scaling the voltage/frequency operating points must not be violated - the CPU must never be clocked faster than the operating voltage supports. Typically a look-up table of voltages required to support each level of performance is provided to control the power supply and for guaranteed operation over temperature and process spread a conservative characterization process is required.

With Adaptive Voltage Scaling the operating voltage is made continuously adjustable such that it can be varied to compensate for process and temperature within the power supply control loop. In order to support dynamic performance scaling the concept of a secondary 'target' clock is introduced. When requesting to increase performance the CPU must be maintained at the current performance value while the target clock is used to probe a 'Hardware Performance Monitor' (HPM) of some form that is used in the power supply control feedback loop to ascertain when safe operating voltage at the new performance setting has stabilized. At this point it is safe to switch the processor to the higher frequency clock. When reducing performance the CPU and target clocks are immediately switched to the lower clock frequency and the power supply then reduces the operating voltage to support the new target frequency that is monitored by the HPM.

The clock generators must support concurrent clock synthesis of current and target frequencies.
Energy efficient SOC design technology and methodology

Figure 3.11A – Performance Level Request Coding

<table>
<thead>
<tr>
<th>Perf Level</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1xxxx</td>
<td>100%</td>
</tr>
<tr>
<td>01xxx</td>
<td>83%</td>
</tr>
<tr>
<td>001xx</td>
<td>66%</td>
</tr>
<tr>
<td>0001x</td>
<td>50%</td>
</tr>
<tr>
<td>00001</td>
<td>0% / Idle</td>
</tr>
</tbody>
</table>

Figure 3.11B – Voltage Ready Request Coding

<table>
<thead>
<tr>
<th>Voltage Ready</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1xxxx</td>
<td>100%</td>
</tr>
<tr>
<td>01xxx</td>
<td>83%</td>
</tr>
<tr>
<td>001xx</td>
<td>66%</td>
</tr>
<tr>
<td>0001x</td>
<td>50%</td>
</tr>
<tr>
<td>00001</td>
<td>0% / Idle</td>
</tr>
</tbody>
</table>

Figure 3.11C – Shift-register Design Implementation

![Shift-register Design Implementation Diagram]
Clock switching to the CPU must be clean and never violate minimum pulse widths at the selected current or target frequencies. The requirement to introduce the secondary PLL adds complexity and the approach adopted is to logically OR the clocks and clock enables between the two clock dividers and provide a synchronizer and handshake interface between the two (semi-synchronous) clock generators using an "active"/"hold-off" request acknowledge sequence.

**Dynamic Clock Control Interface Specification**

**Performance Level request**

Gray-coded 5-bit buses are used to convey the target performance clock setting from the Intelligent Energy Controller. These should be synchronized to the local domain clock before gating with the clock enables. See Figure 3.11A.

**Voltage Ready Level**

Gray-coded 5-bit buses are used to convey the safe operating voltage level at present from the Dynamic Voltage Controller. These should be synchronized to the local domain clock before gating with the clock enables. See Figure 3.11B.

**Dynamic Performance Monitoring**

The Intelligent Energy Controller should use the "AND" of the Target Performance level and the Voltage Ready buses to determine the currently active performance level. Although these control levels have a few cycles of synchronization penalty, there are no extended PLL out-of-lock delay times, so the performance switching is effectively instantaneous.

**Implementation Details**

A shift-register design for the clock generators is used. A pair of shift registers are preloaded with the appropriate clock and clock enable waveform every HCLK cycle for the selected target/CPU frequencies and this is then simply shifted out at the PLL clock rate. This keeps the implementation fast and efficient for the high-speed clock. Figure 3.11C shows the shift-register style design used for the ATLAS926 DVFS clock controller.

**Summary**

The challenges in designing for dynamic frequency and voltage scaling can be overcome but integration timing interfaces either need detailed design and careful timing verification — or need to be treated as asynchronous interfaces with associated cross-clock-domain handshakes or synchronizers. Although an efficient synchronous timing relationship can be designed in as described in this chapter, this does require expert design resource for SOC integration. The author chose to specify fully asynchronous interfaces for the ARM1176 IEM-ready product IP that is licensed commercially to customers.
Energy efficient SOC design technology and methodology
4. Design for State-Retention Power-Gating

Principles of Power-gating design methodology and flow

Leakage power dissipation grows every generation of CMOS process technology. This leakage power is not only a serious challenge to battery powered or portable products but increasingly an issue that has to be addressed in mains-powered or tethered equipment too where added leakage power generates increased heat and often requires specialized packaging or cooling.

It is highly desirable to add mechanisms to fully or partially switch the leaky power rails to reduce the leakage power that is dissipated.

In this chapter, a set of best practice approaches to architecting a SOC for one or more power-gated regions in a SOC are introduced and described in detail. The next chapter deals with the detailed transistor design and analysis issues as these are very technology dependent, here the primary interest is in understanding how RTL designers can design for power-gating implementations in as technology-independent and portable manner as possible.

RTL design conventionally assumes ideal power rails and logical communication between modules. Switching or gating the power rails needs special care and attention in the RTL partitioning coding and verification.

Dynamic and Leakage power profiles

Clock gating can be handled fairly transparently from an implementation and tools perspective, power-gating is more invasive than clock-gating in that it affects inter-block interface communication and adds in non insignificant time delays to safely enter and exit power gated modes.

For the purposes of describing power-gating principles in this chapter the concepts of entry and exit from such power modes are introduced:

- SLEEP events initiate entry to the low power mode
- WAKE events initiate return to active mode

Such events may be scheduled explicitly by control software as part of device drivers or operating system idle tasks, or alternatively initiated in hardware by timers or system level power management controllers.

System designers frequently choose more explicit and appropriate names, but the concepts should be clear from what follows.

Figure 4.1A shows an example activity profile for a sub-system that needs to be power managed. In the case of basic clock gating the leakage power component is shown at the base of the graph.

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Figure 4.1A – Activity profile with Clock Gating

Figure 4.1B – Activity profile with ideal Power-gating

Figure 4.1C – Activity profile with non-ideal Power-gating
Architecturally one is faced with trade-offs between
- the degree of leakage power savings that are possible
- the entry and exit time penalties incurred
- the energy dissipated entering and leaving such leakage saving modes
- the activity profile (proportion and frequency of times asleep or active)

Figure 4.1B shows an example activity profile for the same sub-system with basic power-gating implemented. The real-time response time between the WAKE event and having clocks running may be significant and cannot be ignored at the system design level.

Figure 4.1C shows more realistically the leakage power savings are not perfect and instantaneous, the full leakage power savings take some time to reach target levels due partly to the (hotter) thermal profile of the preceding activity and the non-ideal nature of the power-gating technology. Therefore the achievable savings are compromised to some extent.

Impact of Power-gating on classes of sub-system

A cached CPU subsystem for example can typically be dormant or inactive for long periods (Fig 4.2A)
- power-gating the entire CPU provides very good leakage power reduction
- but wake-up-time response to an interrupt has significant system level design implications (may even require deeper FIFO’s or scheduled time-slots)
- if the cache contents are lost every time the CPU is woken up then there is likely to be a significant energy cost in having to repeat all the bus activity to refill the cache
- net energy savings depend on the ‘sleep’/‘wake’ activity profile as to how much energy was saved when power gated versus that burnt in reloading state

Alternatively a peripheral subsystem may have a much better defined profile under control of a device driver and operating system power management scheme (Fig 4.2B)
- power-gating most of the block but maintaining key state may give best leakage power reduction
- the device driver may be required to explicitly load/restore key state or initiate hardware sequencer control
- the real-time and recovery costs can be easily profiled and optimized
- net energy savings are relatively easy to quantify from (existing) device driver statistics

Finally by way of illustration a more complex multi-processor CPU cluster would be an example of a hierarchical power-gating subsystem where one or more processors may be power gated off completely (Fig 4.2C)
- power-gating individual CPUs provides very good leakage system level power reduction
- in such an MP cluster, coherency has to be re-established when a CPU is re-powered. Therefore the fact that the local cache contents have been lost every time it was power gated in not a problem. The CPU is awoken clean and reset ready to execute and cache the next task it is given
- optimized net energy savings may well require adaptive shutdown algorithms that vary the number of CPU cores power gated and active with varying workload
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Figure 4.2A – Cached CPU sub-system

![Cached CPU sub-system diagram](image1)

Figure 4.2B – Peripheral sub-system

![Peripheral sub-system diagram](image2)

Figure 4.2C – Multi-processor CPU cluster sub-system

![Multi-processor CPU cluster sub-system diagram](image3)

Figure 4.2D – Functional Partitioning for Power-gating

![Functional Partitioning for Power-gating diagram](image4)

Figure 4.2E – Functional power gated subsystem packaged for integration

![Functional power gated subsystem packaged for integration diagram](image5)
Power-gating Design Partitioning

There are two parts to architect power-gating systems:

- the IP block(s) or subsystem(s) that will be power gated
- the controller that is responsible for sequencing the power control to the power-gated subsystem

The controller typically must be supplied with power from an "always-on" supply to ensure it has the ability to manage the Wake and Sleep interfaces on behalf of the power-gated block. The control signals for the power-gating hook-up need to be explicitly coded in the RTL and providing a defined control protocol is used may be verified with a protocol test-bench. See Fig 4.2D.

More often it may be desirable to package the IP-specific power controller with power managed block itself – as the power sequencing may be tailored to an implementation specific configuration rather than being a generic reusable component. However the hierarchical partitioning must be handled carefully to ensure the controller and power-gated portions can be cleanly mapped onto separate power supplies and even separate physical regions potentially. The implicit SOC-level power supplies are shown powering the controller and the power switching circuitry, and the concept of packaging the output isolation functionality with the module is introduced – ensuring that the composite component can be safely deployed in a SOC with clean safe logic outputs. See Fig 4.2E.

With more complex state retention mechanisms that may require functional state save and state restore operations then the power gated unit or module may have explicit control pins. Otherwise the interface for the power gated regions can be largely transparent to the RTL coding.

RTL Design for Power-gating

The primary considerations are the hierarchical partitioning of the design to ease the implementation and verification and the degree of power-gating granularity within the subsystem hierarchy. The concept of a power-island, or a bounded region of design hierarchy with controlled power rails, is introduced. Any region that is locally power gated or externally switched as a power rail introduces a set of constraints into the system design that affect not only dynamic and leakage power modes of operation, but also:

- the functional control of clocks and resets
- interface isolation
- implementation and analysis constraints
- state-dependent verification for each supported power state
- power state transition coverage to ensure all legal state entry and exit arcs are tested
- manufacturing and production test implications

The most basic form of power-gating control, and that with the lowest long-term leakage power, is that of providing an externally switched power rail. It is important to ensure that the SOC architecture provides clear hierarchical visibility of all switched power rails as this effects not only power but clocks, resets and any signals that pass through a power island.

Where a number of on-chip subsystems share a power rail the next level of refinement is to support on-chip power-gating at the complete subsystem level. Power-gating a complete subsystem is typically easier from an implementation and verification perspective - the larger the block that is switched the greater the leakage power savings for long periods of inactivity in general. This results in a number of power islands on a shared power supply rail.
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Figure 4.3A – Conceptual Hierarchical Power-gating

---

Figure 4.3B – Conceptual Hierarchical Power-gating Function Table

<table>
<thead>
<tr>
<th>Cache</th>
<th>CPU</th>
<th>MAC</th>
<th>VFP</th>
<th>Power State</th>
</tr>
</thead>
<tbody>
<tr>
<td>(OFF)</td>
<td>(OFF)</td>
<td>-</td>
<td>-</td>
<td>Shutdown (Cache cleaned, VDDCPU off)</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>-</td>
<td>-</td>
<td>Deep Sleep (Cache preserved)</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>Normal Operation</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>DSP workload</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>Graphics workload</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>Intensive multimedia mode</td>
</tr>
</tbody>
</table>

Figure 4.3C – Conceptual Hierarchical Power-gating

---

Figure 4.3D – Conceptual Hierarchical Power-gating Function Table

<table>
<thead>
<tr>
<th>Cache</th>
<th>CPU</th>
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<th>VFP</th>
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<td>(OFF)</td>
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<td>ON</td>
<td>Graphics workload</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>Intensive multimedia mode</td>
</tr>
</tbody>
</table>
However power-gating at finer granularity within the subsystem tends to provide optimal savings when certain functional units may be effectively turned off for even short periods. For example a complex co-processor in a CPU might be a good candidate for local power-gating if it is only used by certain threads on demand. Each sub-component of a sub-system needs to be treated as a true power island due to the interface boundary conditions and testability.

**Chip architecture for power-gating**

A scalable approach to chip architecture is valuable as a system-on-chip design today typically becomes a component in a larger or more complex integration in a subsequent product generation. It is recommended that module boundaries must be enforced at the power island level, even if more advanced EDA flows support process by process tagging of voltage and operating conditions. Ensuring one has clean visibility of the boundaries of a power-gated block for verification and testability purposes is important to ensure a clean top down implementation flow.

**Hierarchy and Power-gating**

Although one can in theory arbitrarily nest power gated modules within power gated subsystems which are in turn nested on a shared switched power rail, there are considerable benefits in not inferring multiple levels of power switching fabric. As will be described in Section 4.3 power-gating is intrusive and adds in some voltage drop and degradation of performance. Even if a functional power management view is presented at the architectural level the implementation is improved if this is mapped onto a single level of power-gating at implementation. For example a CPU conceptually has all the core logic power gated, and within it a number of functional units that can be individually powered down independently – a Multiply-Accumulate and a Vector Floating Point units in this case. See Fig 4.3A and Function table at Fig 4.3B.

From an implementation standpoint the switching fabric is flattened as shown below. There is never any case when the MAC or VFP functional units would be switched on without the CPU core itself so the switch control semantics are adjusted to AND the control terms rather than cascade the switch elements. See Fig 4.3C. The tabular power mode description now requires explicit control of the nested power gated functional units at Fig 4.3D.

**Recommendations:**

- Map power gated regions to explicit module boundaries
- When partitioning a hierarchical power-gating design ensure that the power-gating control terms can be mapped back to a flat switching control fabric rather than design to cascade power-gating more than one or two levels

**Pit-fails:**

- Avoid control signals passing through power-gated or power-down regions to other power regions that are not hierarchically switched with the first region
- Avoid excessively fine power-gating granularity unless absolutely required for aggressive leakage power management. Every interface adds implementation and verification challenges and complicates the system level production test challenges.
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Figure 4.4A - Power Networks and Control

Figure 4.4B - External Power Rail switching
Design for State-Retention Power-Gating - SRPG

**Power networks and their control**

In the design of a processor-based SOC the CPU system may well introduce a number of power networks

- An independent power rail to the entire cached CPU subsystem – this allows the CPU to be completely turned off for long-term "sleep" modes of operation
- Power gated supply to the logic to support short-term leakage savings modes where the cache memory can be left retained but all the leaky standard cell logic turned off locally
- Optionally support state-retention on registers in the standard cell portion of the design by some form of retention power supply from the non power gated rail
- Non power-gated supply to the control circuitry and buffering that supports the power-gating fabric itself and any state retention control signaling

Finally one will need a SOC-level supply that is always on to control the external rail switching handshake with the power supply - and optionally include the on-chip power-gating support on the same rail

The figure below illustrates the power networks with independent "VDDCPU" and "VDDSOC" that is always powered, sharing a common VSS ground connection. In this example the power-gated standard cell area has a non-gated state retention supply shown to indicate an active supply rail within a power gated region

See Fig 44A

**External power rail switching**

External power rail switching offers the best long-term leakage power savings – but introduces a significant turn-on delay to allow voltage regulation to stabilize and settle within specification

Only a few voltage rails can typically be externally switched, every power supply incurs (external) regulator cost and area on the circuit board – usually inductors and capacitors required to implement high-efficiency switched mode power supplies. Every power rail also requires on-chip power gnd or nng supplies that cost area and complicate the power planning and physical floor-planning. Most SOC's already have at least three power rails

- IO power (1.8/2.5/4.3V for external memory interfaces typically)
- "Always-on" SOC core rail (technology dependent logic and memory power rail)
- Clean analog power supply rail to PLL's etc
- Optionally one may have "keep-alive" voltage supply to real-time clock

Adding more than couple of external switch power rails adds significant complexity and end-product cost

Typically a shared ground /VSS connection approach to the chip and board works best for external power rail switching. Although there are typically independent VSS pins for both the IO pad-nng and the chip core in order to decouple the worst of any output simultaneous switching activity from the logic and memory these are typically grounded on the circuit board into a shared "0-volt" ground plane. Treating any other power supplies as switched positive supplies relative to the common ground minimizes complexities when adding power-gating. See Fig 44B
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Figure 4.5A – On-chip Virtual Rail Power-gating
Design for State-Retention Power-Gating - SRPG

External power rail switching incurs significant delays on wake-up events – from the order of tens of microseconds to milliseconds or even longer potentially. Seeking to specify much faster supply switching times is not necessarily desirable – the inrush currents to re-charge all the capacitive nodes in the power down subsystem result in noise injection into other (powered) regions of the chip and the resulting "ground-bounce" in a shared ground system can introduce problems that are hard to quantify until very late in the implementation and analysis parts of the design flow.

Translating such latencies into clock cycles at RTL level is not simple. Normally the clocks should be suppressed until a switched power rail is stable and within specified tolerance. For a design operating in the hundreds of MHz region this may be the equivalent of tens of thousands of clock cycles and with the actual delays being highly dependent on the power supply technology (that may have to be multi-sourced in a production).

Separate power rails become a necessity when one introduces the concepts of dynamic voltage scaling (Chapter 5). It may also be highly desirable in processor-based designs where large banks of memory can be given their own supply which may then be switched to intermediate RAM retention operating conditions for example.

Recommendations:

- Minimize the number of external switched independent power rails — each one must be justified from an end-product requirement given the associated additional power supply real-estate costs and on-chip power distribution
- Switched (positive) supply rails with a common ground — common VSS mesh
- In systems implementing voltage scaling an independent rail must be provided for each, and the power rail switching is simply mapped as an extreme case of the voltage scaling supply — to zero

Pit-falls:

- Design for significant external power rail switching times. Tens or hundreds of thousands of clock cycle latencies must be factored into wake-up and will be dependent on the external PSU specifications
- Although multiple rails appear elegant from a system design perspective they introduce verification and deployment challenges in production. Independent supply rails have independent voltage control regulators, and independent rails can exhibit vastly different load regulation characteristics when active, wait-stated or halted compared to logic powered at interfaces. Worst case conditions across interfaces need careful verification

On-chip power-gating

Given a restricted number of external (switched) power rails the on-chip power-gating further segments the supplies to functional areas of the hierarchy.

The terminology often used to describe power gated supply rails is that of "virtual rails". A power gated ground rail is that of a Virtual Ground or Virtual-VSS rail, while a power-gated supply rail would typically be referred to as a Virtual-VDD rail. See Fig 4.5A.
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Figure 4.6A – “Fine-Grain” Intra-cell Power-gating

```
VDD SUPPLY

"TURN ON"

VSS GROUND
```
On chip power-gating of a much smaller region of a design is potentially much faster but not instantaneous. The current required to re-power a small power gated region is much less significant than that typical for a full switch power rail but time must be budgeted to manage the minimization of power-gating transients and noise injection as seen by other logic and memory. Therefore it is realistic to see power-gating in terms of numbers of clock cycles for very small regions and tens or even hundreds of clock cycles for more significant gate counts. Trying to turn on a number of small power-gated regions at the same time is no better than a large block and this may lead to the requirement to have the power-gating of multiple independent sub-blocks centrally managed in order to ensure the delay times are minimized with respect to total sub-system demands. In the finest level of granularity the power-gating can even be factored with the standard cell library such that each (high-leakage) gate has a local power switch built in series with the power rail inside the cell. In theory the RTL designer needs to know nothing more than the fact that the cells have a very fast internal power-gating function built in – but it turns out that the designer will in fact have to handle the timing or delay of such functionality just as carefully to ensure that the implementation does not have over-constrained switching demands placed on the power-gating functionality. See Fig 4.6A. Power-gating has an impact on both performance and area, as will discussed in Chapter 4, due to the nature of the switching transistor fabric, so at the outset it must be understood that there may well be a headline-performance limitation compared to implementations that sit on an externally regulated voltage rail. Mapping on-chip power-gating to the cached processor example:

- Power rail to the cached CPU subsystem (externally switched potentially)
- Power gated supply to the CPU logic – a local Virtual-VDDCPU rail
- Non-power-gated supply to switching control sequencer and switch fabric buffering
- Non-power-gated supply to isolation regions and buffer trees
- Power gated supply to the CPU floating-point unit – a local Virtual-VDDVFP rail
- Power gated supply to the CPU Multiply-Accumulator – a local Virtual-VDDMAC rail

See retention support in later section of this chapter for details for additional control buffering and state preservation power requirements for non-power-gated supplies.

**Recommendations:**

- Design for technology-dependent power-gating times tens or hundreds of clock cycle latencies may require to be factored into wake-up times dependent on the area switched and the switching fabric control characteristics
- Therefore design for “wait-states” across boundaries where there are dynamically power gated functional units such that the implementation-dependent delay times can be safely managed and latency constraints set

**Pit-falls:**

- Every power-gated rail introduces verification and test challenges so the number of power gated regions needs to be carefully justified and factored into project timescales
- Although multiple power-gated supplies appear elegant from a system design perspective introduce verification and deployment challenges in production. Each power gated rail requires independent control sequencing, and introduces “wait-state” implications across boundaries that require independent verification
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Figure 4.7A – Basic (PMOS) Header Switch

Figure 4.7B – Basic (NMOS) Footer Switch
"Header" and "Footer" switches

The transistor structures for power-gating are described in Chapter 4. The switches are highly technology specific. A lot of the academic papers on "MTCMOS" - Multi-Threshold CMOS where high-Vt switches are used as series power switches for faster leaky low-Vt gates – advocate both P-channel "Header" switches gating the VDD supply and N-channel "Footer" switches gating the VSS ground. However, two such high-Vt power switches in series with the gate do cause a more significant IR voltage drop in the supply as seen by the gate. In many practical designs where performance cannot be sacrificed unduly switching of only the supply rail or the ground can be tolerated. The leakage current reduction comes from the first of any switches added.

The basic Header Switch is shown in Fig 4.7A, footer switch in Fig 4.7B.

With Header switch fabric the internal nodes and outputs of a power gated block collapse down towards the ground rail, with footer switches the internal nodes and outputs all charge towards the supply rail. There is no guarantee the power gated nodes will ever fully discharge to ground or charge to the supply as equilibrium is reached when the leakage currents through the switches are balanced by the sub-threshold leakage of the switched cells.

Recommendations.

- Only bother switching the supply rail or ground, rather than both, dependent on the appropriate switch fabric characteristics for the technology in order to minimize the IR drop due to power-gating.
- Decide early on in the design phase whether header or footer switches most naturally fits with the system design as this will affect the isolation and interface protocols across the power gated interfaces.
- Header switches are the most appropriate choice for switches if they are power-gating an externally switched power-rail. This ensures that outputs behave the same whether power gated or externally switched and the input parking condition is consistent regardless of the "depth of sleep".
- In systems implementing voltage scaling header-switches are favourable. Level shifters typically share a common ground across interfaces, therefore using a virtual-VDD rail and a common ground maintains consistency when it comes to clamping signals at boundaries whether scaling or gating power supplies.

Pit-falls:

- Seek to avoid "sneak paths" between driven inputs and header or footer power gated regions that inject current into the inputs of switched if the "natural" discharge potential is the opposite sense (e.g. active-high signals asserted into header-switched region when these are power down).
- Beware of mixing "virtual-ground" power-gating with externally switched power rails or voltage scaling. This results in sleep mode-dependent input and output states.
Energy efficient SOC design technology and methodology
Power-gating control networks

The control networks for power-gating at the RTL level are not straightforward. The control sequencing needs to be explicit and match the technology-dependent control of the power switching fabric. The power-gated portion of the design typically is transparent to this, much in the way that scan testability is not visible in the RTL and implementation-specific ports for scan data and enable(s) only appear later in the implementation flow.

In the implementation, such power control networks are typically high-fanout nets that have implied buffer trees. Such buffer trees need to be powered from the primary rail, not the power-gated virtual rail, to ensure all power switches see valid and safe drive signals. If there are multiple control nets for phased turn-on of networks, as discussed in Chapter 5, then multiple control ports must be made explicit in the RTL design and careful hook-up of such control ports to the power-gating fabric netlist supported in the implementation and verification methodologies.

Best practice RTL design will require the designer to ensure controllability of resets for testability. Ideally, all derived or resynchronized resets (or presets) are multiplexed from an external controllable primary reset control pin, or with reduced test coverage inhibit asynchronous reset assertion when configured in a test access mode.

For similar reasons, the designer needs to provide controllability of power-gating control networks. It is crucial that scan test patterns cannot accidentally toggle state machine outputs that activate power-gating of subsystems. Power control signals therefore need to be gated or multiplexed when in test rather than functional mode, and optionally controlled externally if power-gating leakage analysis is to be performed on a tester.

From a verification standpoint, assertions and coverage should be added in order to validate the correct sequencing and polarity of the control networks.

Recommendations and Pitfalls for power-gating control

Recommendations:

- Explicit control in the RTL controller needs to be tailored to the technology-specific power-gating fabric chosen.
- Assertions should be provided for the power-gating control ports, to match the chosen switch technology to ensure function verification and coverage in the RTL design environment before the power-gating fabric is implemented.
- Power-gating control signals must be made controllable during test.

Pitfalls:

- Uncontrollable power-gating control signals may well break testability later in the implementation flow.
- Hierarchical designs with power-gating networks that pass through power-rail switched regions have the potential to construct power-gating control networks that function in power-gating but fail with rail switching.
Energy efficient SOC design technology and methodology

Figure 4.9A - Basic (AND) Clamp-Low Isolation cell

Figure 4.9B - Basic (OR) Clamp-High Isolation cell

Figure 4.9C - Basic (Pull-Down) Clamp-Low

Figure 4.9D - Basic (Pull-Up) Clamp-High

Figure 4.9E - Intra-cell clamp high in Fine-Grain footer-switched cell
Power domain Interface signal isolations methods

Every interface to a power gated region needs management of the signals that traverse this boundary and outputs that are unsafe or un-driven are the primary concern

Signal Isolation
Power-gated or externally switched power rails result in outputs that exhibit non-logic values. Worse than ‘X’ values in simulation, these un-driven outputs are unsafe inputs of non-power-gated logic and can cause high currents to flow in the gates that constitute the receiving interface, and potentially may even “crow-bar” that supply rail. When using header switches for power-gating an AND-gate function which forces the power-gated signal low is what is required to park the output safely at logic ‘0’, with footer switches the desired function is that of an OR-gate function which parks the output at logic ‘1’. Clamp library cells must be designed to ensure they cause no sneak leakage paths when the input that is power gated floats, and typically they have extra attributes that EDA tools need to ensure these never get optimized away, buffered incorrectly or inverted as part of logic optimization.

Conceptual AND-style isolation clamp-low, when “VALID” is true, signal passes to output, when false output is clamped low shown in Fig 4.9A.

Conceptual OR-style isolation clamp-high, when “INVALID” is true, output is clamped high, when false signal passes to output shown in Fig 4.9B.

Special purpose clamp gates as described do add delay on potentially add to critical paths – for example on cache memory interfaces that interface to power gated control logic. A low-cost alternative that does not add full gate delays appears to be that of a much simpler pull-down transistor clamp when using header switches, or pull-up transistor clamp when using footer switches that forces the power gated signal to the parked value without actually intercepting it. However this effectively introduces multiple drivers on the power gated net that require careful sequencing to avoid contention when switching, and exclusive logical control at power up. Even if the pull-up or pull-down transistors are relatively weak devices the total number may become significant.

Conceptual pull-down style clamp-low, when “INVALID” is true, output is clamped low, when false signal passes to output shown in Fig 4.9C.

Conceptual pull-up style clamp-high, when “VALID” is true, signal passes to output, when false output is clamped high shown in Fig 4.9D.

In the simple fine-grain switched cell the same control signal can potentially be used to turn-off the power footer switch say and enable the pull-up as the layout and timing can minimize contention, it is not possible to guarantee this for layout-dependent networks. An example fine-grain cell with footer power switch and integrated output pull-up is shown in Fig 4.9E.

Finally, ideally one wants to isolate outputs until power-gating has stabilized to avoid output glitches and this is obviously logically possible with the clamp cells but not with pull transistors that would fight the output values whenever these powered back up in an active state.

Therefore pull-up and pull-down clamps are not recommended despite the lower area and timing cost for portable RTL design, and the “gate-style” cell styles are favored, and described in the rest of this section. However with careful use these have value in specialized situations where the signalling protocols are understood and the pull-up or pull-down clamps do not cause contention by design when enabled.
Figure 4.10A – Power-gating and clamping

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INPUTS FORCED "LOW" WHEN ISOLATED

VDD SUPPLY

'TURN OFF'

GATED VDD

Power-Gated Region

OUTPUTS DRIVEN "LOW" (INACTIVE) WHEN ISOLATED
Output or Input Isolation

As explained, it is the electrical problem of floating outputs that must be addressed. Clamping at the output or the input appears to make little difference functionally but there are pros and cons either way.

Library isolation cells or clamps typically require to be placed in the power domain that remains powered relative to the power gated region. And the EDA tools and implementation methodology for any control signal buffeting or output drive strength optimization phases need to respect this.

Isolating or clamping a power-gated output to a safe level allows the cases of fan-out to multiple inputs to be handled cleanly in one place. Isolating the inputs in the powered domain may well result in duplication of the clamp functionality multiple times.

Therefore it is desirable to limit fan-out across power gated interfaces to a minimum and ensures clean implementation visibility of where signals may safely be buffered (after the isolation clamp not before).

From the reusable IP perspective the desirability of integrated clamps "within" the subsystem such that the complications of isolation or non-logic value signals are hidden from the SOC-level integration interfaces has been introduced earlier. From an RTL design perspective this requires that a "VDDSOC" power rail interface module is introduced into the design that can be mapped to the appropriate power domain and all the isolation clamps and any local high fan-out net buffeting can be implemented in this region.

Interface Protocols

Inputs to power-gated region do not require explicit isolation for fear of electrical failure or breakdown but applying clocks or driven inputs to a power domain effectively waste power by charging up some nodes that then leak back into the power gated ground or current return path.

Therefore it is desirable to define the module boundaries between power-gated regions in the RTL design with interface signalling that maintains the best state-dependent leakage states across interfaces when isolated for power-gating.

Taking the example of power-gating regions using header switches, the preference is for active-high interface signal protocols. The de-assertion case then matches the preferred isolation clamp values for parking signals. Parking the clock at zero is ideal because then the clock network is driven low logically before power-gating which then minimizes leakage currents into this high buffer strength network.

The only RTL design level exception to the active-high signalling preference for header-switched regions is that of resets. When powering back up after power-gating, registers will typically need to be reset (see State Retention section later for qualification of this) to initialize state correctly. By having an active-low reset asserted through power-gating and the stabilization period when power is reapplied correct behaviour is guaranteed. Most standard cell registers are available with active low asynchronous set or reset control inputs so this is a natural fit. In fact as long the module boundaries are specified in the RTL to have active high signalling and active low reset protocols then the appropriate buffer tree inversions can then be handled in the implementation regardless of the actual library cell preferences. See Fig 4.10A.

For footer-switched power-gated regions the inverse is in fact true. With a virtual-ground the protocols that fit naturally at the interfaces are active-low signalling and active high asynchronous resets. Again specifying this in the RTL interface descriptions then ensures that the implementation flow handles any inversions or preferences.

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Energy efficient SOC design technology and methodology
Design for State-Retention Power-Gating - SRPG

Recommendations and Pitfalls for power-gating interface isolation

Recommendations:

- Minimize the output fan-out across power-gated interfaces. Point-to-point power-gated output to isolation receiver minimizes timing closure and buffering.
- Design for isolation cells on interfaces rather than pull-up or pull-down style clamps unless using very specialized interface protocols (where the "multiple-driver" challenges are worth the implementation complications).

Assuming a power gated or externally switched power rail and common ground:

- Specify active-high signalling protocols on outputs, such that the "parked" or isolated condition of 'zeros' on outputs is avoided.
- Specify active-high clocking and signalling protocols on inputs, to avoid wasting power dissipation in the power-gated module.
- The exception to active high signal levels is that of asynchronous resets. Active-low reset(s) that cleanly asserted before the power is switched off and de-asserted after power is restored provide guaranteed initialization behaviour (See the State Retention section for more complex reset and state restore factors).
- Minimize the output fan-out across power-gated interfaces. Point-to-point power-gated output to isolation receiver minimizes timing closure and buffering.

Alternatively, for a gated or switched ground and common supply rail:

- Specify active-low signalling protocols on outputs, such that the "parked" or isolated condition of 'ones' on outputs is avoided.
- Specify active-low clocking and signalling protocols on inputs, to avoid wasting power dissipation in the power-gated module.
- Active high asynchronous resets fit most naturally with switched ground approaches and should be asserted before the power is switched off and de-asserted after power is restored and stable (See the State Retention section for more complex reset and state restore factors).

Pitfalls:

- Isolation clamps on outputs will behave as expected when locally power-gated. But if the power rail can be externally switched for alternative modes of power saving then these clamps could become un-powered and result in floating outputs despite the clamp in the design.
- Isolation clamps on clocks between voltage regions tend to force a single point of entry into a subsystem Clock tree balancing on either side if the isolation clamp becomes an issue if there is a wide fan-out on the clock in the island that remains powered.
Energy efficient SOC design technology and methodology
State retention and restoration methods

State retention with power-gating is more challenging to support in a seamless way but can be highly desirable. Although in some cases one can afford to power off a subsystem, throw away all state and simply apply reset to re-initialize the block when power is reapplied, there is typically an energy or real-time cost in resuming operation.

Retaining the state of registers over a sleep/wake power-gated episode is both power efficient and may reduce wake-up latency, compared to losing all register state and having to reset the power-gated subsystem, and run again without any contextual state built up over time.

How essential this is depends on the subsystem characteristics. A Digital Signal Processing unit that is primarily data-flow driven may usefully be able to start afresh supplied with new input data. However a peripheral or cached processor typically has a lot of residual state, and it may well be waste time and energy to require a significant amount of bus traffic to reload the state that was lost.

Although one could use software approaches to reading specific register state and saving it away to memory, and subsequently reading it back and writing it back into the registers, which may be appropriate in some cases, this section focuses on hardware solutions that may be transparently overlaid on an RTL design.

State Retention with Power-gating, or SRPG as it is often referred to, builds on the basic power-gating described so far and is able to offer the potential of the illusion to that of clock gating, an RTL design resumes with the state it had at the last active event (the state just before the sleep event that initiated the power-gating).

RTL design relies on the principle of latches or registers that exhibit state preservation or retention between activation events in some form of “Shadow” register. The explicit activation events in RTL are basically the clocks and resets into a process that infers registered state, and in the case of transparent latches sensitivity lists that includes enables and data terms for inferred level sensitive storage, for example.

Clock gating can be overlaid on such RTL designs simply by intercepting the clock and suppressing clock pulses whenever the particular enable term for the register is not active. Providing the reset and enable terms have been coded cleanly for synthesis in the RTL description the register state values exhibit the same behaviour when implemented with clock gating tools and implementation methodologies. There is an area cost associated with the clock gating latches that need to be implemented when gating clocks, but this is offset typically by the power saving that is gained by suppressing clock edges to flip-flops that have their clocks gated.

Retention Registers

An elegant approach to providing state retention while power-gating is to replace a standard register with a special version that supports a locally “always-powered” island with some form of “shadow register” that can preserve and restore the register state between power sleep and wake events.

A D-type flip flop is typically built as a Master-Slave pair of latches, often optimized for speed and minimum setup and hold times to the sampling clock edge. Library designers and vendors have come up with a number of variants of retention registers that trade off the performance and area costs to support state retention functionality. This may involve a third latch implemented in High-Vt technology with some extra control functionality to capture and restore state to the high-speed register core. Alternatively the slave latch may be isolated and become the retention node at some cost to the clock-to-output timing.
The "RET" box indicates the additional retention latch with associated control signals to support saving and restoring the register state.
Whatever the library element approach some form of control interface must be added to the register to allow the suppression of clocks or state saving and restoring functionality, and this may well impose extra constraints on in which state the clock must be for save and restore functionality.

In the simplest approach one could imagine constraining the implementation to only using High-Vt registers, connecting these to the un-switched power rail, and simply power-gating all the leaky (Low- or Mixed-Vt) combinational logic between register stages from the power gated power rail. However in any reasonable sized block the reset and clock networks typically have to be implemented with high-leakage low-Vt buffer trees which contribute a significant portion of the leakage for the block, as soon as these high fanout nets are power gated then the clocks and resets float and would corrupt standard registers.

Real-world retention registers do all have some area overhead, typically 20-30% larger. If they incorporate guard bands to isolate the retention state as robustly as possible from power-gating transients then the area increase may be much greater, potentially as much as 50%. In a design with a large proportion of registers the area impact can be significant.

In addition to the area overhead there is a control requirement as well. From a control IP perspective there are one or more extra signals required to drive to sequence state capture and control, and rarely can these be shared with the power-gating control line, for safe operation the save state operation and more problematically the safe restoration of state back to the main storage element need to be safely away from the power-gating transients and unknown propagation.

Examples of control signal approaches include:

- a pair of level sensitive signals of the form of Save and Restore
- a single edge-sensitive Retain control that capture on one edge and restores on the other

By way of example a conceptual register with conventional reset and scan multiplexing is show opposite. A retention latch structure is incorporated – with a non-power gated power supply connection not shown – and control signals to support copying the active register state into this shadow latch before power-gating, and restoring the state value after power-gating before restarting the clock. See Fig 4.13A.

Designers are used to the fact that registers with integrated scan multiplexers can automatically be substituted and hooked up later in the implementation flow. From the perspective of the power gated region this is the ideal abstraction for full state retention. The control signals need to be implemented as always-on networks to avoid state corruption during periods of power-gating but otherwise can be treated transparently to the RTL design.

However the control IP must manage the explicit sequencing of the save and restore signalling as part of the power management control state machine.

One other detail needs understanding from the RTL design perspective. RTL coding for synthesis requires that asynchronous resets have precedence over the clock edge and clock gating terms, retention transparent to the RTL design requires that neither the clock nor reset is activated during retention. Given that both clock and reset trees are likely to be power gated and uncontrollable during power down for best leakage power saving, there is an underlying assumption that retention has priority over clock and reset.

Evaluation of the available cells in the power-gating library is important to ensure the high-level retention scheme coded into the RTL design is not corrupted in implementation due to floating clocks and resets.
Energy efficient SOC design technology and methodology
Partial and Full State Retention

Full state retention has been described and from a methodology perspective so far As long as clean control sequencing is provided it is possible to make RTL design behave transparently with respect to state retention All state is guaranteed to be the same before and after power gating

Partial state retention appears much more attractive If only the "architecturally visible" state is saved and restored then the associated retention register area cost should be much more acceptable However this adds verification complexity to ensure that the interaction of retained and non-retained state is always legal and safe – and cannot result in state-machine deadlock or lost data of value

Best practice RTL design advocates storage that can be initialized – typically with asynchronous set or reset top level signals With partial retention this becomes mandatory because the state space is too large to prove that all X's can be safely flushed in a design from many retained state conditions as opposed to just from (power-on) reset

In order to design RTL that is portable across different styles of retention register, where, for example the precedence of reset may be higher than that of state retention controlled save and restore, it becomes important to separate out the reset signals explicitly for retention and non retention storage It then becomes possible to architect fully the "power-on-reset" full initialization and the restart function after power-gating to restore retained state for retention areas and initialized all the non retention registers that would otherwise come back with "X" values

The power control sequencer for partial retention must therefore drive independent (named) resets to the appropriate portions of the subsystem Some rigorous functional testing will be required to ensure that there are no illegal combinations of states that might cause deadlock

A more subtle complication arises from a potential interaction with clock gating that will be implemented further down the design flow All the state bits that make up clock gating enable terms need to be retained themselves or be re-initialized to a safe and restart-able condition such that the transparent latch contents of integrated clock gating library cells can cleanly be regenerated – without the requirement to require retention-enabled variants of clock gates as well

State Retention using standard Scan-Flops

Scan chains that are implemented for manufacturing test are potentially reusable as a mechanism to emulate state retention without any register area overhead except for some extra control sequencing It becomes possible to implement the design using standard multiplexed scan-flops and once state is scanned out the entire subsystem can be power gated off

From an RTL design perspective there are of course challenges The number of registers is typically only known after initial implementation (including optimization of constant value registers for example)

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2 Keating, M "Reuse Methodology Manual", (see Bibliography)
Energy efficient SOC design technology and methodology

Figure 4.1A - Retention using manufacturing scan chains

Figure 4.1B - RTL Emulation of scan retention state

```verbatim
#define CPU_SCAN_LEN 257 /* set to implementation length once known */

ifdef RTL_SLEEP_EMULATE
parameter scan_reg_length = `CPU_SCAN_LEN;
reg [15:0] scanword [0:scan_reg_length-1];
integer i;

initial /* initialize the scan chain to count pattern, or more draconian X */
begin
    for (i=0; i < scan_reg_length; i=i+1)
        begin
            scanword[i]<=i; // or 16'hXXXX;
        end
end

always@(posedge CLX) /* emulate scan shift CPUSI -> CPUSO */
begin
    if (CPUSE == 1'b1) /* when controlled SCAN ENABLE is active */
        begin
            for (i=1; i < scan_reg_length; i=i+1)
                begin
                    scanword[i]<=scanword[i-1];
                end
            scanword[0] <= CPUSI[15:0];
        end
    assign CPUSO [15:0] = scanword[scan_reg_length-1];
endif
```
Therefore the control sequencer needs to be parameterized to manage implementation-dependent counters, and explicit control of scan enable and scan chains needs to provided that will later be hooked up with the net-list

- The state needs to be saved somewhere so an on-chip or off-chip area of memory is typically required sufficient to hold the number of scanned bits required to hold the state during retention.
- There is a real-time delay cost in both saving and restoring state, and this grows depending on the size of the block to be scanned out and back in, and is a function of how many scan chains are to be implemented.
- If more than one chain is used (typically byte- or bus-width is more efficient) then it is necessary to add sufficient extra registers to balance up the scan chains such that they can share the same shift enable signal.
- There is also an energy cost in shifting out and back in the register state. Typically the patterns shifted are highly state dependent on the condition the subsystem was at the request for sleep. In the pathological case the worst case patterns must be handled to ensure that the dynamic power and IR voltage drop constraints are not violated.
- For long term sleep the lower leakage power of power-gating of power-rail switching an entire subsystem yet supporting state restored continuation can be highly desirable from a product perspective compared to the energy costs of restarting with all state reset after power-gating.

An example simplified to 4-bit save and restore data is shown below. If the number of scan chains does not divide exactly by the width of the retention scan data path then one or more flops must be added. When balanced the state can be saved to memory ("write data") and later restored from memory ("read data") such that every register has the original state bit re-scanned. See Fig 4.15A.

Functional testing and simulation at the RTL level before netlist implementation is a challenge, but not insurmountable. One approach is to add some conditional code into the RTL design which is only compiled in for simulation when emulating scan-based retention. Behaviour at shift registers are modeled and can be implemented with simple test sequences or even checksums to verify that exactly the same state is reloaded that was saved for example.

An example of providing an RTL model of a CPU to be implemented with 16 scan chains for retention support that can allow early verification of the control functionality is shown in Fig 4.15B. At a later stage a netlist simulation should be performed to ensure that the implementation-specific scan chains and control signals really are wired up correctly and that the correct length scan chain has been implemented and balanced.
Energy efficient SOC design technology and methodology
Recommendations and Pitfalls for state retention

Recommendations

- State retention has the potential to offer very fast wake-up times after power-gating and allow transparent continuation. This has to be traded off against an impact on the implementation sequential cell area.
- Ideally implement full-retention at the module level rather than specific sequential processed in order to end up with a block-level verification approach.
- Ideally register all inputs to a state retention module or region as this the ensure that all internal clock gating enable terms can be regenerated after power-gating – which is essential to ensure clock gating behaves correctly in the implementation flow.
- Ensure that all registers in a full or partial retention design can be initialized. Registers without set or reset functionality can be tolerated in designs that can be exhaustively tested from power-on-reset, but with retention the state space grows beyond what can be verified.
- Retention controls must be made controllable during scan test.
- If partial retention is implemented then it is strongly advised that separate resets are coded for the retained and the non-retained storage portions of the design. This allows clean verification visibility of power on reset and restore/re-initialize operation.
- When implementing partial retention ensure that state machines and sequencers have no dependencies on non-retained state, in order to avoid state-dependent deadlock or invalid state conditions. (The state space to verify can be enormous if many retention state values must be tested with non-retained state).
- Where the area impact of specialized retention registers is too high then reusing the manufacturing scan chains is a realistic option. Although this requires some care to map cleanly onto netlist implementation after test structures have been generated this can be managed relatively cleanly in RTL-coded control state machines.

Pit-falls

- Poor power-gating inrush current management or retention power supplies noise have the potential to corrupt retention registers resulting in unsafe/invalid state on restart. Great care must be taken in the RTL power control to ensure power is reapplied to power down blocks safely and gently.
- Partial retention requires much more rigorous reset and restore validation to ensure there are never deadlock conditions between maintained (architectural) state and re-initialized non-retained state.
- Clock gating enable terms that affect retention state themselves need to have retention registers on their entire fan-in state in order to ensure that “next state” sequencing behaves correctly.
- Using both edges of the clock in a design with retention is strongly discouraged. Clock gating elements have internal transparent latch structures and these potentially fail if power gated. As soon as both edges of the clock are used, some integrated clock gates will be required to retain their enable state rather than to be able to resample this from logic terms based on retention or reinitialized registers.
- In the case of scan-based save and restore care needs to be taken to ensure any bus-based serialization of data can support wait-states. Scan-enable is a very basic form of serialization control and any generic or reusable design requires the clock to be started and stopped on demand in order to ensure there is never any data loss on scanning state in and out.
Figure 4.17A – Power-gating Control sequencing

CLOCK
N_ISOLATE
N_RESET
N_PWRON

Figure 4.17B – Power-gating Control sequencing with Retention

CLOCK
N_ISOLATE
SAVE
N_PWRON
RESTORE
Design for State-Retention Power-Gating - SRPG

**Power-gating control**

Having described the aspects of designing subsystems for power-gating without and with power-gating we turn to the explicit RTL that is required to control the additional functionality.

**Power control sequencing**

Putting together the power-gating and retention control requirements the RTL sequencing details become clear.

To power gate a region without retention:
- Flush through any bus or external operations in progress
- Stop the clocks, in the appropriate phase to minimize leakage into the power-gated region
- Assert the isolation control signal to park all outputs in safe condition
- Assert the power-gating control signal to power down the block

To restore power:
- De-assert the power-gating control signal to power back up the block
  - Optionally sequence multiple control signals for phased power-up depending on the current inrush management approach and technology
- De-assert reset to ensure clean initialization following the gated power-up
- Assert the state retention restore condition (pulse or edge-triggered is technology dependent)
- De-assert the isolation control signal to restore all outputs
- Restart the clocks, without glitches or violating minimum pulse width design constraints

The sequence is shown in waveform representation at Fig 4.17A

To power gate a region with retention:
- Flush through any bus or external operations in progress
- Stop the clocks, in the appropriate phase to minimize leakage into the power-gated region
- Assert the state retention save condition (pulse or edge-triggered is technology dependent)
- Assert the isolation control signal to park all outputs in safe condition
- Assert the power-gating control signal to power down the block

To restore power and retained state:
- De-assert the power-gating control signal to power back up the block
  - Optionally sequence multiple control signals for phased power-up depending on the current inrush management approach and technology
- De-assert reset to ensure clean initialization following the gated power-up
- Assert the state retention restore condition (pulse or edge-triggered is technology dependent)
- De-assert the isolation control signal to restore all outputs
- Restart the clocks, without glitches or violating minimum pulse width design constraints

The sequence is shown in waveform representation at Fig 4.17B

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Energy efficient SOC design technology and methodology

Figure 4 18A – Power-gating Control with Request and Acknowledge
Design for State-Retention Power-Gating - SRPG

Handshake Protocols

As has been made clear earlier in this chapter, power-gating takes time and safe switching and settling times must be designed into the controller IP. The simplest way is to embed synchronous delay or counters into the control IP to add in enough clock cycles to meet the power up or power down times. However embedding such time constants in the RTL makes the IP reusability or portability much harder — even on migrating a working product design onto a next generation technology node where the power-gating transistor characteristics affect timing. For best practice it is advisable to design in both request and acknowledge or “power valid” interface signals to support double edge synchronization handshaking between power being requested and subsequently acknowledged as safe.

In simple small power gated blocks one might just tie the power request back to the request. In more aggressive designs where analog IP is provided in the power control fabric to sense when gated power rails are safe and within specification then the acknowledge is driven directly by these. The advantage is that one does not have to design for the worst case delays because the sensing can be adaptive to the environmental conditions and how partially discharged a power gated region is. The sequence is shown in waveform representation at Fig 4.18A. Designing in such acknowledge handshakes into the control IP leaves open the implementation options as wide as possible and allows the selection of implementation technology to be handled later.

Recommendations and Pitfalls for power-gating controllers

Recommendations:

- Design the control sequencers or state with request and acknowledge handshakes for reuse across different generations of power-gating technology.
- Build in interlocks to ensure safe wake-up the time when a region is in the process of power-gating (i.e. synchronize both edges of power request and acknowledge to ensure the control does not overrun the switch fabric and control networks).
- Any power-gating acknowledge timing is technology and network area dependent so should be synchronized to the sequencer clock (unless such a low clock speed is used that this asynchronous timing would never be a problem).

Pit-falls

- Because powering down is typically dependent on semiconductor process and temperature the “hazardous” case is typically in the time window if an IP block is just being put to sleep when a wake up condition occurs before the block is fully power gated.
- Partial retention of state requires great care, and for verification purposes will ideally require independent resets to retention and non-retention register state.
Energy efficient SOC design technology and methodology

Figure 4.19A – RTL coding suitable for power-gating post-processing

```verilog
always @ (posedge clk or negedge nrst) begin
    if (!nrst)
        state <= 4'b0101;
    else
        state <= next_state;
end
```

Figure 4.19B – RTL coding after power-gating post-processing

```verilog
always @ (posedge clk or negedge nrst)
    ifdef RTL_PG_EMULATE
        or negedge PWR
    endif
) begin
    ifdef RTL_PG_EMULATE
        if (!PWR)
            state <= 4'bXXXX;
        else
            endif
    ifdef RTL_PG_EMULATE
        if (!nrst)
            state <= 4'b0101;
        else
            state <= next_state;
    else
        endif
```
Power-gating design verification – RTL simulation

Providing one uses a rigorous RTL coding style and consistent naming scheme for clocks and resets then it is possible to automatically annotate synthesizable RTL code with simple scripts to provide:

- functional modelling of power-gating (including forcing outputs to X when power gated)
- functional modelling of save and restore
- functional modelling of the precedence of power-gating/retention/reset

This is highly desirable for functional testing and allows test code and vectors to be generated for both the RTL and the implementation net-list.

Inferring Power-gating Behaviour in RTL

Providing a consistent clean (RMM\(^3\) compliant) design style has been used to code up a consistent asynchronous reset (or set) and synchronous clocking style to all sequential statements in the RTL subsystem then it is possible to script a conditional set of power-gating and behaviours that allow rigorous simulation modelling:

- Force ‘X’ on all state outputs when power-gated (potentially when not PWR_REQ or PWR_ACK)
- Ensure state is set to ‘X’ by power-gating to verify that explicit reset resets state after power-gating
- Model correctly the priorities of power-gating/reset/clocking to ensure correct sequencing

Providing the asynchronous “initialization” section of the RTL has been coded cleanly then it has proved straightforward to augment the RTL to infer simulation behaviour to match the netlist:

e.g. RTL for synthesis shown in Fig 4.19A.

This can be automatically converted to code to support simulation testing with power-gating controller RTL as shown in Fig 4.19B.

When simulating with RTL\_PG\_EMULATE defined the RTL control of the PWR power-gating (enabled) RTL input is added to the sensitivity list and as the highest priority term in the sequential process descriptions forces state unknown whenever power is removed (PWR deasserted).

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\(^3\) Keating, M. “Reuse Methodology Manual”, (see Bibliography)
Energy efficient SOC design technology and methodology

Figure 4.20A – RTL coding suitable for retention post-processing

```verilog
always @(posedge clk or negedge nrst) begin
    if (!nrst)
        state <= 4'b0101;
    else
        state <= next_state;
end
```

Figure 4.20B – RTL coding after retention post-processing

```verilog
`ifdef RTL_PG_EMULATE
    reg [3:0] state_SAVE = 4'bXXX; // declare new state
    wire PWR;
    assign PWR = pwr_req & pwr_ack;
`endif

always @(posedge clk or negedge nrst)
    if (!pwr)
        state <= 4'bXXXX;
    else if (SAVE)
        state_SAVE <= state;
    else if (!NRESTORE)
        state <= state_SAVE;
    else
        `ifdef RTL_PG_EMULATE
            if (!pwr)
                state <= 4'bXXXX;
            else if (SAVE)
                state_SAVE <= state;
            else if (!NRESTORE)
                state <= state_SAVE;
            else
                `endif
            `endif
        if (!nrst)
            state <= 4'b0101;
        else
            state <= next_state;
end
```

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Design for State-Retention Power-Gating - SRPG

Inferring Power-gating and Retention Behaviour in RTL

Providing a consistent clean (RMM compliant) design style has been used to code up a consistent asynchronous reset (or set) and synchronous clocking style to all sequential statements in the RTL subsystem then it is possible to script a conditional set of power-gating and retention behaviours that allows rigorous simulation modelling

- Force ‘X’ on all state outputs when power-gated (potentially when not PWR_REQ or PWR_ACK)
- Sample state to extra inferred retention state variables for “SAVE” operation
- Re-initialize state from retention state variables on “RESTORE” operation
- Initialize retention state variables to ‘X’ to capture invalid RESTORE before SAVE operation
- Model correctly the priorities of power-gating/retention/reset-clocking to ensure correct sequencing

Providing the asynchronous “initialization” section of the RTL has been coded cleanly then it has proved straightforward to augment the RTL to infer simulation behaviour to match the netlist e.g. RTL for synthesis shown in Fig 4.20A

This can be automatically converted to code of the form shown in Fig 4.20B

When simulating with RTL_PG_EMULATE defined the RTL control of the PWR power-gating (enabled) RTL input is added to the sensitivity list together with an active-high SAVE and an active-low NRESTORE pair of signals in this example, chosen to match the retention library IP components. Added shadow state variables are instantiated and the save and restore and power-gating priorities are added to the sequential process descriptions to model in RTL the underlying behaviour

An example perl script is included in Appendix-A to show how the simply automation of the adding of this template code to cleanly coded RTL has been achieved

Design For Test considerations

Standard best-practice considerations are primarily about providing test modes that make clocks and resets externally controllable such that standard Automatic Test Pattern Generation tools can generate high coverage test vectors

The primary additional consideration for the system and RTL designer is to extend these DFT rules for State-Retention Power-Gating. The additional questions that need to be posed are

- Power-gating switch functionality – fully switch on and off?
- Isolation functionality – are isolation interfaces safely low leakage, buffered and driven correctly?
- Retention-register functionality – clean state save, retain and restore operation?
- Control signal connectivity for all the above – do controls and handshakes correctly control the analogue switching?
Energy efficient SOC design technology and methodology
Power Gates and DFT

Functional problems that need checking at implementation time are basic things such as control signal polarity and ensuring that control buffers are all on the correct power domains etc. Manufacturing problems are tougher. Control buffer or switch transistor faults may lead either to some power gates not being switched on properly – resulting in IR-drop “hot-spots” in the gated power rails to some cells, or one or more power gates that are permanently on that then cause leakage power modes to malfunction and potentially result in product standby battery time failures.

As has been recommended earlier in this chapter making (all) power-gating externally controllable ensures that the power-gates controls do not get inadvertently switched when shifting in scan patterns.

At-speed testing is the only automated way of ensuring that power-gated regions behave correctly. Any poor impedance or broken switches will tend to induce timing faults in critical paths. From a DFT perspective this usually requires slightly specialized test control of clock switching between signal scan clocks that set up the register state scenarios for path testing and the functional at-speed clocks that capture state at full performance.

Providing a mechanism is provided to turn off power-gates externally then a fairly coarse quiescent current measurement test (IDDQ) may be possible to support in production testing where standby battery life is a major concern. But such tests are expensive in terms of timing and given that the leakage spread across process on shrinking geometries this may have to be approached later in the assembled product test flow.

Functional test vectors to cover the control state machine sequencing are the best way of proving that the control state machines have no breaks in connectivity or stuck-at-zero/-one faults. These are also very valuable in the early implementation flow testing to make sure that the correct signal polarities between the explicit RTL state machine controllers and the technology-specific power switching fabric have been correctly understood and connected.

When more complex power gate control structures are employed, as in the case of sequenced slow weak turn-on followed by strong low-impedance power-gating then functional test is required in order to ensure that any switching transients are managed properly and void potential corruption of retained state that is described in the next section.

Isolation and DFT

Isolation or clamping across power-gated interface boundaries should be straightforward from a functional test perspective. The implementation and verification flow must provide the power rail integrity checking that buffer trees are implemented on the correct power supply etc. The functional test coverage required from the RTL perspective is to ensure that the correct sequencing is applied to the power gated interfaces and that the correct control signal polarity is used with the technology specific isolation cells in the library.

There is only extra requirement from the RTL design perspective, interface clamping signals are typically controlled by state machine register outputs so these need to be made controllable so that that clamp signals are not inadvertently toggled during scan test.
Energy efficient SOC design technology and methodology
State Retention

The state save, hold and restore functionality are typically controlled by state machine register outputs. If these are not made explicitly controllable then shifting patterns through the sequencing logic on one power domain may cause the scan flops to stop behaving as scan flops in the power gated region.

Functional and manufacturing tests require proof that both zeroes and ones can be safely captured and restored, and ideally the state can be senally scanned to prove retention latch integrity.

Therefore making the retention control mechanisms visible to the test tools is important. Mapping these to external pins may not always be possible so some form of coded test mode control inputs may be the best alternative to allow ATPG tools to gain visibility and controllability.

Functional test vectors to cover the control state machine sequencing are the best way of proving that the control state machines have no breaks in connectivity or stuck-at faults in the save and restore networks. These are also very valuable in the early implementation flow testing to make sure that the correct signal polarities between the explicit RTL state machine controllers and the technology-specific state capture and restore functions have been correctly understood and connected.

As described in the preceding section, power gating must be functionally sequenced correctly to avoid sudden IR-drop transients that could corrupt retention registers inadvertently.

In the case of scan-based state retention, this has to be tested with functional vectors to guarantee that the scan-flops have been correctly balanced, the scan chain lengths do indeed match the RTL-implemented counters and that there are no arbitrary inversions or scan test control functions that have crept in from the implementation flow. Finally, such functional test vectors are important to ensure that any unknown propagation does not "leak" into the net-list due to incorrect isolation or un-initialized storage.

Recommendations and Pitfalls for SRPG DFT

Recommendations:
- Clock and reset signals must be made externally controllable during test
- Power-gating control signals must also be made externally controllable during test
- Isolation control signals need to be made controllable during scan test
- Retention controls must be made controllable during scan test
- Functional test programs/vectors are validated on an RTL emulation of the final design
- Support for externally IDDQ on visible power rails in the case where "stuck-on" power gates could potentially cause product malfunction in the end-customer system

Pit-falls:
- Power gated quiescent current measurements can only be "relative" to full-on current measurements due to the wide spread in leakage currents across fabrication process
Energy efficient SOC design technology and methodology

Figure 4.23A – Power State Machine design for SALT90G project

```
“WAKE” Events

“TURBO”
RUN
With Wells Forward-biased

“HALT”
Idle
With Clocks Stopped

“NORMAL”
RUN
With standard Well-Bias

“SNOOZE”
Idle
State Retention
Power Gating

“POWERSAVER”
RUN
With Wells Back-biased

“HIBERNATE”
Idle
Scan Retention
External Power Rail Switching

“SLEEP”
Event

RESET

“SHUTDOWN”
Idle
External Power Rail Switching of CPU and Cache RAMs

WAKE

“NORMAL”

“HALT”

“SNOOZE”

“POWERSAVER”

“SHUTDOWN”

RESET

“TURBO”

“NORMAL”

“HALT”

“POWERSAVER”

“SHUTDOWN”

“SLEEP”
```
Design for State-Retention Power-Gating - SRPG

Power-Gating/State-Retention in the SALT project

The SALT technology demonstrator project was used to evaluate and determine the best-practice approaches to power-gating and state retention that have been described in this chapter. In this section more details on the system design and RTL for this 90nm technology node are described as well as some of the lessons learned that have been described more generically in the pitfalls to beware of.

Leakage modes supported

Most battery-powered ARM-processor based designs have to deal carefully with the balance between sufficient performance to support product features which tends to require more leaky process technology versus the need to provide a number of leakage power reduction "stand-by" modes that trade-off depth of sleep with real-time penalties and cost of energy to enter and exit such power states. For the SALT project four low-power modes were designed. In order of increasing leakage savings - and real-time/recovery energy characteristics:

- **HALT** SLEEP causes architectural clock gating, fast WAKE restart
- **SNOOZE** State Retention Power-gating entry on SLEEP, WAKE as fast as power-gating safely allows The Cache memory state is preserved, logic is power gated
- **HIBERNATE** scan-based State Save to memory and allow VDDCPU power rail switch-off on SLEEP, scan-based signal restore on WAKE when power rail switched back on A 32-bit AMBA-based bus protocol was used to block write to SOC memory-map and block read back A 32-bit CRC was added to provide integrity checking that is saved away with the scanned data and used to protect against restarting with corrupted state via an error mechanism The Cache memory state is preserved, logic is powered down
- **SHUTDOWN** The only mode not transparent to the operating system Explicit cache clean code must be called to write back any dirty data in the cache memories before both the VDDCPU and VDDRAM supplies can power be power-rail switched

In addition support for active leakage reduction was included to support externally managed threshold scaling using back-bias control. Both P- and N-wells for the CPU standard cell area were exposed at pin-level to support experimental analysis of delay and leakage power characteristics.

No "multi-dimensional" delay models for both supply and dynamic well-bias threshold scaling were available or feasible to generate, so a set of delay de-rating curves were derived from characterizing the library cells while sweeping the P and N well bias voltages, and from this a realistic constrained upper frequency limit was determined for the CPU in this "power saver" mode of operation. In addition a "Turbo" mode of operation with some forward bias was also evaluated to support a higher-leakage mode of operation for (short-term) peak performance operation. The latter mode of operation would need on-chip thermal management to avoid potential thermal runaway, but was valuable from an experimental implementation test case.

The system design was then enhanced to enforce state changes between "normal" and back- or forward biased modes of active power management to go through HALT/SNOOZE/HIBERNATE state changes in order to ensure that well-bias voltages were only changed while the design was static and un-clocked, as shown in Fig 4.23A.
Figure 4.24A – Power domain partitioning for SALT90G project

Figure 4.24B – IP re-partitioning for SALT90G project CPU subsystem
Design partitioning

The RTL design was partitioned to allow the three primary power supplies to be mapped to the RTL design:
- **VDDSOC** is the "always-on supply" that powers the digital side of the PLLs, the clock generators and the power management control blocks, plus all the real-time peripherals including real-time clock and timers that can generate wake-up events as part of their interrupt service requests.
  - Within this power domain the USB OTG subsystem is power gated to evaluate RTL approaches to isolation and power-gating control (State retention in local RAM).
- **VDDRAM** is an external switched power rail that supplies the Cache and MMU RAMs. In this project this also allowed detailed leakage and active power consumption profiles to be measured and allowed (limited) reduced voltage headroom retention analysis.
- **VDDCPU** is an external switched power rail that supplies the CPU standard cell area. Support was included for both full state-retention with power-gating, providing fast local leakage reduction, and scan-based full state save and restore enabling external power rail switching to cut leakage completely. In this project the separated supply also allowed detailed leakage and active power consumption profiles to be measured as well as the energy cost functions to get in and out of each power saving state.

See Fig 4.24A

Subsequently the CPU sub-system design was re-implemented to ease design re-use. The Bus Interface and State Retention/Power-Gating controller are integrated into a "VDDSOC" region that is grouped with the CPU such that only VDDSOC interface signals are visible to the SOC-level design. Although this makes the 4-supply-rail CPU subsystem slightly more complex to implement the timing and internal power-gating and isolation interfaces are then all abstracted away from the top-level SOC design. Any changes or enhancements to the low-power states support by the IP block are properly independent of the top level system design providing the wait-state and handshake protocols with the top level clock generator are cleanly defined. See Fig 4.24B

Power-gating control and handshakes

The CPU power-gating control system was initially designed as a top-level module that managed the interfaces to the external power supplies, local header-switch power-gating control, isolation, state retention and the handshake with the system clock generator to switch CPU clock frequencies and manage bus-clock synchronous scan clock pulses for hibernation save and restore functionality.

In the state diagram included below the "SNOOZE" states are all labeled "LSLEEP" as the light sleep SRPG control, and the "HIBERNATE" states labeled as "DSLEEP" for the deep sleep control flow.

In order to support a wide range of power management library components and current in-rush management experiments every control signal, whether for power-gating, isolation, of save, restore and even reset, was driven as a request signal and had an explicit acknowledge signal. All the acknowledge signals were treated as asynchronous and had local synchronizers to the state machine clock domain.

This ensured the design was free of locally coded delays or counts and allowed the acknowledge signals to be tied direct to the requests for some implementations or built as true handshakes when signal buffered nets were implemented for some control schemes - which also provided some form of integrity check on control signal connectivity.

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A couple of design notes that may prove interesting

- The initialization sequence pulses the save/restore signalling to flush out any X-s from the shadow retention flops. This may be useful when running functional test programs or vectors on net-list.
- All timing-dependent state machine transitions include a holding term that waits for the output asserted in that state to be acknowledged in order to maintain the timing-independent request/acknowledge sequencing.
- The power-gating assertion and de-assertion is ‘demand-driven’. In the SALT project there were extra diagnostic control inputs to control the switch fabric which allow the power-gating to be soft-sequenced or forced fully on and off, and only the power-gating acknowledge input to the state machine is used to determine when power is safely restored.

See Fig 4.25A

Isolation

Several different isolation techniques were employed in the project.

The VDDRAM region had input isolation cells instantiated as "Genenc Library Cells", which are in fact wrappers for either behaviour al simulation models or technology-specific clamp cells from the underlying "Power Management Kit" for the standard cell library. This provided explicit instantiation of the cells on the (many) critical path signals into the memories from the CPU core logic, and supported clean visibility of the clocks and select signals that need to be managed carefully in the implementation flow. Clock balancing across isolation cells is not straightforward as such cells typically limit the flexibility the clock buffering tools have to restructure the buffer trees.

The VDDCPU included specialized output isolation cells that pulled down all output signals at the interface when locally power-gating, to guarantee clean SOC interface signals. However when the CPU rail is switched off (Hibernate) these isolation cells lose their VDDCPU power and the outputs could again float; simple bus repeater or "hold-" cells were added in the VDDSOC interface to avoid any further gate delays on the interface, and the bus interface module had explicit resets asserted by the isolate control signal to force logic-0 clamping of all bus interface protocol signals.

Separate RTL isolation signals were used for the RAM and CPU regions in order to avoid the potential problems of an routing an "always-on" clamp control signal through the potentially power-rail-switched CPU to get to the RAM, even though both signals were driven by the same state machine output port.

The OTG block used the alternative of instantiated "AND" gate cells in the RTL with suitable "don't-touch" attributes added to prevent logical optimization across these isolation boundaries.

Subsequently these isolation interfaces have been managed completely transparently to the RTL by adding suitable isolation attributes to the module-level supported by later EDA tools, but for basic functional simulation and verification there is merit in wrapping the clamp functionality in a technology-independent wrapper module which allows EDA-independent design portability to FPGA and SOC tool flows for example.
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Figure 4.26A – RTL post-processing for single-pin NRETAIN ret’n flops

```verilog
`ifdef RTL_PG_EMULATE
  reg [3:0] state_SAVE = 4'bXXXX; // declare new state
  wire PWR;
  assign PWR = pwr_req & pwr_ack;
`endif

always @(posedge clk or negedge nrst)

`ifdef RTL_PG_EMULATE

  or negedge PWR or negedge NRETAIN

`endif

) begin

`ifdef RTL_PG_EMULATE

  if (!PWR)
    state <= 4'bXXXX;
  else if (!NRETAIN)
    state <= state_SAVE;
  else
    `endif

if (!nrst)

  state <= 4'b0101;
else

  state <= next_state;
end

`ifdef RTL_PG_EMULATE

always @(negedge NRETAIN) // capture state on falling NRETAIN

  state_SAVE <= state;
`endif
```

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Retention
The SALT project incorporated a number of techniques to evaluate the area/time/energy cost functions for different approaches to allow comparison and analysis on the same silicon, as many designers.

Full state retention was implemented for the CPU. Given a fully validated CPU core the only safe approach to verifying that the processor could be restarted with arbitrary control and data state was to maintain every register bit state. The option of adding a separate reset or reinitialize signal for “non-architectural” state (i.e. the programmer’s model) was not feasible without a serious verification project phase.

In order to understand the soft-error effects of uncontrolled turn-on power-gating a non-real-time diagnostic mechanism was introduced into the power control sequencing to allow not only SRPG save and restore to be controlled normally but also re-use the “Hibernate” scan functionality to check-sum and save away and the entire register state after SAVE operation and then checksum and save away the entire register contents after RESTORE operation. This allowed error analysis for both random and location sensitive problems and the efficacy of the soft-start power-gating sequencing when not over-ridden. This turned out to be a valuable way of quantifying the safety margins of the retention flops and allowed them to be subjected to thermal and voltage shocks while in retention mode.

On the other hand the USB OTG core is partitioned with persistent USB end-point data held in SRAM while all state in the control state machines and FIFO interfaces to the PHY are transitory. Therefore it is not required to provide retention registers for the power-gated logic providing the control state machine guarantees to flush any transmit or receive buffers to the PHY interface before power-gating, and reinitializes all register state when restoring gated power.

The RTL annotation scheme was adapted to forces X-s at outputs on power-gating and on all register state to ensure correct reset sequencing when waking up after power-gating. The OTG block can indicate able to sleep so that a device driver knows when it is power-gating the core, but the block can be awoken by USB activity detected in the PHY. Verifying the associated tight real-time constraints are met to ensure retention was not required resulted in a significant amount of simulation work to prove that from power-gating to re-initialization to restart was within the USB specifications.

Inferring Power-gating and retention behaviour to RTL for single-pin control retention flops
In the SALT project the retention register library elements had a single-pin control to manage save and restore in an edge-triggered manner. Retention state is captured on the falling edge of an active-low NRETAIN signal and restored on rising-edge of the same NRETAIN:

Building on the same worked example described in section 4.7 the retention register intent could be inferred on the synthesizable RTL by post-processing the source files:

See Figure 4.26A.
Energy efficient SOC design technology and methodology

Figure 4.27A – RTL post-processing for single-pin NRETAIN ret’n flops

```c
PG_ARM926EJ_1616 PG_ARM926EJ_1616 ( ...

// main SOC interface
  .pwr_override(diag_pwr_override),
  .pwr_req(cpu_pwr),
  .pwr_ack(cpu_pwr_ack),
  .save(cpu_save),
  .nrestore(cpu_nrestore),

#ifdef RTL_PG_EMULATE
  .cpuclk(clk_cpu & -(diag_pwrstate[12:11]), // inhibit clock edges
          .cpuresetn(nrst_cpu (|diag_pwrstate[12:10]))), // inhibit asynch reset
  .dbgnrst(nrst_cpu_dbg (|diag_pwrstate[12:10])), // inhibit asynch reset
#else
  .cpuclk(clk_cpu),
  .cpuresetn(nrst_cpu),
  .dbgnrst(nrst_cpu_dbg),
#endif

...
Emulating state-retention power-gating of RTL sub-systems

If one does not have access to the source RTL which is often the case for many designers working with high-value IP components then this is a real issue. For many ARM-based designs the end-customer works with a pre-compiled/obfuscated technology-independent behaviour al model of the CPU and only later switches in the detailed technology specific version that may be provided from an internal IP implementation group or a Foundry for example.

So an alternative approach, when working with subsystems that have encrypted or protected IP models, is to intercept the clocks and resets to the module and emulate retention and state retention in the early design and verification flow.

In the SALT project the leakage management power controller had some high-order flags in the state field that reflect whether the processor is power gated or in hibernation-scan control. In this case a conditional set of connections to the clock and reset(s) is coded which inhibits the clock (AND out the clock term) and the active-low resets (OR in a reset inhibit) such that the RTL or event driven model has all clock and reset transitions inhibited during the power-gating and scan sequencing that would otherwise spuriously advance or re-initialize state.

See Fig 427A.
Energy efficient SOC design technology and methodology
5. Physical IP for Low Power Design

The DVS926 and follow on ULTRA926 projects drove the specification both of library components for dynamic power management and the extended voltage scaling characterization requirements for the full standard cell libraries and memory compiler technology.

For the 90nm and 65nm node technology demonstrators, leakage mitigation was the primary challenge and the ATLAS926 and SALT926 projects provided vehicles to evaluate both fine-grain (intra-cell) power gating and coarse-grain shared power switch networks respectively, as well as a number of different state retention approaches.

All the chips with the exception of the TSMC ATLAS926 project were implemented with physical IP from Artisan Components. Artisan was a collaboration partner for the first three projects, but had been acquired by ARM before the SALT926 project, so the latter project allowed cell-level engineering and experimentation rather than being constrained to customer deliverables and views.

Library IP Support for Dynamic Voltage and Frequency Scaling

The primary components specified and negotiated as add-on cells to the Standard Cell libraries include:

- Low-to-High Level Shifters
  - Active components with dual VDD supply rails to provide correct voltage-swing drive from a lower supply voltage to a higher supply rail.
  - These are often instantiated on critical timing interfaces (between cache RAMs and core logic in a CPU for example) so need to be as fast and efficient as possible.
  - From a methodology perspective these components were specified to be placed in the (output buffer) driver voltage domain – the rail with the higher current supply.
  - Optionally specified either with or without guard-bands between the voltage domains, the area overhead is significant with guard bands but for a number of customers this is preferred to smaller shifters without the guard-band safety.

- High-to-Low Level Shifters
  - In fact simply re-characterized cells that overdrive a weak voltage domain in a lower supply domain from a higher voltage domain.
  - No "bidirectional" capability of supporting arbitrary High/Low to High/Low Shifting.
  - Rigorous methodology enforced to ensure direction always clear and defined.

- Isolation or "Clamp" Gates
  - Support power-down regions for isolating interface signals from floating nets.
  - AND-type functionality chosen to clamp active-high signals to inactive.
  - This matched most naturally the shared-ground multiple VDD shifter architecture.

- Level shifters with Integrated Isolation clamping
  - A valuable “boundary” EDA cell variant for DVS interfaces with power-down.
Energy efficient SOC design technology and methodology

Figure 5.1A - Novel Buffered Header Power Switch

Figure 5.1B - Novel Buffered Header Power Switch - double height
Physical IP for Low Power Design

From a memory perspective, where typically the voltage scaling headroom was negligible or certainly less than the standard cell library voltage scaling range:

- RAMs with integrated input Level shifters
  - Emulated by “pseudo-hardening” discrete Low-to-High level shifters with integrated isolation clamps around standard complied RAM until compilers could be augmented to tile such shifters automatically
  - Proved invaluable to get good multi-voltage timing closure across independent logic and memory domains – any latency variation between voltage regions minimized by design.

Standard cell libraries required extended voltage characterization:

- Most simply an extra set of “Non-linear Delay Model” (NLDM) timing files were required to be characterized at a couple of fixed reduced operating voltage points; the voltages are highly technology dependent and expensive to build on-demand for customers however.
- Synopsys was proposing “Scalable Polynomial Delay Models” (SPDM) around the time of the DVS926 project – these allowed accurate delay interpolation for intermediate operating voltages but turned out to be very expensive in terms of machine time required to build the underlying polynomial delay characteristics.
- Current Source models are now the favoured industry approach – Synopsys have not only “Composite Current Source” (CCS) models for timing but also for power and noise; these are much more efficient to build from a library provider perspective but still involve huge quantities of data, even in the timing libraries that package this up for customer design views.

All the technology demonstrator projects covered in this report were in fact signed-off using NLDM timing and power library views but are proving valuable test cases for CCS timing and power closure subsequently.

Library IP Support for (MTCMOS) Power Gating

The favoured approach to power gating has been distributed shared P-MOS header switching. Although N-MOS footer switches have higher electron mobility for the 90 and 65nm technologies targeted for the leakage demonstrators the system-level benefits of shared ground throughout, and therefore standardizing on active high signalling with clamping to zero, was the driving factor.

Fig 5.1A shows the underlying header switch design approach, with the integrating buffering supporting ease of chaining or cascading switches without added “always-on” control networks, and the ability to add some internal switching control path delay to avoid peak inrush switch currents by design.

Fig 5.1B shows the switch layout optimized for area and switch efficiency; the double height cell layout allowed sharing of the inverter chains to minimize area impact, and the switches were implemented as many “fingers” of transistors to get the best on-current to leakage ratio – here optimized for 90nm TSMC Generic technology.
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Figure 5.2A – Distributing Virtual and Un-switched Power

Figure 5.2B – Novel Buffered Header Power Switch with Weak-Start
The approach taken with the entire prototype power gating library was to add an extra track in addition to the "normal" power rail. An existing 9-track library was used as the starting point and a tenth power track added – not ideal from a cell area perspective – but avoiding all the challenges of supplying "always-on" supply to retention flops and the control buffer networks to control power gating, isolation and retention that must not themselves be power gated or "float".

The dual-height Header switch is designed to sit under a low-impedance VDD power mesh and locally switch (a pair of) Virtual-VDD rails, VVDD. Although a number of experiments were conducted with strategies to use columns of switches to turn on each VVDD row at a time, the only safe strategy adopted was to provide a controlled turn-on of the VVDD as a gridded supply allowing best current sharing between switches to minimize "hot-spots" for voltage drop. The switch cell is shown supporting virtual rail grid connectivity by switch cell abutment.

A final complication shown in Fig 5.1B is that of the switch providing the Well-taps for the adjacent library cells in a final layout. A tap-less baseline cell library was used for the project; the area efficiency of cells in improved by not having well ties explicitly provided inside each cell, but this adds a requirement in the EDA flow that well ties or tap cells must be added within technology-dependent radii of such cells to ensure they behave correctly as originally characterized.

Incorporating the well ties into the switch cells guaranteed that the well connections could be made by design providing they were placed less than 75 micron distant from each other (radially) for the 90nm technology for this project. Because the project was to exploit variable well bias evaluation the P-well and N-well connections are again chained together by abutment.

Fig 5.2A shows examples of how the underlying cell library was converted for 9-track to the experimental 10-track variant with distributed always-on VDD distribution. Conventional cells such as the INVX1 inverter shown simply had a dummy 10-th track (VDD) added and their pre-existing track-9 supply is renamed VVDD; when this virtual rail is switched off the cell loses power with associated reduction in leakage current.

An extra set of "Un-gated" power cells which were given a "U-" prefix were introduced into the library: a higher-strength non-inverting buffer, UBUFX6, is shown alongside the inverter. This is simply rewired to use the always-on VDD supply track 10 rather than track 9 that the parent (BUFX6) library cell used to clone this cell variant.

All cells in the new 10-track library variant have to be re-characterized to take account of the extra parasitic capacitance and to update the cell area parametrics.

Fig 5.2B shows the double-height switch cell enhanced to include a specialized start-up circuit that supports connection by abutment of not only the standard switch structures but also a buffered control chain that feeds a turn-on request "up" the chain and returns an acknowledge back down the chain to support placement-controlled turn-on management. The starter network only turns on a set of three weak switch "fingers" while the remaining 27 fingers are turned on by the main chained switch control to provide the low-IR switch functionality once the virtual grid is safely powered up.
Energy efficient SOC design technology and methodology

Figure 5.3A – Schmitt Trigger Virtual Rail Sensing

Figure 5.3B – Soft-start weak transistor header switch network

Figure 5.3C – Low IR-drop strong transistor header switch network
The SALT virtual power grid switches were developed and simulated using trial loads of standard cells instantiated in between column switches arranged in columns every 50um to match the standard power supply vertical metal pitch for standard single voltage designs.

For the trial implementations the virtual power grid switch network for the SALT926 CPU was:

- Standard cell area: 280 rows x 2000um wide area
  - 50 um column switch grid (to start with)
  - Switches ~ 6.5um wide
  - 11200 switches (5600 double height cells in fact)
  - 72800 um of switch cell
  - 36.5 rows of switches in total
- Total current capacity is high (typ conditions) for 50mV drop
  - 11.42uA/switch x 5600 = 63.9mA
  - Gate current 520.3 pA/switch x 5600 = 2.9uA

The approach of over-designing the power gating in order to guarantee no local high current IR-drop hot-spots was chosen to reduce risk, with the knowledge that in an optimized solution smaller current switches could be selectively be swapped in once the high current cell placements were analyzed – which would then reduce the off-current leakage compared to the initial grid.

Because the design was to implement retention registers which must not be corrupted by turn-on currents in the power gating grid (considerable given the complete capacitance of all power gated cells once these have been gated off and discharged) an active approach to inrush transient management was taken for the project:

A Virtual VDD grid-sensing Schmitt trigger cell was specified – see Fig 5.3A.

- Analog voltage-sense cell for the Virtual-VDD supply rail
  - Generate a “VVDD-ready” signal when start-up voltage reaches ~ 90%
- Integrated AND-gate to allow gating “ready” with “nSLEEP”
  - One cell sufficient to control main power gating network
  - Necessary in order to ensure turn-off time not dependent on network discharge.
- A diagnostic override (OR-gating) structure to allow instantaneous “ready” signalling
  - To allow experimental analysis of retention state soft error rates with and without soft-turn on sensing.

Fig 5.3B shows the chained structure implemented by script-based placement of the weak starter switch structures – in this case distributed every 10 switch columns, and with their control path chained serially to provide a gentle turn-on characteristic.

Fig 5.3C shows conceptually how the high-current switch columns are arranged and controlled, and only turned on once the level-sensing Schmitt trigger indicates the starter network is on and safe to turn on the strong header switches. Only on starter column is shown for this part of the VVDD grid switch network, which is simply a replication of further switch columns to the right of this.
Energy efficient SOC design technology and methodology

Figure 5.4A - Column-based Switch Fabric Deployment

Figure 5.4B - Close-up of optimized connection by abutment
The SALT virtual power switch grid is only one example of how such a shared or distributed power gating network might be built – e.g. Row-switches rather than the Column approach of Fig 5.4A. The project determined four classes of power gating implementation each of which requires more EDA tools support but more appropriate for synthesizable IP design flows:

"Concealed" Power Gating
- Custom 10 Track Library (easy distribution of true VDD)
- SALT project header switch example - "physical only" cells
- Not in the netlist – hard to analyze
- Pre-placed by perl script
- Connection by abutment, as shown in Fig 5.4B.
- Power domains in RTL Hierarchy, need manual power gating control hook-up

"Explicit" Power Gating
- Standard 9-Track library (VDD must be explicitly routed)
- Fully characterized headers (pre-production Power Management Kit)
- Switches exist in the netlist – can be analyzed
- Pre-placed by perl script
- Connection by pre routing in back-end router
- Power domains in RTL hierarchy, again need manual power gating control hook-up

"Inferred" Power Gating
- Standard 9-Track library (tap-less)
- Fully characterized headers (pre-production Power Management Kit)
- In the netlist – can be analyzed
- Automatically placed and routed by synthesis tools
- Minimal switch topology scripting – intelligence now in the tools
- Power domains inferred from RTL

"Automated" Power Gating
- Standard 9-Track library (90GT)
- Fully characterized headers (production Power Management Kit)
- In the netlist – can be analyzed
- Automatically placed and routed by front-end synthesis tools
- Require minimal IC-Compiler (Synopsys synthesis/place & route) scripting
- Power domains specified during implementation

Library IP Characterization for Power Gating

Adding switches in series with power rails results in context-sensitive voltage drop for power-gated library cells. One approach would simply be to over-constrain the timing in order to compensate for some level of IR drop that would only be known once the layout and extraction is complete.
Energy efficient SOC design technology and methodology

Figure 5.5A – Single-pin control Retention Register – single height

Figure 5.5B – StateSaver Retention Register – Double Height
For the project the base library was re-characterized at 5% and 10% voltage derating from the standard voltage sign-off conditions: for the 90nm library that has worst-case voltage corner specification of 0.9V (1.0V nominal minus 10% voltage), two more worst case timing libraries were built:

- 0.85V, slow corner, highest temperature
- 0.80V, slow corner, highest temperature

Re-synthesizing and routing the ARM926 CPU configuration with these libraries resulted in derating of the performance by:

- ~10% of FMAX using the 0.85V slow corner library
- ~29% of FMAX using the 0.80V slow corner library

For the project the 50mV IR drop was taken as the absolute maximum target derating so the synthesis and analysis was all completed using the 0.85V worst case library for setup times, and the standard 1.1V, fast, low temperature library used for hold-timing closure.

By the end of the SALT926 project the CCS-Timing models were fully supported for the static timing analysis and scheduled to be supported for the front-end placement-aware synthesis from mid 2007 – which will allow customer designs to work with standard library deliverables and not require extra reduced voltage headroom characterization “specials”.

**Library IP support for State Retention**

State retention register designs typically add a High-Vt low leakage latch structure that has a retention power supply to a conventional low-Vt high performance Master-Slave register that can be power-gated off. A well publicised version is known as the “Balloon-flop”\(^1\) which has a pair of extra control signals:

- A SAVE signal to transfer state to the retention latch
- A RESTORE signal to copy state back into the register when re-powered up

The signals need careful sequencing and have to be driven by non-power-gated control buffer networks to ensure no state corruption.

For the SALT926 project two new styles of retention register were investigated and implemented: a single-pin-control retention register, invented by a colleague in the ARM Austin design centre, and a more radical alternative co-invented in Cambridge which simply reused the existing scan-enable and reset pins.

**Fig 5.5A** shows the layout of the retention register used for the final tape-out:

- An edge-sensitive NRETAIN control pin captures state on falling edge before power gating and restores state on the rising-edge.

**Fig 5.5B** shows the layout of the “StateSaver” retention register design:

- An asynchronous pulse on SCAN-ENABLE copies register state to the retention latch
- The NRESET control doubles as the retention restore when SCAN-ENABLE is low and a true reset when SCAN-ENABLE is high

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Figure 5.6- TSMC90G Dynamic Well Bias Delay Simulations
The single-pin control design was most easily supported by the EDA tools flow. The StateSaver version has the potential to be retrofitted to legacy IP and mixed with standard reset-able/scan-able registers with the only constraint that the Scan-Enable buffer network should be non power-gated and therefore ideally implemented in low-leakage High-Vt cells. EDA support that does no break the Design-for-Test tools is still currently in the R&D groups and support is not yet productized.

In both cases there is an area over head penalty per register – 30% to 50% overhead per retention register over conventional register depending on the register variant and drive strength. The 10-track prototype cells provided transparent retention supply routing to the registers which kept the design power planning simple for the project. Production registers revert to standard track height and add extra retention supply ports that must be explicitly power routed in the design flow. The current requirements for the retention supplies are low compared to the at-speed functional register operation so do not require a major supply grid.

**Library IP support for Dynamic Well Bias**

A number of customers have expressed interest in the leakage savings possible with the addition of back-bias to the cells – but only IDMs with their own fabrication plants have been able to productize this for mass manufacture. The SPICE models and manufacturing guarantees offered on Foundry processes are complete when wells are tied off to standard supply rails but less well specified for forward or reversed biased transistor operation. And the EDA library views are well characterized for supply voltage variation but not the extra dimension of well bias for reduced leakage operation with back-bias or the more risky faster/leakier operation with forward-bias (and the potential of thermal runaway). The SALT project took on board the challenge of providing experimental control of well and bulk voltages for the CPU logic domain – for both standby and active leakage current analysis. A representative netlist design based on a ranking of gates used in the SALT926 CPU implementation were simulated at 0.1V steps for the range -0.9V to approaching +0.8V to understand the derating effect on the standard 0.9V WC library and the 0.85V and 0.8V special characterized libraries for the project:

**Fig 5.6** shows the graphical plot of aggregate timing delay across the range. This analysis then allowed the specification of two active modes of chip operation under software control:

- **SAVER mode**, running at 200MHz compared to the worst-case 300MHz operation to support running with controlled back-bias
- **TURBO mode**, running at 400MHz to support

Because no EDA timing models support dynamic changing of supply voltage and P-well/N-well bias architectural design support was put in to ensure the Wait-For-Interrupt mechanism was used to ensure clocks stopped and held idle until power supply acknowledges safe and stable well supply voltages.
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Figure 5.7A – GIDL for 65LP LVT and HVT header switch transistors

Figure 5.7B – HVT and SCC-LVT header switch area efficiency
Adding in well bias introduces a number of design flow and evaluation platform challenges. Analyzing the leakage and performance benefits is only part of the work. There are also serious issues with respect to manufacturing variation and the danger of latch-up without very careful external power supply sequencing and decoupling.

**Library IP support for Super Cut-off CMOS (SCCMOS)**

All the leakage mitigation IP developed and described in this chapter have been based on Multi-Threshold CMOS, MTCMOS, technology, where Low-Vt but leaky transistors are used on critical paths to meet timing constraints and High-Vt transistors are used on non-timing critical paths and as the series power gates in order to ensure power gating leakage power is reduced as low as possible.

The ATLAS926-65LP used three different cell library transistors with High, Standard and Low Vt characteristics (with the fine grain power gating libraries adding High-Vt switch transistors to the leakier Standard and Low Vt implementation cells) while the SALT926 project used a pair of low and high Vt cell libraries and high-Vt transistors for the power gates. Every Vt variant requires another expensive implant mask layer and processing steps in the manufacturing flow, and the variability introduced with each implant does not track the other Vt's precisely, so the overall circuit design timing and leakage variation varies in a complex way.

A number of high-volume customers are very sensitive to mask costs and are interested in the trade-offs associated with active and leakage power and extra mask steps and yield impacts. To address this some detailed work on transistor simulations of 90nm and 65nm technologies was performed in order to understand non-MT-CMOS approaches to leakage power management.

Fig 5.7A shows the Gate-Induced Drain Leakage characteristics simulated from for the TSMC 65nm LP process, the process used for the MTCMOS ATLAS65LP project:

- The gate voltage is overdriven from the 1.0V nominal logic signalling level to show the effect on drain current. On the log scale several orders of magnitude of leakage current can be obtained by driving the gate voltage into “super-cut-off” operation.
- With a gate voltage of approx 1.5V the “off” leakage for the Low Vt transistor is as good as (in fact better!) than the High-Vt transistor can ever achieve with a gate bias of about 1.2V.

This is for a P-MOS header switch in this example.

Fig 5.7B shows the area trade-off for the HVT and LVt switches. The Low-Vt switches can carry a higher current per unit area. Even scaling the HVT switches to 10x the area still only matches the on-current performance of the Low-Vt unit area switch while the off-current leakage at optimal gate bias voltage leakage is worse proportionally.

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Physical IP for Low Power Design

Providing voltage control signals that are beyond the supply rails of course add complexity and risk. The SCCMOS approach is being investigated further by focusing on a “ring-switch” topology style where any out-of-logic-range control signalling voltages can be managed and encapsulated within strips of switches applied to the periphery of blocks to be power gated such that the routing and buffering of analogue control signals can be managed locally and not add implementation/testability and verification complexity to the IP block implementation flows.
Energy efficient SOC design technology and methodology
6. Evaluation Platforms

A series of development boards were created over the lifetime of the research programme to support:

- Basic testing of the silicon functionality
- Software development environment for in-depth test program development
- Evaluation and measurement platform for dynamic and leakage power analysis (and comparison with predicted results from simulation)
- Dynamic Voltage Scaling power supply evaluation system to support the collaboration with National Semiconductors and their initial "PowerWise" AVS power control silicon samples

Later on in the program the scope grew to encompass more functions and become the basis of the "Intelligent Energy Manager" demonstration platform:

- Demonstration systems for lead customer access
- Exhibition systems for stand-alone operation – booting from compact flash and displaying on VGA-resolution monitor screen
- Customer 'loan' system for detailed energy measurement using proprietary work-loads
- Systems built and given to lead partners to allow them to demonstrate their silicon to customers independently
- Battery power experimental test systems to allow battery-life measurements for low-power active and standby energy characterisation

This chapter of the report introduces the basic architecture for the first board and the evolution and enhancement of the design to match each stage of the development of the canonical design for the SOC.

Design Goals

To use simple off-the-shelf components and low-power modules wherever possible to simplify board design and component procurement:

- SDRAM DIMM modules and sockets rather than memory components
- Conventional (0.1" pitch) sockets and DIN-64/-96 way connectors
- Independent power supply and system board components supporting detailed current measurements of power rails independently and supporting third-party power supplies
- Minimal on-board 16-bit wide Flash EPROM to support basic diagnostic monitor
- Basic RS-232 serial communications to support communication with the diagnostic monitor through a standard terminal emulator
- Basic clock oscillator support
- Multi-ICE debug agent support through a standard header connector used from the ARM development tools to debug the chip and memory system and flash the on-board memory
- Support for audio output analogue interface to allow real-time software development and testing

6-1
Energy efficient SOC design technology and methodology

Figure 6.1 – 180nm sARS2 evaluation board
Evaluation Platforms

180nm sARS2 Evaluation Board

The first board in the programme was specified by the author but designed and built by Synopsys engineers in Hillsboro, WA. The SOC technology was 180nm so 1.8V core logic and 3.3V IO and memory systems were required for the external interfaces:

- A pair of on-board linear voltage regulators, provided with removable links on the power rails to allow power measurement.

Four memory subsystems were supported:

- A pair of 8-bit wide 32Kbyte flash memories were fitted as the 16-bit bootstrap memory and diagnostic monitor
- On-board SRAM devices – a pair of 1Mbit 8-bit wide SRAMs arranged to provide 256Kbytes of 16-bit-wide static memory
- On board Synchronous SRAM (SSRAM) bank to support 32-bit wide fast static memory access in order to enable pseudo-dual-ported DMA access for audio subsystem
- SDRAM DIMM socket for 32Mbytes of 32-bit wide SDRAM bulk memory for program development

A ZIF socket was procured for the project to meet the specification for the 408-pin BGA package used for this chip, with the aim of re-using this for subsequent SOC iterations. This was essential as no wafer or package level test was possible (cost reasons primarily) and silicon had to be tested in functional usage.

There is a large footprint area reserved for this on the circuit board but the sprung-loaded contacts can be released by unscrewing the socket and a known-good chip can then be surface-mount soldered onto the same footprint.

The only board-level peripherals were:

- RS232 level converter and 9-pin D-connector
- 8 LEDs connected to GPIO lines
- 8 Switches connecter to GPIO lines
- Simple stereo D-A filtering for audio connection on 3.5mm jack socket

All other signals were made available at header connectors shown in the lower half of the board, laid out to support logic analyser connection and external interfacing to memory mapped expansion regions.

Acknowledgement to Larry Rogers at Synopsys for schematic capture and board layout for the sARS2 board.

Only 3 boards were built for this first collaborative project.

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1 In the figure opposite these are in fact the two surface mount sockets. Due to a timing problem in the JTAG interface on this design the external Multi-ICE debug agent connection to the debugger was unusable so rather then using the ARM CPU core to program the flash memories under control of the debugger the memory devices were in fact programmed in an external EPROM programmer and the fitted in sockets on the board rather than being soldered down directly.
Energy efficient SOC design technology and methodology

Figure 6.2 – Intelligent Energy Controller FPGA prototype platform
**Evaluation Platforms**

**Software development board for “IEC”**

Due to the long fabrication and packaging schedule for the first Dynamic Voltage Scaling silicon (the 130nm DVS926 chips) an alternative hardware platform was devised for the software engineering team which emulated the DVFS environment in order to support the development of the device drivers and control stack ahead of the actual chips.

The requirements included:

- Support for Linux OS with "reasonable" performance
- Register-compatible interface to the performance control and monitoring functions of the prototype “Intelligent Energy Controller” in the first silicon.
- Emulate the behaviour of DVFS in terms of clock and voltage settling times and to emulate reduced performance levels reasonably accurately

The only FPGA platform that could be sourced to support 200MHz operation (from cache and external DDR memory) was a development board that ARM had built around the Altera Excalibur device which has a pre-hardened ARM922T CPU with 8Kbyte caches and memory controllers built within a "stripe" alongside the programmable logic.

It was not possible to reprogram the PLL clock to the CPU dynamically so a pulse-width-modulated scheme was developed that controlled the Run and Stop duty cycle of the CPU to emulate performance levels below 100%.

The synthesizable performance controller and monitors from the SOC design were re-synthesized using FPGA tools and apart from minor adjustments for the overall memory map to work with the Altera part a full emulation of the programming environment was built.

The configuration for the PLD was put into flash memory such that the device auto-configured on power-on-reset

The board itself is only part of the software development platform. This Excalibur "Logic Module" in fact has stacking connectors to allow it to be plugged in as a daughter card into an application development backplane that supports video card, Ethernet interface and the other Linux peripherals expected in the OS development environment.

Only two systems were built and commissioned.

They were successfully used to develop the driver interfaces, to port the Intelligent Energy Manager control stack and policies, and even allow some real-time profiling. (The FPGA proved ideal for such purposes allowing selected real-time signals to be routed out to a logic-analyzer connector for measurement and tuning).
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Figure 6.3 – 130nm DVS926 Voltage Scaling Test platform
Evaluation Platforms

**130nm DVS926 Voltage Scaling Test Platform**

The next board in the programme was designed entirely in-house by the author to re-use components used for commercial ARM development systems, and the circuit board was laid out by a local contractor to meet complex power plane requirements.

The SOC technology was 130nm so multiple (well at least separable in the first instance) 1.2V core logic supplies and 3.3V IO pad ring supplies were required. Before any fancy voltage scaling experiments could be started the primary requirement was to logically test the SOC devices; no wafer test was possible for cost reasons to raw untested die had been packaged.

The decision was made to separate the supplies to the pad-ring and the memories in order to measure the proportion of power consumed in the interfaces and the memories themselves.

- The power regulation was moved off the main board through a 64-way connector (lower connector of Fig 6.3) to allow both bench and standalone power supplies to be used and developed independently and by carefully splitting all the power planes and supplies on the main board support independent measurement of current and power explicitly. A fixed 1.2V functional test supply is show to the bottom of the figure.

Two on-board memory subsystems were supported:
- A single 16-bit wide 64Mbit SMT Flash EPROM to support 8 Mbytes of diagnostic monitor and application programs or operating system boot-strap. Programming is via the JTAG controlled debug agent (simulated in more detail on this chip after the problems with the sARS2 chip debug port)
- Standard PC-style SDRAM DIMM socket for 64/128Mbytes of 32-bit wide SDRAM bulk memory for program development (64Mbytes per side so support double-sided DIMM modules)

The footprint for the same ZIF socket was reused from the previous project – the same 408-pin BGA package was used for this chip but with different pin-out due to the multiple power rails and interfaces.

There is a large footprint area reserved for this on the circuit board but the sprung-loaded contacts leave the board undamaged when the socket is removed, allowing known-good tested parts to be soldered to the same board subsequently.

The only board-level peripherals were dual channel RS232 level converter and 9-pin D-connectors. One 96-way connector provided access to 48 General Purpose IO signals, audio and Synchronous Serial IO ports, and allowed external switches and LEDs to be connected for diagnostic purposes (connector on the right hand edge of Fig 6.3).

A second 96-way connector provided access to the full static memory address, control and data buses to support logic analysis and memory expansion (top edge of Fig 6.3).

Only 3 boards were built and used to functionally test DVS926 silicon and develop the diagnostic monitor code in order to characterize the DVFS behaviour.
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Figure 6.4 - 130nm DVS926 Voltage Scaling Demo platform
Evaluation Platforms

130nm DVS926 Voltage Scaling Demonstration Platform

After the successful testing of both DVS926 silicon and the evaluation board, a follow on evaluation board was developed to support internal and external software developers and to provide a number of demonstration systems to be shown to customers across the regional offices and even loaned out to customers for internal power and energy benchmarking.

The schematics were re-used from the previous board design and then a number of enhancements added:

- A “daughter” card power supply system was developed. This provided individual regulated rails to all the SOC core and IO voltage rails, together with link-selectable current monitoring facilities for each rail to support detail power measurement and analysis.
- Linear regulators were used (shown at the bottom of Fig 6.4) to ease design and construction rather than switch-mode supplies that would have exhibited better power efficiency; noise-free measurements after the regulators were the benefit with wide current load regulation for testing running and halted.
- A rudimentary dynamic voltage scaling system built into this PSU board to support open-loop table driven voltage scaling of CPU and Memory which was used for basic DVS control at different frequencies.
- Two sets of 5 LEDs were provided to indicate dynamic performance request and the values of the National AVS slack detector built into the CPU scaled voltage domain.
- Switches were added to control the “ready” level acknowledge to the Intelligent Energy Controller on board to simulate different power supply ready behaviour.
- National Semiconductor in parallel developed a switch-mode Adaptive Voltage Scaling power supply daughter board with their first PowerWise interface IC (LP5550).

The Main board was also enhanced to add a pair of memory-mapped CompactFlash slots (top of Fig 6.4). This required a pair of PLD’s to be developed that provided both hot-powered insertion protection and the fairly complex memory card timing sequencing and control for 8- and 16-bit cards. This proved very valuable and allowed Ethernet, VGA and Flash memory card drivers to be developed that provided a set of standalone demonstration modes to showcase the DVS926 silicon running MPEG-4 decoding in software with DVFS.

A batch of 20 boards was built using known tested devices verified on the previous test board with ZIF socket and the BGA devices were soldered down directly. 5 had manufacturing short circuits or problems, the remaining 15 were commissioned and used globally by sales staff with customers and at trade shows.
Figure 6.5 – DVFS Voltage Scaling Exhibition Board
"IEM" Voltage Scaling Exhibition Platform

For the first ARM Developers' Conference in Santa Clara, CA, a smaller footprint demonstration vehicle for the IEM software and hardware was developed. The basic circuitry and schematics were reused and re-partitioned across a set of small circuit boards designed to be stacked and allow modular use with and without the CompactFlash subsystem. And the opportunity to allow larger Flash EPROM images was added to support more comprehensive Linux bootstrap systems and file-system images.

A footprint the size of a Business card was chosen as the basic building block and the following set of cards were developed:

- System SOC board with DVS926, 8Mbyte Flash EPROM, crystal clock and Multi-ICE debug connector on the top side, and a laptop SODIMM memory socket on the underside of the board. DVS926 test-chips were pre-tested using the ZIF-socket-ed functional test board so could be soldered onto a small circuit-board foot-print without the need for the large socket keep-out area. With minimal trace lengths for the resultant system many of the series termination impedance matching resistors were cost-reduced from the original larger board layouts.
- Miniature stacking connectors at either end of this and all modules to route power and ground supplies, dynamic voltage scaling control, and expansion static memory interface, UART and GPIO signals.
- A dual-slot CompactFlash stacking card with PLDs and card sockets on top and bottom sides of this board
- An add-on 32Mbyte Flash Memory board that by means of a pull-down signal on the card disables and overlays the 8-Mbyte Flash EPROM on the CPU board.
- A development "mother-board" that provides plug-compatible 64-way power supply connector to National Semiconductor or ARM dynamic voltage scaling boards, plus the dual RS-232 connectors, power-on-reset circuitry and push-button plus a 96-way interface connector compatible with the GPIO/Sound/SSI connector on the previous DVS926 boards.
- Finally, an optional battery powered base-board to be used in place of the motherboard described above that allows 3 NiMH 1.2V cells to power the entire stack of boards and provide dual RS-232 and 3 20-way headers for simple expansion interfacing and logic analysis. This provided fixed 1.2V core voltage supply rather than full dynamic voltage scaling.

A CPU + CompactFlash + Motherboard are shown stacked together at the lower centre of Fig 6.5 (with a VGA interface card plugged in for MPEG playback demonstrations) surrounded by, in clockwise order, the alternative battery-powered baseboard, the system/CPU card, the dual CompactFlash card, the development motherboard and the optional Flash EPROM expansion module.

10 exhibition systems were built and commissioned for world-wide exhibition and trade-show use.
Figure 6.6 – 130nm ULTRA926 Voltage Scaling Demo platform
130nm ULTRA926 Voltage Scaling Demonstration Platform

The ULTRA926 chips were designed with the same BGA package and pin-out as the DVS926. Fig 6.6 shows a DVS926 Demonstration board reused with ZIF socket used to screen and test the ULTRA926 devices.

The testing turned out not to be straightforward due to a problem with the new PLLs that were used for the project:

- The silicon failed to phase-lock to the 12MHz crystal source.
- External PLL visibility could only be observed indirectly via SDRAM clocks and power supply interface signalling
- By plugging in a known-good DVS926 chip it was eventually possible to program up the Flash EPROM with a derivative of the diagnostic monitor built for the ULTRA926 SOC.
- Eventually it was possible to prove that ULTRA926 devices were in fact functional despite the SDRAM clocks being unstable by being able to capture RS-232 characters at one eighth of the programmed 9600-baud (1200-baud) – despite the PLL instability (the baud rate dividers filtered out much of the PLL instability)

Armed with this information a post-mortem with the PLL designers in San Diego pinpointed an error in the Verilog model for the PLL that resulted in a divide-by-8 function on the reference clock input rather than the divide-by-1 in the model used for simulation and signed off of the chip.

- After experimenting with how to overdrive the crystal input pad circuitry using a bench-top waveform generator set at exactly 8 times the 12MHz reference clock frequency and carefully adjusting the amplitude and DC offset, the ULTRA926 silicon then behaved functionally correctly from SDRAM

- A simple modification to the clock circuitry was devised for the ULTRA926 build of the board that used a custom-made 3.3V CMOS 96MHz oscillator and a passive signal conditioning network to overdrive the CMOS crystal pad input

After overcoming the clock generation problems the ULTRA926 DVFS demonstration board became a useful evaluation platform. The four dynamic CPU performance levels between 50% and 100% of the 288MHz design target operating frequency exhibited better energy savings compared to the original DVS926 design and the system operated up to 360MHz on the bench at room temperature with the close-to-typical silicon fabricated devices.

A batch of 8 limited production cards were built with surface-mounted pre-tested ULTRA926 devices, hand modified with a yield sufficient to successfully show at the Design Automation Conference and ARM Developer Conferences in 2006, and with some boards then supplied to UMC for their own use.
Energy efficient SOC design technology and methodology

Figure 6.7 – 65nm ATLAS926 Voltage Scaling Demo platform
Evaluation Platforms

65nm ATLAS926 DVS/Leakage Demonstration Platform

The ATLAS926 chips were again designed to use the same BGA package and pin-out as the DVS926. Fig 6.7 shows a DVS926 Demonstration board reused with surface-mounted ATLAS926 silicon.

The system again required some basic modifications to support the specific voltage requirements introduced as the result of 65LP technology:

- The Generic IO pads were specified at 2.5V rather than the 3.3V used for previous boards and required for the standard SDRAM and Flash memory components interfaced direct to the chip
- The analogue power supply to the on-board 1GHz PLLs in particular needed a 2.5V +/-10% clean supply rail.
- After negotiation with TSMC it was agreed to run the pad-ring at around 2.8V, not high enough to stress the IO devices for evaluation usage, and high-enough to give clean clocking and signalling at the interfaces of the Flash and SDRAM. (Flash EPROM requires a minimum of 3V3 – 10% for safe programming, the SDRAM similarly is unsafe below 3.0 volts and the clock rise-time specifications require careful attention.
- After negotiation with TSMC it was agreed to run the pad-ring at around 2.8V, not high enough to stress the IO devices for evaluation usage, and high-enough to give clean clocking and signalling at the interfaces of the Flash and SDRAM. (Flash EPROM requires a minimum of 3V3 – 10% for safe programming, the SDRAM similarly is unsafe below 3.0 volts and the clock rise-time specifications require careful attention.
- A set of modifications to the Power Supply daughter boards were devised to run the SDRAM and Flash supply rails at around 3.10V (minor adjustment to the regulator reference resistor dividers), the SOC IO ring at 2.8V and the filtered PLL supply voltage exhibited clean start-up behaviour.
- The 5 “Slack value” LEDs from the DVS926 and ULTRA926 adaptive voltage scaling interface were re-used on the ARM PSU board to provide visual indication of:
  - 2-bit Leakage mode (Halt/SRPG/Scan-Hibernate/Shutdown)
  - 2-bit Performance level (Turbo/Normal/Long-Life)
  - Wake up event (enabled interrupt following Wait-For-Interrupt)

An ATLAS926-specific version of the diagnostic monitor with the appropriate IEC performance control values and support the new leakage management states.

MPEG-4 video decode demonstration software was successfully ported by the author to the ATLAS board but due to subtle change to the Synopsys DesignWare UART functionality in the release of the IP used for this project the Linux serial drivers fail with some form of interrupt that cannot be cleared so only the basic Linux kernel is ported to this system.

A batch of 8 “production” cards were built with surface-mounted pre-tested ATLAS926 devices and the system was successfully shown at the Design Automation Conference and ARM Developer Conferences in 2006 with some boards then supplied to TSMC for their own use.
Figure 6.8 – Diagnostic and Analysis boards

Figure 6.8A – Power Measurement "break-out" analysis board

Figure 6.8B – Diagnostic LED and Switch module
Evaluation Platforms

**Diagnostic and Analysis Boards**

The "canonical" board design with a common package footprint has proved a valuable and cost-effective approach for the EngD research programme.

Using somewhat old-fashioned 0.1" pitch industrial quality connectors for all the boards apart from the miniaturised exhibition system it has been possible to construct simple interface plug-in boards for power analysis and diagnostics purposes to aid basic software development – using standard prototyping "grid-board" rather than having to resort to further printed circuit board development and manufacture.

*Fig 6.8A* shows the simple power rail intercept board that was used to monitor current and voltage with the range of National, ARM and bench power supplies used for voltage scaling characterization.

The lower edge of *Fig 6.8B* shows a basic diagnostic board that interfaces 8 LEDs and 8 Switches to generic GPIO lines that is used for basic bootstrap code development and supports power-on-self-test diagnostics that set appropriate patterns on the LEDs to indicate good/bad status when working though the memory and peripheral checks from power up. This board proved invaluable for the basic manufacturing test of new boards.

The left hand side of *Fig 6.8B* also shows a specially modified power supply module connected to the system board. In this case the CPU/Cache-RAM supply regulator has been bypassed and a 1.2V NiCd or NiMH rechargeable cell is connected in place through a switch controlled by a low voltage relay. The relay mounted up below this provides zero-ohm switching between the battery source and the core supply 1.2V fixed voltage linear regulator. This circuitry was designed to enable concrete energy consumption measurements. After fully charging the rechargeable cell the true integration of current and voltage over time can be measured for repeating MPEG4 movie playback using different DVFS algorithms for dynamic energy savings and different leakage modes for Wait-for-Interrupt periods at the end of the data dependent frame decoding and rendering.

This method provides much more accurate energy consumption measurements compared to accumulating the product of measuring average current and measured average voltage given the high-speed burst-nature of current consumption for a cached CPU core.
Energy efficient SOC design technology and methodology

Figure 6.9A – 90nm SALT926 packaged silicon and new ZIF socket

Figure 6.9B – 90nm SALT926 Test Board prototype
Evaluation Platforms

90nm SALT926 Test Board

At the time of writing up this thesis the SALT926 silicon has just arrived back from packaging and the first of the new test boards built up.

This silicon is packaged in a 388-pin BGA package unlike all the earlier test chips, and incorporate a 480MHz USB OTG PHY interface that requires special PCB layout so the board for this project is being designed by Synopsys using the Author’s SDRAM, Flash and Serial RS-232 circuitry.

As can be seen from the socket in Fig 6.9A this is a larger footprint package and has a centre cluster of 16 (grounded) balls that can be removed form the package for experimental purposes. Because leakage power is exponentially related to die temperature the balls that are under the centre of the die act as a thermal heat-sink for the plastic package and substrate, by removing these balls the effect of higher die temperature will be valuable to analyse once the board is ready. (The socket acts as a form of heat-sink so the experiment may only be conclusive with directly surface mounted packages with and without the 16-ball thermal sink)

Fig 6.9B shows the prototype SALT90G board

- SDRAM interface and DIMM socket to the top side of the circuit board
- RS-232 sockets, reset switches and PLL configuration to the right hand side
- In the lower right area are GPIO and diagnostic connector links. The chip has a 16-bit GPIO interface and a multi-purpose 16-bit bidirectional diagnostic channel that can be configured for 8 different modes of operation from manufacturing scan test to leakage state machine visibility for real-time measurements of on-chip power gating entry and exit times and tracking soft errors in State-Retention entry and exit
- USB OTG mini 5-pin connector to the lower edge of the board
- A small on-board switched-mode power supply is implemented lower left to generate the 1V core supply rails and 1.8V analogue PLL supply in addition to the 3.3V IO and memory supplies
- The left hand side circuitry shares the 16-bit static memory interface between an 8Mbyte on-board Flash memory and an experimental 128x128 OLED panel display which has a parallel data and command interface to an integrated frame-store. This has been chosen as an alternative to the CompactFlash approach to external VGA display cards (after all manufacturing for these appears to have been discontinued)
- To the immediate left of the SOC socket is the Multi-ICE debug agent connector provided as the primary diagnostic and programming interface

Five boards are being manufactured initially and the first 20 die have been packaged. Only limited screening of the packaged devices has been possible to isolate some devices without wire-bond short circuits.
Energy efficient SOC design technology and methodology
7. Technology Demonstrator Evaluation and Analysis

SARS2 180nm SOC Evaluation

The first SOC design was used to "pipe-clean" the standard design flow, and should have been a straightforward integration exercise. However to simulate full customer design flows with pre-verified foundry CPU core (ARM946 with dual 8K-byte caches in this case) the processor was treated as "black-box" design with the following design views:

- Timing Model - a pin-level (Liberty) timing library view (worst and best case timing for sign-off of setup and hold times)
- Design Simulation Model (an encrypted cycle accurate model with Venlog timing "shell" to support back annotation of delays from the final SOC layout)
- Physical Model representing footprint, signal and power ports and "keep-out" regions over the memory

All the above views were insufficient in certain ways and a detailed report was written to feedback to the ARM CPU hardening team to address deficiencies and issues.

The silicon was packaged untested and had to be debugged on the evaluation board designed for it. None of the packaged devices would communicate with the Multi-ICE Debug Agent and yet there were signs of life on the PLL and externally visible SDRAM clock. This was a major problem given that the Flash EPROM devices soldered onto the board were blank and were only programmable through the Multi-ICE debugger JTAG interface.

Two approaches were taken to understand the problems:

- The software diagnostic monitor that had been prepared and simulated was blown into Flash EPROM devices using a bench programmer, the surface mount EPROMs were desoldered from the board and surface mount sockets procured and eventually soldered to the evaluation board. The UART based diagnostic monitor was successfully ported.
- The JTAG interface timing was analyzed with a storage oscilloscope and eventually a race hazard on the clock synchronization was uncovered. No workaround was possible.

The latter was traced directly to clock latency modeling problem with the abstracted timing view and SDF back-annotation where a negative setup time violation was "rounded" to zero.

SARS2 Lessons Learned

Very painful learning experience on what should have been a straightforward SOC design. The JTAG validation test-bench coverage was increased to check signatures in detail before the next project was verified. And design review guidelines developed to address timing sign-off criteria were developed.
Energy efficient SOC design technology and methodology

Figure 7.1A – RSD926 DVFS Evaluation (Chip#1, 22°C) – V limit

Figure 7.1B – RSD926 DVFS Evaluation (Chip#1, 22°C) – Current (mA)

Figure 7.1C – RSD926 DVFS Evaluation (Chip#1, 22°C) – Power (mW)
DVS926 Silicon Evaluation

Silicon Verification

Compared to the first SOC design the DVS926 silicon carried a lot more risk but after the clock skew hazards unearthed in the first project there had been much greater review scrutiny in the timing sign-off for this DVFS design.

Again no wafer test was available for cost reasons so the untested packaged devices had to be screened in an untested board, with untested diagnostic firmware and unknown bonding quality.

Good signs off life were detected from five devices tested, and the Multi-ICE debug agent established JTAG connection successfully with the ARM926 CPU on four of these devices. The SOC, CPU and RAM supplies were all set to a fixed, shared 1.2V supply for functional testing:

- Memory-mapped control registers could be successfully read and written
- SDRAM clocks were eventually balanced and timing configured to support download and upload of data – after a number of scares with byte mask hold times causing some byte write corruption
- The Flash Programming application was then developed and down-loaded to SDRAM to support programming of basic diagnostic bootstrap loader
- Finally the terminal-based monitor application was developed and tested and programmed into Flash memory to support stand-alone operation

DVFS analysis

In order to test and measure the power and energy savings with Voltage Scaling, and to verify the level shifter IP and complex clock pre-compensation scheme functioned correctly across some degree of CPU/RAM reduced supply range.

The Diagnostic monitor was augmented to add:

- Performance control programming of the IEC prototype interface to support 100%, 75%, 50% and 25% levels, and a 0% halt mode using wait-for-interrupt for leakage power measurements
- A stand-alone Dhrystone-based cache-intensive workload to exercise the CPU and cache memories intensively and repetitively in order to allow average current and power measurements to be made accurately, and thermal stability to be exercised
- A UART-based protocol to support communication with a LabView configuration to allow test-bench automation of run/test with success or fail/time-out reporting to allow an IEE488 (HPIB) power supply to be used to sweep voltage and measure current

The measured limits of voltage headroom (Fig7.1A), current (Fig7.1B), and power (Fig7.1C) are shown graphically. The slight “hook” in the voltage headroom curve was unexpected but clean monotonic operation in the range 1.32 to 0.8V was encouraging for typical silicon.

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Energy efficient SOC design technology and methodology

Figure 7.2A - RSD926 DVFS Evaluation (Chip#1, 22°C) - Energy Consumption

**DVS926 - Normalized Energy Measurements**
(Power x Duration to complete - for cached workload)

- Energy: fixed 1.2V DFS
- Energy: Open Loop DVS
- Energy: AVS limit +5% (25°C)
- Energy: AVS limit (25°C)

Figure 7.2B - RSD926 DVFS Evaluation (Chip#1, 22°C) - Energy Savings

**Measured Voltage/Power/Energy Analysis**

- Voltage Headroom at 1.2V
- Operational Voltage (DVFS)
- Wasted Power at 1.2V
- Operational Power (DVFS)
- Wasted Energy at 1.2V
- Operational Energy (DVFS)
Energy Measurement

In order to relate the power measurements to energy consumption – the real metric for the IEM product development – the same Dhrystone workload was run a fixed number of iterations at each of the performance levels. The cache intensive nature of the workload in fact resulted in close to inverse linear scaling; running at half the performance duly resulted in having to run the workload twice as long.

Fig 7.2A shows the measured power x duration values for energy consumption:

- In the case of no voltage scaling the energy consumption at lower performance levels was roughly the same (as expected when running at half the power for twice as long)
- The lowest curve is shown for the limit of operation – at room temperature with the near-typical silicon.
- The next curve above this – the “AVS” curve was plotted with the extra (5% or so) voltage headroom with the on-chip process and temperature slack detector control loop functionality
- The curve above this is a reference with +10% voltage headroom for table-driven open-loop or non adaptive dynamic voltage scaling

Energy savings of 50% for the cached CPU were measurable even with open loop voltage margins – and the energy saving for the 25% performance level was negligible compared to the 50% performance point – only the 100%/75%/50% performance levels were useful to IEM control software.

Fig 7.2B shows the results displayed graphically as bar charts in the form that became the basis of an EE-Times article written by the author for publication in January 2004.

DVS926 Lessons Learned

The lack of good low voltage characterization has been a concern going into the project. From the analysis it is apparent that there was no value in providing the 25% performance level – there was insufficient voltage headroom to provide any power saving below the 50% performance level. Knowing this beforehand would have resulted in a different dynamic clock generator design.

The analogue level shifters and isolation clamps had not been simulated at transistor level; there was indeed a problem when the CPU was stopped and held in Wait-For-Interrupt mode which resulted in leakage power measurements much higher than expected from the standard-cell models and this was traced to floating-nodes in the level shifters that caused currents to flow.

The silicon was fully functional for DVFS operation and once the Linux port was completed the evaluation platform was made available to the Intelligent Energy Manager software team and eventually to end customers to allow commercially sensitive workload profiles to be run and measured with realistic multi-tasking application software.

Although only typical silicon resulted from the project the ability to increase the PLL master frequency in 5% steps up to +25% was found to be useful to emulate the effect of running closer to the limit - as if slower silicon. This also allowed the increased resolution in voltage/frequency points for Fig7.1A-C.

1 http://www.eetimes.com/in_focus/mixed_signals/OEG20040122S0028
Energy efficient SOC design technology and methodology

Figure 7.3A - ULTRA926 DVFS Evaluation (Chip#2, 22°C) - Current (mA)

Figure 7.3B - ULTRA926 DVFS Evaluation (Chip#2, 22°C) - Power (mW)

Figure 7.3C - ULTRA926 DVFS Evaluation (Chip#2) - Dhrystone/second

<table>
<thead>
<tr>
<th>Freq (MHz)</th>
<th>KDhry/second</th>
</tr>
</thead>
<tbody>
<tr>
<td>144</td>
<td>217.00</td>
</tr>
<tr>
<td>192</td>
<td>288.32</td>
</tr>
<tr>
<td>240</td>
<td>360.58</td>
</tr>
<tr>
<td>288</td>
<td>432.91</td>
</tr>
</tbody>
</table>

Figure 7.3D - ULTRA926 DVFS Evaluation (Chip#2) - Work Duration

<table>
<thead>
<tr>
<th>Freq (MHz)</th>
<th>1MDhry (milliseconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>144</td>
<td>4608.30</td>
</tr>
<tr>
<td>192</td>
<td>3468.31</td>
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<tr>
<td>240</td>
<td>2773.30</td>
</tr>
<tr>
<td>288</td>
<td>2309.97</td>
</tr>
</tbody>
</table>
ULTRA926 Silicon Evaluation

Silicon Verification

Compared to the DVS926 silicon the ULTRA926 project had the benefit of a full set of detailed transistor-level simulations of the cached CPU core that had been used to design the dynamic clock generator. Therefore measuring actual power and energy usage compared to predictions was a large part of this project.

However the evaluation work on this chip ran into two unforeseen problems:

- All the first 8 devices screened suffered from what appeared to be power supply short circuits across the VDDRAM supply network to VSS. On more careful inspection this was found to be a few ohms and by using a high current limit on the supply some life could be detected on the SOC. Checking more devices in Taiwan led to the discovery that a few parts showed higher impedance on the RAM supply, and on re-screening 50 packaged devices 4 were found to be usable.

- The PLLs were found to suffer from a problem where they would not lock to frequency and a swept-frequency signal was found on what should have been the steady SDRAM clock drivers. The root cause of this and the workaround in the form or an external 96MHz oscillator are described in Chapter 6 for the ULTRA926 evaluation system, suffice to say that a couple of functional parts were eventually running cache diagnostics and ready for analysis.

After updating the memory configuration programming the diagnostic monitor was largely reused from the DVS926 project but with a couple of enhancements:

- Performance control programming of the IEC prototype interface updated to support 100%, 83%, 67% and 50% levels – for the new faster 288MHz worst-case design.
- 0% halt mode using wait-for-interrupt for leakage power measurements (without the floating nodes leakage power problems of previous chip)

The measured current I/V and power P/V curves are shown at Fig 7.3A and Fig 7.3B respectively, and show good monotonicity. The measurements are at the power supply connections to the board power connector so the actual silicon has IR-drop for circuit board, socket, BGA socket bonding and on-chip power rails are all additional to this – while the transistor simulations do not take any of these into account. So maintaining operation down to 0.72V with typical silicon at room temperature was encouraging.

Fig 7.3C and Fig 7.3D show the detailed measurements of cache-intensive Dhrystone application work load and how this translates into work-load duration for the energy consumption analysis.
Energy efficient SOC design technology and methodology

Figure 7.4A – ULTRA926 DVFS Evaluation (Chip#2, 22°C) – Energy

<table>
<thead>
<tr>
<th>V</th>
<th>E(288MHz) (mJ)</th>
<th>E(240MHz) (mJ)</th>
<th>E(192MHz) (mJ)</th>
<th>E(144MHz) (mJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.72</td>
<td>(unsafe)</td>
<td>(unsafe)</td>
<td>(unsafe)</td>
<td>37.44</td>
</tr>
<tr>
<td>0.78</td>
<td>(unsafe)</td>
<td>(unsafe)</td>
<td>42.12</td>
<td>43.68</td>
</tr>
<tr>
<td>0.84</td>
<td>(unsafe)</td>
<td>48.38</td>
<td>49.14</td>
<td>50.40</td>
</tr>
<tr>
<td>0.90</td>
<td>(unsafe)</td>
<td>56.16</td>
<td>56.70</td>
<td>57.60</td>
</tr>
<tr>
<td>0.96</td>
<td>63.36</td>
<td>63.36</td>
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</tr>
<tr>
<td>1.02</td>
<td>71.40</td>
<td>72.22</td>
<td>73.44</td>
<td>73.44</td>
</tr>
<tr>
<td>1.08</td>
<td>81.00</td>
<td>81.65</td>
<td>82.62</td>
<td>84.24</td>
</tr>
<tr>
<td>1.14</td>
<td>91.20</td>
<td>91.66</td>
<td>92.34</td>
<td>93.48</td>
</tr>
<tr>
<td>1.20</td>
<td>100.80</td>
<td>102.24</td>
<td>104.40</td>
<td>105.60</td>
</tr>
<tr>
<td>1.26</td>
<td>112.14</td>
<td>113.40</td>
<td>115.29</td>
<td>115.92</td>
</tr>
<tr>
<td>1.32</td>
<td>124.08</td>
<td>126.72</td>
<td>126.72</td>
<td>129.36</td>
</tr>
</tbody>
</table>

Figure 7.4B – ULTRA926 DVFS Evaluation (Chip#2, 22°C) – Energy

Figure 7.4C – ULTRA926 DVFS Evaluation Overclocked – Energy

<table>
<thead>
<tr>
<th>CPU MHz</th>
<th>Vmin (limit)</th>
<th>I (mA)</th>
<th>KDhry/sec</th>
<th>Energy (mJ)</th>
<th>Energy consumed</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>0.777</td>
<td>33</td>
<td>271.003</td>
<td>95</td>
<td>58%</td>
</tr>
<tr>
<td>240</td>
<td>0.842</td>
<td>47</td>
<td>363.636</td>
<td>109</td>
<td>67%</td>
</tr>
<tr>
<td>300</td>
<td>0.932</td>
<td>65</td>
<td>454.546</td>
<td>133</td>
<td>82%</td>
</tr>
<tr>
<td>360</td>
<td>1.030</td>
<td>86</td>
<td>542.005</td>
<td>163</td>
<td>100%</td>
</tr>
</tbody>
</table>
ULTRA926 DVFS Energy Savings

Energy Consumption Analysis

Fig 7.4A shows the tabulated power x duration measurement data displayed at the four performance levels designed into the ULTRA926 SOC. These were gathered across 5% steps of VDDCPU supply from 60% to 110% of the nominal (1.2V) supply rail. A blank in the column entry indicates the processor is outside safe operating range.

The frequencies chosen for the ULTRA926 project are in fact all multiples of a master 48MHz bus clock at the default PLL multiplier configuration setting:

- 6x (100%) for worst case 288MHz “FMax” sign-off
- 5x (83.3%) for 240 MHz
- 4x (66.7%) for 192MHz
- 3x (50%) for 144MHz

The energy measurements all correlate very cleanly — taking a row for a certain operating voltage the energy consumption is shown similar at each of the frequencies with some positive increase approaching 5% in the 144MHz case.

Fig 7.4B shows the energy consumption plotted in histogram form to visually display the close-to-linear energy efficiency relationship measured for the device.

Even with 10% voltage margins added back for safety there is still of the order of 50% energy savings possible on workloads that can be run for twice as long at half the frequency (50.4 milli-Joules for 144MHz at 0.84V compared to 100.8 milli-Joules for 288MHz at 1.2V).

The ULTRA926 CPU subsystem was implemented on UMC 130HS process technology which is faster but leakier than the 130LL Low Leakage technology used to implement the rest of the SOC. The leakage power becomes apparent in the energy “losses” for the 83%, 66% and 50% performance levels compared to 100%. For leakier process technology nodes this is a reminder of the balance that must be evaluated between runner slower in order to reduce voltage and power as much as possible but at the expense of burning leakage power for longer.

The “shuttle” silicon for this project was confirmed as close to typical process by UMC. To explore the case of slower silicon in order to observe and understand the energy savings possible the master PLL frequency configuration was changed to raise FMax to 360MHz.

The measured minimum voltages for the four supported fractional performance levels are tabulated in Fig 7.4C together with the energy consumption savings possible while emulating “moving the silicon” closer to the edge as if slower.
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Figure 7.5A – ULTRA926 160x120 MPEG4 Decode Workload

Figure 7.5B – ULTRA926 DVFS analysis test bench
MPEG-4 QQVGA Movie Playback Workload Analysis

In order to build a repeatable dynamic workload environment a 25-frame-per second 160x120 (quarter-quarter-VGA) movie with software-only MPEG-4 decoder application were developed and programmed into the on-board Flash EPROM. The small display is representative of mobile-phone and small PDA devices sufficient to run realistic application workloads.

The display hardware was in the form of a memory-mapped CompactFlash VGA card that was supported by the Demonstration and Exhibition boards developed from the original DVS926 evaluation board. The CV-VGA card has an integrated frame-store buffer and only changes from a previous frame need to be updated which avoids an expensive software complete video buffer copy every frame.

Fig 7.5A shows example display output as shown on an external VGA monitor:

- The centre window shows a frame of the 20 second (500 Frame) compressed movie
- The lower window displays a rolling display of the dynamic performance control for every frame of the movie. The Yellow (lower) trace shows the fractional performance level requested by the movie player, that varies according to how complex the motion estimation is and decode complexity on the video stream, and how far ahead of the next real-time frame display interrupt the decoder is running.
- The Red (upper) trace shows the actual performance level quantized in hardware to the next highest available frequency. Although hard to see it is just possible to discern the 50% (half-height), 67%, 83% and occasional 100% levels dynamically chosen for frames in the example movie. It will be observed the video player can keep up with the simple frames of the movie much of the time at 50% or 67% of the 288MHz CPU core but on complex video sequences this grows occasionally to 83% and even 100% (around half-way along the rolling frame history window)

DVFS (and PLL) Testbench

Fig 7.5B shows the equipment test-rig used to evaluate the ULTRA926 devices.

- An Hewlett-Packard (Agilent) programmable power supply shown as the lower test rack was used to provide the voltage and current testing of the dynamic and fixed power rails.
- An HP Frequency Generator (balanced on top of the PSU) is also shown that was used to develop the workaround for the PLL reference frequency divider – which in the end required overdriving a sinusoidal 96MHz signal with managed DC-offset voltage into a 12MHz crystal oscillator circuit with internal harmonic filtering, after much experimentation.

Lessons learned

The detailed low voltage characterization at the design phase of the ULTRA926 project resulted in the highly usable DVFS performance, and the choice of four performance levels between 50% and 100% offered much better algorithmic control compared to the previous DVS926 project.

The chip proved a useful testing ground for the Artisan Analogue IP – including picking up the divergence between the simulation model and the silicon for the PLL design ahead of other customers. This chip design became the case-study for a tutorial the author was asked to present at DAC2005.
Energy efficient SOC design technology and methodology

Figure 7.6A – ATLAS926-65LP evaluation test bench

Figure 7.6B – ATLAS926-65LP Evaluation (Chip#21, 22°C) – Power (mW)

Figure 7.6C – ATLAS926-65LP Evaluation (Chip#21, 22°C) – Energy (%)
ATLAS926-65LP Silicon DVFS Evaluation

The ATLAS926 silicon suffered from a problem that the JTAG Multi-ICE connection failed – regardless of speed of connection and JTAG clock duty cycle. After some hours tracing this problem, a Verilog coding error in the edge synchronization of the on-chip debug clock was discovered – which was not picked up in the self-checking simulation test-bench. A workaround was devised that inverted the JTAG clock (TCK) to the board and inverted the return clock (RTCK) from the board such that the CPU sampled the debug data on the alternate edge of the clock. A small daughter board was built that intercepted the 20-pin Multi-ICE connector and proved to transparently fix this problem (shown mounted vertically in Fig 6.7).

Subsequently the monitor code was able to be tested, updated and the Flash programming all worked reliably.

- The monitor was enhanced to support the 100%/80%/60%/40%/20% DVFS performance levels
- A number of leakage control functions were added, described on the next page.

The DVFS design for the 65nm LP process was complicated by the fact that the standard cell logic portion of the CPU had headroom on the 1.2V nominal voltage process to support voltage scaling but the (cache) RAMs were not guaranteed to have any voltage scaling headroom. In order to support this level shifters had to be added onto every signal to be “up-shifted” from the CPU domain to the RAM domain – and RAM outputs down-shifted back to CPU. Understanding the timing impact of adding the level shifters onto the critical path cache access circuitry and validating that the timing relationships at the RAMs were not violated by voltage scaling – something that had been hard to sign-off before tape-out.

The VDDCPU and VDDRAM supplies were separately bonded out of the ATLAS design and supported interception for independent current monitoring and safe working voltage testing.

Fig 7.6A shows the DVS test-rig adapted for the ATLAS silicon.

The limits of voltage scaling were mapped and the current measurements for reliable operation were captured and used to derive the measured steady-state power graphs shown in Fig 7.6B at 20mV intervals. The graphs are basically monotonic but the current resolution of 1mA resulted in slight quantized current readings resulting in the staircase appearance of the graphs. Below 1.08V a shallower gradient is just apparent and this shows the effect of the RAM voltage not being scaled below this voltage while the standard cell logic is scaled a further 200mV.

Fig 7.6C shows the energy consumption after the workload duration scaling has been factored in and is shown normalized to the 1.08V (1.2V - 10%). Again the energy efficiency gradient is slightly shallower below this voltage due to the RAM energy cost remaining consistent below this point.
Energy efficient SOC design technology and methodology

Figure 7.7A – ATLAS926-65LP Leakage Evaluation (Chip#21, 22°C)

Halt-Mode Leakage

![Halt-Mode Leakage Graph](image)

Figure 7.7B – ATLAS926-65LP Leakage Evaluation (Chip#21, 22°C)

Power Gating

![Power Gating Graph](image)

Figure 7.7C – ATLAS926-65LP Leakage Evaluation (Chip#21, 22°C)

Leakage Mitigation Analysis (Device#01)

![Leakage Mitigation Analysis Graph](image)
ATLAS926-65LP Silicon Leakage Mitigation Evaluation

The leakage mitigation techniques for the ATLAS design were analysed in detail. The leakage control states are all entered by the processor executing a Wait-For-Interrupt instruction, completing all outstanding bus transactions and signalling that clocks may be stopped. The metrics of interest are not only how much leakage power may be saved over and above simply.

- **HALT** mode allows stopping the clock, has the fastest real-time wake-up time following an interrupt and allows the baseline static leakage to be measured. This is equivalent to high-level (architectural) clock gating. **Fig 7.7A** shows the leakage power measured at 5% voltage steps from 55% to 110% intervals for both the mixed-Vt standard cell logic and the High-Vt cache RAM partitions of the CPU. In fact because voltage scaling has real-time costs the only "instantaneous" wake up condition is at the appropriate voltage scaling that the CPU was halted and then re-awoken. However the analysis is proving useful to understand how to use header switches to power gate between reduced voltage "retention" supply and standard full-current rail.

- **LIGHT SLEEP** (SRPG) mode offers a transparent "emulation" of clock gating. After the clock is stopped the state is internally retained in a low-leakage always powered "balloon latch" and then all the leaky logic switched off using local power gates (fine-grain intra-cell footer switches in this project). The real-time wake-up cost is impacted by the times required to safely power back up the logic and restore state from the balloon to the active register latches. **Fig 7.7B** shows the leakage power measured at 5% voltage steps from 55% to 110% intervals for both the mixed-Vt standard cell logic and the High-Vt cache RAM partitions of the CPU. The leakage power is shown to be reduced from the HALT-mode clock-gating by power-gating at 1.2V by more than 8-fold, and the RAM now becomes the dominant leakage power component. Because only the Low-Vt and Standard-Vt standard cells have fine-grain power gating support the residual leakage power comes from the always-on networks to control the power-gating, the save and restore control networks and the balloon latches and the remaining High-Vt logic on non-critical timing paths.

- **DEEP SLEEP** mode is the scan-based state save and restore mode that allows the state to be stored in (slower, lower power) memory on-chip or even off-chip. This has higher real-time latency penalties than SRPG but allows the CPU logic rail to be powered off completely. The RAM power measurements from **Fig 7.7B** are the same, the power gated logic component reduces to zero. For this particular technology it can be see that as the RAM leakage power dominates savings are only of the order of 30% over SRPG, but on higher leakage technologies this will be more valuable.

**Fig 7.7C** shows the leakage power plotted on linear and log scales – and the effect of the "floor" on VDDRAM of 1.08V required to ensure retention – for Clock Gating, State-Retention Power-Gating and scan-based rail switching.

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Energy efficient SOC design technology and methodology

Figure 7.8A – ATLAS926-65LP Leakage/Temperature analysis (Chip #21)

HALT(CG) vs Temp

Leakage Power (uW)

0 200 400 600 800 1000 1200 1400 1600

0 20 40 60 80 Temp (°C)

VDD = 0.6 V
VDD = 0.7 V
VDD = 0.8 V
VDD = 0.9 V
VDD = 1.0 V
VDD = 1.1 V
VDD = 1.2 V
VDD = 1.3 V

Figure 7.8B – ATLAS926-65LP CG/PG Ratio (Chip #21)

HALT/PG vs Temp

Ratio (HalT/PG)

0 5.00 10.00 15.00 20.00 25.00 30.00 35.00

0 20 40 60 80 Temp

VDD = 0.6 V
VDD = 0.7 V
VDD = 0.8 V
VDD = 0.9 V
VDD = 1.0 V
VDD = 1.1 V
VDD = 1.2 V
VDD = 1.3 V
ATLAS926-65LP Thermal Leakage Characteristics

All the initial leakage measurements and analysis were at room temperature. The die-size is small (4x4mm) and the CPU dynamic power dissipation less than 75mW at 1.2V for the DVFS analysis work so the thermal characteristics are optimistic compared to a larger real-world SOC design with higher-power integrated subsystems. Because the leakage term is exponentially proportional to temperature a follow on set of measurements was conducted in an environmental control chamber that supported controlled temperatures between 0° and 80° Centigrade.

Understanding the temperature characteristics is also important from the perspective of the complications of effects such as “temperature-inversion” where delay characteristics become non monotonic in relation to temperature, highly dependent on the supply voltage.

Fig 7.8A shows the leakage power graphs measured at 10-degree Celsius intervals for the standard-cell portion of the CPU subsystem (i.e. without the RAM portion); the upper graph shows the measurements for clock gating using the HALT mode. The lower graph shows the measurements for state-retention power-gating using the LIGHT SLEEP leakage mitigation mode. As expected the effects of increased temperature are dramatic:

- Clock-gated (CG) leakage grows more than six-fold between room temperature and 80°C to more than 1mWatt for this “typical” silicon.
- SRPG leakage grows less strongly - roughly quadrupled over the same temperature range to a little over 40uWatt.

Fig 7.8B shows the graphing of the relative savings of SRPG over Clock Gating. This is a much more interesting metric from the perspective of understanding the relative cost functions of how much leakage power can be saved at particular operating conditions versus the energy costs to enter and exit deeper levels of leakage mitigation and their associated wake-up latencies. Again this is shown for the standard-cell portion of the processor where the power gating is applied:

- The savings grow from roughly 20-fold at room temperature to 30-fold at temperature of 60°C. The experiment was conducted over two days to allow full thermal stability to be reached by the board and the plastic package to ensure that the measurements closely tracked die temperature.
- The decrease in the effectiveness in SRPG over static leakage at elevated temperatures is related to the proportion of non-power gated High-Vt logic to power gated Low and Standard-Vt cells; the High-Vt leakage characteristics grow faster at elevated temperatures compared to the lower Vt’s so start to dominate the leakage characteristic.
- The thermal profile matches well the die-temperatures of SOC products in low-cost plastic packages and the results are valuable to understand for leakage management control algorithms.
Energy efficient SOC design technology and methodology

Figure 7.9A – ATLAS926-65LP Leakage/Temperature analysis (Chip #21)

![Graph showing leakage power versus temperature for ARM926 CPU+CACHE and RAM HALT](image)

Figure 7.9B – ATLAS926-65LP CG/PG Ratio (Chip #21)

![Graph showing relative leakage power savings versus temperature](image)
Fig 7.9A shows the leakage power graphs measured at 10-degree Celsius intervals for the complete CPU subsystem, both standard cells and the High-VT RAM portion. The upper temperature was extended up to 100°C, the lower end reduced to -10°C and the graphs are plotted on log scales to show more clearly the RAM proportion of the leakage power and how this varies with temperature.

The upper graph shows the measurements for clock gating using the HALT mode. The lower graph shows the measurements for state-retention power-gating using the LIGHT SLEEP leakage mitigation mode. As expected the effects of increased temperature are dramatic.

- Clock-gated (CG) leakage grows more than ten-fold over a +70°C temperature change for this "typical" silicon.
- SRPG leakage is dominated by the RAM leakage power - the cached CPU leakage power reaches 100uWatt at only +30°C above room temperature.

Fig 7.9B shows the graphing of the relative savings of SRPG over Clock Gating, taking into account both RAM and logic.

- The savings grow to roughly 8-fold at temperature of 40°C. Again the experiment was conducted over a couple of days to ensure thermal equilibrium for the board and the plastic package so that the measurements closely tracked die temperature.
- The decrease in the effectiveness of SRPG over static leakage at elevated temperatures is related to the proportion of non-power gated High-Vt logic to power gated Low and Standard-Vt cells, the High-Vt leakage characteristics grow faster at elevated temperatures compared to the lower Vts so start to dominate the leakage characteristic. Because the RAM leakage is significant this depresses the "peak" ratio temperature from the +60°C figure established in Fig 7.8B for the logic alone.
- The thermal profile still matches well the die-temperatures of portable battery powered SOC products in low-cost plastic packages, and the results are valuable to understand for leakage management control algorithms.

Lessons learned

The ATLAS926 project has proved a very useful vehicle to understand 65-nanometer low leakage processes — and explore the merits of both dynamic voltage scaling on this higher voltage 1.2V technology, and the relative merits of a number of leakage mitigation schemes under development. The chip proved a useful testing ground for RTL design techniques for state retention and on-chip power gating, and strengthened the relation with TSMC and opened up 45nm collaboration potential.

This chip design was demonstrated running MPEG-4 movie decode applications at DAC2006 and the results presented at joint ARM/TSMC customer booth sessions during the conference.

Finally the project provided a prototype development platform for the leakage extensions to the IEC and the basis for a follow-on coarse-grain leakage projected on leakier 90nm "G" technology.
Energy efficient SOC design technology and methodology
8. Patents Filed/Granted

A number of patentable ideas have been generated during the research programme.

**System Control for power management**

- US 6,883,102 developed with two colleagues in the Austin Design Centre
- 5 US patent applications for dynamic performance control, including
  - US 7,181,633
  - US 7,194,647
- 1 US patent application for AMBA bus-based state save and restore
  - US 2004/0153762 close to notice of allowance

**RTL coding for power management**

- US 6,950,951 a protocol for RTL design that reuses the asynchronous reset coding for synthesis as a power ready control acknowledge for multi-voltage design

**Physical IP for leakage management**

- US 7,154,317 developed with David Howard for zero-pin overhead StateSaver retention register
- 3 other patent applications in progress covering
  - power control networks
  - reduced leakage isolation clamps
  - leakage optimized registers

Only the published patents or those with notice of allowance are discussed in this chapter.
Energy efficient SOC design technology and methodology

Figure 8.1 – US 6,883,102 - Power Management Control API Patent

(12) United States Patent
Williams, III et al

(45) Date of Patent: Apr. 19, 2005

(54) APPARATUS AND METHOD FOR PERFORMING POWER MANAGEMENT FUNCTIONS

(73) Assignee - ARM Limited Cambridge (GB)

(5) Notice Subject to any disclaimer, the term of this patent is extended or adjusted under \( \text{USC} \) 154(a) by 546 days.

(21) Appl. No 10/120,511
(22) Filed Dec. 18, 2001

(65) Prior Publication Data

(51) Int. Cl. \( \text{G}06 \text{F} 1/30, \text{G}06 \text{F} 9 / 44 \)
(52) U.S. Cl. \( 713/500, 717/124, 717/123 \)
(56) References Cited
U.S. PATENT DOCUMENTS
5,590,002 A ** 7/1996 Yakin 714/38
5,610,576 A ** 7/1997 Yakin 714/196
5,832,386 A ** 11/1998 Yakin 717/524
5,980,776 A ** 6/1999 Capelle 717/764
5,982,818 A ** 11/1999 Capelle 717/764

* cited by examiner

Primary Examiner—Lynn H Brown
Assistant Examiner—Matthew Henry
Attorneys, Agent, or Firm—McNair & Vanderhye PC

The present invention provides a data processing apparatus and method for testing power management instructions. The data processing apparatus comprises a processor for executing data processing instructions including power management instructions, an associated power management controller, and an interface. A power management controller is also provided for receiving command data from the processor when a command power management instruction is executed by the processor, and to control power management logic to perform the associated set of power management functions dependent on the command data. The data processing apparatus includes first power management logic controllable by the power management controller, with the power management controller also having an interface to enable communications with additional power management logic. In accordance with the present invention, the processor is arranged when executing the command power management instruction to specify within the command data provided to the power management controller whether an emulation mode of operation is set. The power management controller is arranged when the emulation mode is not set to simulate the associated set of power management functions dependent on the command data, whereas if the emulation mode is set it is arranged to only initiate a subset of the associated set of power management functions not requiring communication over the interface. By this approach it is possible to perform some testing of power management software before all aspects of the power management hardware have been designed.

27 Claims, 8 Drawing Sheets

8-2
Developed to support the work of the ARM10 project team in the ARM Austin Design Center

A control interface was developed that mapped the control API (Application Programmer Interface) through a co-processor or memory-mapped interface to abstract the design specific power supply control interface. A secondary node of operation was added to allow the software emulation of entry and exit of various levels of dynamic performance and various depths of sleep, addressing a verification challenge voiced by Operating System companies on simpler hardware focused designs.

An embodiment of the interface was built into the ARM1020E processor macro-cell design.

The API maps between an extensible set of performance level or power states and simple generic interface to power supply controllers with hardware handshake request and acknowledge support.

**Original Submission**

Proposed title

Communications channel and method for communication of power-down state-change events

Novel approach

Architecturally defined co-processor accessible communications channel to provide memory-map independent programming interface to system-specific power controller

- hardware handshake protocols ensuring safe power domain isolation and reset control
- software handshake protocols for OS system portability across SoC designs
- software transparent scheme to support portable OS handler code to support technology dependent features (low-leakage CMOS using clock-gating or high-performance CMOS processes supporting logic/memory power-down)

Applicability

ARM software architectural mode for (applications) processors that run the system power management

Visibility

Software visible CP15 access mechanism ensuring OS 'lock-in' and easy policing of patent infringement
Figure 8.2 – US 6,950,951 RTL Power Control Interface Patent

(45) Date of Patent: Sep 27, 2005

Abstract

Data processing systems (1) having power management control units (8, 10, 14, 16) for one or more power domains (6, 12) are shown in which high power enable request generated by a power controller (8, 14) is encoded or adjusted under 35 USC 154(b) by 92 days.

Primary Examiner—Roberto P. Baldo
Assistant Examiner—Stefan G. Stowers
(74) Attorney Agent, or Firm—Nelson & Vanderhye PLLC

(57) ABSTRACT

Data processing systems (1) having power management control units (8, 10, 14, 16) for one or more power domains (6, 12) show an active high power enable request generated by a power controller (8, 14) to trigger a power supply unit (10, 16) to generate a required power supply signal. Pending valid generation of the power supply signal, or more generally when a power domain is switched off, an active signal which is generated by the power controller (8, 14) and applied to the reset input of the power domain (6, 12) is used to hold the power domain (6, 12) in an inactive reset state. When the power supply signal becomes valid, the active signal releases the power domain (6, 12) to commence operation.
Original Submission:

The novel approach is to re-use the reset signalling – explicit and visible to the RTL designer – as the "power valid" signalling protocol to each and every power domain in a system. Industry standard cell libraries typically offer register functions with active-low asynchronous resets and this is exploited in typical embodiments.

In essence the protocol specifies:

- active-high power domain ‘request’ signalling
- active-low reset handshake to power domain
- active high signalling for all outputs from the power domain to other domains
- active-high signalling on all input signals to the domain other than reset(s)
- optional (AND) gating of outputs from other domains using active-low reset handshake
- optional (AND) gating of power-enable and domain reset to minimize power explicitly to support implementations where there are less physical power domains than explicit system design domains

Highly applicable to:

- Soft-IP creation within ARM to support power domain switching and at platform level for controllable sub-systems
- Potentially a fundamental foundation for AMBA 3.0 interconnect specification (which must be power aware)
- Very appropriate to provide patent cover in negotiations with off-chip power supply regulator manufacturers for external analogue power devices
- Potentially a hook into EDA vendors for tools support for ARM low-power IP

Discoverability/Visibility:

- Compared to the implicit usage of the concept in ARM102xE, the aim is to make this explicitly visible for soft-IP
- Especially easy to ‘police’ as the protocol should be visible between SOC designs and external power controllers – and compatibility with external power controllers employing this protocol

Novelty/Non-obviousness:

- The inventive step claimed builds significantly on simple prior art of ‘voltage valid’ power supply signalling by allowing the HDL (Hardware Design Language) designer to work with design rules that can support multiple power/voltage domains using familiar reset coding styles
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Figure 8.3 – US 2004/0153762 A1 Bus-based state save and restore

(19) United States
(12) Patent Application Publication
(10) Pub No. US 2004/0153762 A1
(43) Pub. Date: Aug. 5, 2004

(54) HARDWARE-DRIVEN STATE SAVE/RESTORE IN A DATA PROCESSING SYSTEM
(73) Inventor: David Walter Flynn, Cambridge (GB)
        Domaino Hugo Synnea, Cherry Haven (GB)

Correspondence Address
NIXON & VANDFRIE, PC
1100 N G.L.3-13 ROAD
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ARLINGTON, VA 22201-4714 (US)

(21) Appl No. 10/691,501
(22) Filed Oct. 24, 2003

CONVENTIONAL CPU IN SOC DESIGN

State data from a system bus 2 is saved in a memory 14 via a system bus 4, 6, 8, 10 under control of a status control 16. The state data may be captured within state chains 12 provided for production test within the system with these state chains supplying respective bits to the multi-bit state saving data words that are stored in the memory via the system bus.
Novel method for high-speed CPU state save/restore for leakage sensitive applications where CPU must be powered down/up for standby efficiency with extensibility for on-chip diagnosis (Dominic Symes’ extension proposal)

Builds on the author's Patent US 5,525,971 granted for the AMBA Test Interface Controller originally developed for full-custom core test purposes

- Configure scan-ready CPU core for 32 scan-chains re-use 32 HRDATA inputs pins as scan-in, 32 HWDATA outputs as scan-out
- Use standard ATPG or core-based test tools for test coverage
- 'Wrap' this CPU core with a thin AMBA (AHB) bus-master sequencer that can also control the scan enable signal

When power management requires CPU to be frozen/powered down

- Sequencer writes all the D-type state to memory in simple burst mode using standard AMBA protocols using a programmed base address (looks to system like a bus master doing lots of buffered word writes)

When power manager needs to wake up the core then, when voltage stable

- Sequencer reads 32-bit data from memory and shifts into scan chains using standard burst reads (looks like lots of cache fills to system)
- Once fully reloaded simply disable scan-enable and re-enable the CPU to start with the entire state restored [This is much easier than trying to use ARM code to reload CPU, Cache control, MMU state, VFP, and internal control state]

Diagnostic usage

DSymes introduced the idea of being able to not only save state but then to re-load the scan-chains in the same manner from diagnostic code "sessions" - including complete test context switching

- Appropriate for safety-critical (automotive) applications where the CPU core may need to have one of a number of diagnostic tests run every millisecond and potentially run whenever the CPU is idle e.g. An ARM7TDMI-S (with 3700+ D-types including full register-bank etc) could be state saved with 116 word writes (for balanced scan chains)
- Which at 120MHz (0 18u target) is only about a microsecond

Patent attributes

- Highly visible as AMBA core is compliance checked
A data processing system includes a processor 44 operable to generate control signals to control one or more further circuits 4, 6 to adopt operational states to support different performance levels of the processor. The one or more further circuits generate current operation signals indicative of their current operation. Examples of further circuits are a clock generator 4 which generates a current operation signal indicative of a currently generated clock signal or possibly currently available clock signals. A voltage controller 6 may be a feature within which serves to provide a power signal to the system and which generates a current operation signal indicative of the current maximum voltage level which the voltage controller is able to supply.

**Figure 8.4** – US 7,181,633 IEC Performance Available Response
During the development of the Intelligent Energy Controller hardware abstraction layer a novel approach to the interface protocol between

- The programmed performance level from the Intelligent Energy Controller (IEC)
- The available performance level(s) from SOC-specific dynamic clock generator
  This supports variable latency PLL lock times on dynamic clock generation and support for minimum bus-clock frequencies always available to ensure "forward progress"
- The available level(s) of voltage from the SOC-specific dynamic voltage controller
  This supports variable latency power supply settling times on dynamic voltage scaling generation and support for reduced level power available to ensure "forward progress"
- the actual performance level fed back to the IEC to support automated hardware fractional performance level accumulation to cope with variable latency clocks and power supply ready timing

A thermometer coding scheme was adopted for each interface. This supports independent bit synchronizing across the multiple clock domains for each of the above interfaces and allows very simple logical gating to determine available performance levels.
Performance control of a processor core 52 is achieved by modulating between a processing mode power supply configuration and a holding mode power supply configuration which the processor core 52 is clocked and a holding mode power supply configuration which the processor core 52 is not clocked. By modulating between these two power supply configuration modes, a target performance level may be achieved and energy consumption whilst in the holding mode can be reduced.
By adding a "BUSY" status signal to a CPU core or processing subsystem to indicate on de-assertion that the system is ready to go idle and all buffered bus transactions are complete, and mandating the use of active high protocol signalling such that all signalling is in an inactive (low) state, the fractional performance control interface developed for the IEC may be used to emulate a multiple step Dynamic Voltage Scaling system simply by controlling a power supply to switch between normal (sufficient to support 100% CPU performance), V_RUN and a retention-level voltage, V_HOLD The control signal would typically be modulated using a Pulse-Width-Modulation (PWM) approach using the logical OR of any IEC hardware "PANIC" wake up request, the "BUSY" status from the processing subsystem and the target PWM mark-to-pace ratio of the IEC target performance level

The "slot" time resolution of the PWM would be in 10's of microseconds and benefit from a fast closed-loop power supply

No changes would be required to the IEC programmer's interface and would allow operating systems to work with traditional multiple-voltage designs

The key advantages are summarised as

- Simple on-off switching of the maximum CPU clock signal is all that is required to emulate reduced rate clocking (allowing smooth interpolation of clock performance levels)
- Support for power supply reduction when the clock is stopped to give both dynamic and leakage energy savings
- No level shifters required between bus and processing subsystem - simply AND-gate style clamp gates
- Standard SOC static timing analysis and verification – at the maximum clock rate of the design
- Re-uses the isolated voltage domain to support state save/restore for isolation when the processing subsystem is to be switched off completely to prevent any leakage
- OS/API transparent, providing a wait-for interrupt and bus transaction flush call is provided in the "idle" task to support both conventional voltage scaling and MAX/MIN switched power supply as described above
- Real time wake-up support by synchronizing the PWM scheme with any panic wake up
- Multi-processor ready - can be shared by one or more processors on shared switched voltage domain In this case all CPU "BUSY" status indicators must be OR-ed together
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Figure 8.6 – US 7,154,317 Zero-pin control overhead “StateSaver” Register
US 7,154,317 Zero-pin control overhead “StateSaver” Retention Register


Patent Idea - StateSaver DFF

This is a type of balloon flop, but has the unusual feature that it requires no more inputs than a standard DFF. This is achieved by using the existing “nReset” and “SE” pins to control the restore and save functions respectively. The nReset pin controls both reset and restore operations, while the SE pin controls both scan-enable and save functions. This behaviour is asynchronous and is independent of the Clk pin. The term “StateSaver register” refers to this new DFF design and “StateSaver latch” refers to the “balloon” latch within it.

There are several benefits of this design:

- The cell will be handled by existing EDA tools with minimal changes to the methodology because all the pins are common to DFFs in many libraries.
- Since there are no extra “save” or “restore” or “sleep” pins on the DFFs, there is no need to build large networks of buffers to drive them. Other retention flops typically have one or more of these pins, and some of these buffers trees must be powered from the non-switched supply, adding to the static leakage problem.
- The cell is interchangeable with a normal (non-retention) DFFR in a netlist, so it will be possible to swap cell types easily prior to layout.
- The StateSaver latch node can be buffered with a single inverter to create a ScanOut pin. This pin exists in some DFF designs to avoid adding unnecessary load onto Q output when connecting up the scan chains. The ScanOut or “SO” pin is typically implemented as Q AND’ed with SE, this prevents it toggling and wasting power when not in scan mode. Since the StateSaver latch only toggles when SE is high, that power-saving functionality is already built into this design, and therefore just a single inverter is needed to drive this output.

System benefits of “StateSaver” registers in IP/SOC design

For many (sub-)system designs only the registers holding architecturally defined state in fact have to be replaced by StateSaver registers reducing the area penalty that all registers would incur. For example for a CPU core all state visible to the programmer must be preserved across power gating sleep periods while other state (micro-TLBs and other transparently cached state, for example) could simple be discarded as long as the state is re-initialized when power is re-applied. It is obviously important that non StateSaver state must be initialized to inactive condition rather than “unknown” or “X-value”
Energy efficient SOC design technology and methodology
9. Publications and Conferences

Most of the specifications and reports generated from the research project portfolio have commercial confidentiality access restrictions. However, the papers that have been published and public presentations that directly result from the research work are summarized in this chapter and the papers attached as Appendix B.

In summary, this chapter documents:

- The initial sARS2 technology demonstrator work resulted in:
  - The invitation to contribute a chapter on Synthesizable ARM IP to a book edited by Kurt Keutzer and David Chinnery (Berkeley University, CA)
  - A keynote address at the Canadian Microelectronics Corporation 2002 workshop
- The DVS926 technology demonstrator resulted in a number of conference presentations and led to ARM product announcements in relation to the Intelligent Energy Manager product and the productized ARM1176JZ(F)-S product with integrated Dynamic Voltage Scaling support:
  - Microprocessor Reports Adaptive Voltage Scaling article built up for Max Baron
  - DesignCon 2003 DVS Hardware and Software presentation and paper
  - HotChips 2003 presentation, Stanford University CA, presentation
  - EE-Times article Jan 2004 publishing the energy savings results
  - DATE 2004 paper and presentation on detailed DVS926 power/energy savings
  - IEE/ACM Colloquium low-power keynote, Sept 2004 at Loughborough University
  - EDA Interoperability Conference presentation, Oct 2004
- The ULTRA926 technology demonstrator generated material for:
  - DAC 2005 All-day Low-power Tutorial using the ULTRA926 as worked DVFS example
  - SOC Conference 2005, Newport Beach, low power design flow panelist
  - DAC 2006 UMC Voltage Scaling and Energy Savings presentation and demonstration
- Leakage Mitigation work:
  - ARM Developers Conference, Santa Clara 2005, leakage management approaches
  - DAC 2006 TSMC Voltage Scaling and Energy Savings presentation and demonstration
  - ARM Developers Conference, Santa Clara 2006, low power panelist
- Finally, contract in place as primary author for 2007 publication in preparation:
  - Low Power SOC Methodology Manual to be published by Springer
  - Scheduled for DAC 2007 launch, volume publication from July 2007
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Figure 9.1A - "Creating Synthesizable ARM Processors with Near-Custom Performance"

Tools and Techniques for High-Performance ASIC Design
David Chinnery
Kurt Keutzer

Figure 9.1B - Canadian Microelectronics Corporation keynote

CANADIAN SYSTEM-ON-CHIP WORKSHOP 2002
July 5, 2002
Banff Conference Centre, Banff, Canada
Proceedings

The opportunity to configure your research platform!

Morning Program (Chair: Hugh Polliitt-Smith, CMC)

Goal: To inform the research community on the status of the SOCRN and then gather information leading to important decisions on what direction to take on key technical topics.

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"Creating Synthesizable ARM Processors with Near-Custom Performance"

Guest author of Chapter 17 (with Michael Keating at Synopsys adding the EDA material) of "Closing the Gap between ASIC and Custom" compiled by Kurt Keutzer and David Chinnery University of California, Berkeley, published by Kluwer 2002, ISBN 1-4020-7113-2. (Figure 9.1A).

The request to write this had come via Michael Keating at Synopsys as a result of the sARS2 technology project collaboration and earlier work as a contributor to his “Reuse Methodology Manual” which has wide industry recognition as best practice for design for synthesis.

Based on material generated and learnt from the experience of re-architecting the ARM7TDMI processor from a full-custom design to a widely licensable core for standard synthesis design flows, with interface re-design for ease of integration. The final drafts were written up around the time of the 2002 DATE conference in Paris and Mike Keating helped expand out the Synopsys related EDA flow sections before the a technical writer in Mountain View finalised the style and presentation.

The book went to the publishers (Kluwer Publishing, Inc.) on 1st April 2002, and was published 1st May 2002.

Canadian Microelectronics Corporation keynote presentation

The Canadian Microelectronics Corporation is a non-profit corporation that provides Canadian Universities with design tools and resources, manufacturing technology and centralized IP repository by taking on the procurement and licensing framework on behalf of individual university research groups.

CMC licensed the ARM7TDMI CPU macro-cell for university SOC project integration in 2002 and invited a keynote presentation on SOC design with microprocessor IP cores.

The presentation proved a useful opportunity to bring together the learning experiences from the sARS2 reference design particularly with respect to the

The presentation was given at a SOC Workshop hosted by CMC in July in Banff – see Figure 9.1B. The presentation was archived with the Canadian System-On-Chip Workshop 2002 proceedings.

1 http://www.eecs.berkeley.edu/~chinnery/asic_vs_custom_speed/book_chapters.html
2 http://www.springer.com/uk/home/engineering/circuits+%26+systems?SGWID=3-40604-22-33340599-detailsPage=pmmmediaaltoc
Figure 9.2A – Dynamic & Adaptive Voltage Scaling paper built for MPR

Memory speed is no longer guilty of limiting processor performance. The infamous title has been awarded to battery capacity. Cellular telephones, PDAs, notebooks, and portable multimedia devices could bring higher microprocessor revenues and more rewarding.

Figure 9.2B – DesignCon paper jointly with National Semiconductor

2003 Archive

Highlights | Schedule | Exhibitor List

2003 DesignCon Schedule

January 27–30, 2003

Tuesday, January 28

11:00 am - 11:50 am

SA2-3

A Combined Hardware-Software Approach for Low-Power SoCs: Applying Adaptive Voltage Scaling and the Vertigo Performance-Setting Algorithms
Dynamic & Adaptive Voltage Scaling paper built for Micro-Processor Reports

Max Barron at MPR approached ARM to understand and write up the IEM + Adaptive Voltage Scaling technology announced in November 2002. The author worked on the system diagrams, based on the DVS926 project work and the IEM control framework, and also helped furnish the power and energy savings predicted and achievable, justified by measured data from early National Semiconductor AVS silicon. (See Fig 9.2A for example of the system diagrams produced).

The article was turned around at high speed in order to meet publication in the second (bi-weekly) January edition of Micro-Processor Reports, a respected industry reference for ARM customers:

Analog and CPU Wizards Reduce Digital Power
Max Baron - Principal Analyst (01/21/2003)

In November 2002, National Semiconductor Corp. and ARM announced a strategic business relationship to jointly develop and market power-efficient systems that, they claim, will increase the battery life of handheld portable devices in several stages—from 25% to as much as 400%. The two companies' joint effort will leverage ARM's penetration in the mobile-phone market and National Semiconductor's expertise in analog design and power management.

NSC and ARM's joint project aims to create circuits, software, and tools that address three energy-consumption tasks: frequency reduction, minimal voltage levels to support it, and reduction of leakage current.

Microprocessor Report readers can access the full story here:

https://www.mdronline.com/publications/epw/issues/epw_158.html

DesignCon 2003 Paper and Presentation

A joint paper between ARM and National Semiconductor was presented at the end of January4:

- Krisztian Flautner presented the IEM software framework (Vertigo codename from original University of Michigan PhD project that was the control basis for ARM DVFS)
- Mark Rives from National Semiconductor presented the Adaptive Voltage Scaling IP and early results from 0.18um test chip project
- The author presented the system design, implementation and analysis work and detailed information on the synchronous design challenges with DVFS and proposed solutions.

ANALOGandDSP - News and technical information about...
Published on: 1/2/2005
By Krisztian Flautner, Principal Research Engineer, David Flynn, a Fellow in the Research and Development group, ARM, Inc., and Mark Rives, Principal Applications Engineer, NatSemi Corp.

4 www.analoganddsp.com/results.asp?entryid=6067

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Figure 9.3A – HotChips 2003 presentation

Figure 9.3B – HotChips 2003 DVS926 project publicised
HotChips 2003 “Intelligent Energy Management” presentation

ARM was invited to present a paper at HotChips conference in 2003 and the IEM prototype work based on the DVS926 project was chosen as the technology to highlight – although at some risk given that the silicon only arrived out of fabrication the month before the conference and due to chip packaging issues was not available to show physically at the conference. The device sprang to life the week after the conference, in time for the ARM Partner Meeting hosted in Cambridge following on from HotChips.

Figure 9.3A describes this particular industry conference and context. The conference historically focus on high speed processors typically fabricated as stand-alone components so the ARM IP macrocells appear in the Embedded session/track.

The presentation was split into three primary sections:

- The whole case for DVFS, focussing on energy metric rather than dynamic power dissipation that is well understood by the CPU community. Because results were not yet available from the DVS926 project, measured data from a 0.18um ARM926 testchip were used to set the context as well as predicted figures from the IEM prototype project.

- The performance control software. This is difficult to convey and yet is the fundamental concept to convey in order to be able to exploit the dynamic performance and voltage scaling hardware. To an audience that is primarily hardware-focussed a number of slides were developed to build up the case for how the operating system builds up a view of the varying application load and task deadlines without having to touch the application code.
  - A projected movie was presented with both the MPEG frame playback and an annotated dynamic performance prediction graph overlayed to show visually how the OS-based task performance monitoring and scheduling behaves with IEM policies.

- The hardware control approach, and the underlying design challenges to be addressed to support voltage scaling within standard EDA tools environment:
  - The Intelligent Energy Controller design was presented and the interfaces to clock generator and DVS/AVE power controller discussed along with how the interfaces are abstracted to give a unified fractional view of performance requested and monitored taking into account the granularity of control and PSU-specific ramp-time constants.
  - How the National Semiconductor Adaptive Voltage Scaling is interfaced and controlled.
  - An overview of the implementation complexities from a tools and library characterization perspective.

Figure 9.3B shows a slide from the presentation looking forward to the actual silicon results.

Acknowledgements to Dr Kris Flautner for work on the instrumented movie, and to Clive Watts for integrating the marketing material for the IEM software and National Semiconductor PowerWise hardware.

Archives | HOT CHIPS 15
www.hotchips.org/archives/hc15
Intelligent Energy Management: an SoC Design Based on ARM926EJ-S, David Flynn (ARM)
The latest portable devices—from mobile phones to media players—offer a host of new Internet, multimedia and gaming features that place a significant strain on batteries. So the quest to optimize system-wide power use and maximize battery life has led four companies—ARM, Artisan, National and Synopsys—to collaborate on the design of power-saving intellectual property (IP) and systems-on-chip (SoC) that reduce dynamic power consumption based on application software workload, available silicon performance and environmental conditions.

Here’s how they met the challenge.

In 2003, ARM and Synopsys collaborated with National and Artisan on an SoC test chip that can dramatically increase the battery life of portable devices. The SoC was based on IP that intelligently and dynamically adjusts performance and power consumption to maximize energy conservation.

The chip addressed dynamic frequency and voltage scaling, implemented multiple power and clock domains and targeted a 0.13-micron process from Taiwan Semiconductor Manufacturing Co. (TSMC).

The design was partitioned into three primary on-chip power domains:

- A voltage-scaled CPU power domain, which featured level shifters, a retiming interface to the main SoC and a separate VDD CPU power ring and pads for supply rails. This scaled-voltage domain includes National’s PowerWise hardware performance monitor, which was realized using the same cell library as the CPU.
- A voltage-scaled memory power domain, which featured a dual 16-kbyte instruction, a data scratch pad RAM suitable for a state save-and-restore when the CPU is turned off (for example, when implementing software-controlled leakage management), isolation clamp cells to the CPU a VDD RAM power ring and individual supply pads.
- A standard SoC fixed-voltage, “always-on” power domain for the rest of the chip, which featured SDRAM and flash memory controllers, real-time peripherals and power control. The test chip was implemented and verified in four steps, using Synopsys’ Galaxy Design Platform (Fig. 1).
DVS/AVS Evaluation results for EE-times, Jan 2004

The collaborative partnership of ARM, Artisan, Synopsys and National Semiconductor plus TSMC who had fabricated the DVS926 system-on-chip implementation chose to publicise the evaluation results from the ARM silicon analysis.

An article was written for EE-times which discussed how the multi-voltage SOC design was partitioned and implemented and the power and energy savings achievable on "near-typical" silicon – and in particular how National’s Adaptive Voltage Scaling technology had been integrated in order to support both process and temperature compensation to minimize voltage headroom.

The diagrams and graphed results were the primary technical input were produced at the end of 2003 and the final article incorporating data to satisfy each collaborating party was final published in January 2004.
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Figure 9.5A – DATE, Feb 2004

Figure 9.5B – IEE/ACM Colloquium keynote, Sept 2004
DATE, Feb 2004

The Design And Test, Europe conference is an important forum for customers and licensees of ARM technology. A more detailed paper on the measurable energy savings for a cached CPU core such as the widely licensed ARM926 was chosen as an important paper to target for this conference. DATE as a conference favours papers that cover real-world experimental results and analysis and the measured results from the DVS926 silicon were just available in time to meet the submission deadlines that DATE sets in order to ensure peer review and acceptance.

The paper was co-authored with thee colleagues, Kris Flautner who was the architect behind the DVFS prediction control software, and Dipesh Patel and Dave Roberts who had helped work on the implementation and evaluation aspects respectively. See Figure 9-5A.

The paper  generated a lot of interest and became a valuable reference to use when engaging with prospective licensees and customers of the IEM software and IEM-enable microprocessor cores.

Abstract

One of today's most successful embedded devices, the mobile phone, embodies a set of challenging design requirements: long battery life, small size, high performance and low cost. The single parameter that complicates the simultaneous fulfilment of all of these design goals is energy efficiency of the system, since batteries only hold a finite amount of charge. To operate within the allotted energy budget, systems must be optimized for energy consumption during design and also at run-time. Increasingly it is not sufficient to statically optimize for worst-case conditions but designers must enable systems to adapt to conditions at runtime. The Intelligent Energy Manager™ (IEM) technology provides an integrated solution for addressing energy management of SoC devices. In this paper we present data about the energy consumption characteristics of a multiple power-domain based SoC which includes PDA functionality built around an ARM926EJ-S core.

IEE/ACM Colloquium keynote, Sept 2004

Loughborough University, the IEE Professional Network on System-On-Chip and the Association for Computing Machinery (ACM) Special Interest Group on Design Automation hosted a postgraduate colloquium focussed on Embedded Software, Hardware implementations and hardware-software co-design from the SoC perspective.

The invitation to present the afternoon keynote session gave the opportunity to not only present the systems-based approach to manage both hardware and software components but to also present live the demonstration system running MPEG video decode displayed on the conference projector which helped make the material come to life. (Ideal for the after-lunch slot!) See Figure 9-5B.

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Energy efficient SOC design technology and methodology

Figure 9.6A – Synopsys EDA Interoperability Conference Oct 2004

14th Synopsys EDA Interoperability Developers’ Forum
October 21, 2004
Sun Conference Center, Santa Clara, CA at Agnews Historic Park

Keynote: The Next Big IC Design Discontinuity
Professor A. Richard Newton
Dean of the College of Engineering and the Roy W. Carlson Professor of Engineering,
University of California Berkeley

What Is the Developers’ Forum?
This Forum provides EDA vendors and their customers an opportunity to exchange information and ideas on EDA tool interoperability including information on new interface technologies, future enhancements, upcoming news, and successes from developers and customers. Topics and formats discussed will include Liberty, Milkyway, SDC and SystemVerilog. For more information on these formats, please visit the TAP-in and MAP-in program web pages. Please join us in promoting increased interoperability in the EDA industry.

The slides presented at the October 2004 Developers’ Forum will only be available at the event. Please plan to attend the Forum. Register for this event now at no charge.

Agenda Highlights
7:45AM - 2:15PM  General Session (Lunch Included)
Keynote: Professor A. Richard Newton - U.C. Berkeley
2:30PM - 5:00PM  Breakout Sessions
Track 1 - Low Power Forum

Figure 9.6B – Synopsys EDA IDF Oct 2004 – Low power track based on DVS926

3:00PM - 5:00PM  Track 1 - Low Power Forum
The Elements of the Most Energy Efficient SoC Design

3:00PM  ARM IEM and System-Level Power Management -- Clive Watts and David Flynn, ARM Ltd
Design for Lower Power,
Synopsis/ARM IEM
Reference Methodology and
Other Design Techniques -- Barry Pangre, Synopsys
PowerWise Technology for
Power Supply and Voltage
Control -- Gordon Mortensen, National Semiconductor
Silicon IP for Low Power Design -- Rob Atkhen, Artisan Components

IEM Technology and Interoperability
IEM provides Dynamic Performance Scaling, but...
| IEM-enabled (CPU) cores require |
| Level-shifter interfaces, isolation clamps |
| Library IP, fast-settling PLLs |
| Extended characterization for cell libraries, memory |
| Power-aware RTL coding |
| Global power/ground in current HDLs inadequate |
| Careful hierarchical design for now |
| Latency-aware clock design |
| Clock tree balancing becomes dynamic challenge |
| Either asynchronous or complex clock generation |
| Comprehensive implementation and analysis EDA |
| Plus verification, test and production yield extensions |

ARM 166 ARCHITECTURE FOR THE DIGITAL WORLD™
Energy efficient SOC design technology and methodology

**Synopsys EDA Interoperability Developers Conference Oct 2004**

A presentation was invited by Synopsys to cover.

Clive Watts, the product manager at the time for the Intelligent Energy Manager software product covered the basic overview of how the software control framework and policy manager fit into the system and OS design.

The author presented the primary technical requirements on the EDA tools and library IP components to allow clean design flows and interoperability with different front-end and back-end tools.

**Figure 9.6A** describes this particular industry conference and context.

The systems-level challenge of DVFS and IEM proved a useful framework for the Low Power forum:

- Systems level challenges from the perspective of IP provider and system-on-chip integrator. The DVS926 project was used as the basis for the technical justification:
  - As shown in the summary slide shown in **Figure 9.6B** the challenges to EDA, library and power controller suppliers as well as the need to enhance RTL coding to support multi-voltage design all introduced, and then addressed from the collaborative technology demonstrator project perspective.

- EDA implementation and analysis – using the worked examples from the DVS926 project that Synopsys had worked on and learned from.

- Interfacing to on-chip and off-chip power supply controllers – again using the DVS926 project that National Semiconductors had used as the reference system design for PowerWise prototype.

- The physical library components (primarily level shifters and isolation clamps) and the expensive library re-characterization to support DVFS timing constraints and analysis specified as a result of the DVS926 project. This section presented by Rob Aitken who was later to become the ARM Physical IP R&D director after Artisan Components acquired by ARM. (The ULTRA926 project was running confidentially at this stage and provided the requirements specification for the "Multi-Voltage Kit" components discussed as the basic interoperability components requiring EDA support)

Increasingly the success of the IEM hardware and software was being seen commercially as dependent on the design tools and flows to support both design and verification. Visibility at such EDA conferences and the opportunity to present the challenges and requirements in a customer forum has proved and will continue to prove very valuable in getting tools and methodologies in place to enable successful multi-voltage product designs in the wider market than just the major IDMs.
Overview

- Systems level challenge
  - SW/SOC/PSU design, EDA/Library implications
- Dynamic Power/Energy Management
  - Dynamic Voltage and Frequency Scaling
  - Real-world design issues
- Static/Leakage Power Management
  - Multiple power management states
- Work in progress...

Morning session (Based on ULTRA926)

Afternoon session (Leakage Mitigation)
DAC 2005 – All-day low power tutorial

The ULTRA926 DVFS project and leakage mitigation work in progress presented at Friday tutorial:

**TUTORIAL 4) Advancements in Energy-Efficient Design** (See Figure 9.7A)

Organizers: Barry Pangrle

Speakers: David Flynn - ARM Ltd., Cambridge, UK (See Figure 9.7B)
David Tamura - National Semiconductor, Santa Clara, CA
David Blaauw - Univ. of Michigan, Ann Arbor, MI
Barry Pangrle - Synopsys, Inc., Mountain View, CA

DAC 2005 – Low Power Panellist

From EE-times conference panel report by Ron Wilson:

"A more ambitious design was described in a panel sponsored by Synopsys, and including speakers from ARM and Toshiba. This design was also an ARM processor: in this case an ARM1176 demonstration. ARM fellow David Flynn and Synopsys fellow Mike Keating described a design that employed more invasive techniques and more manual assistance than the Cadence-described flow.

In addition to the usual logic optimization and multi-threshold techniques, this design used dynamic voltage-frequency scaling—a technique that ARM for one has been discussing for a year or so, but that adds considerable complexity to the tool flow. It also employed power gating, which though simple in principle, also adds remarkable complexity.

Both techniques require very careful thought in partitioning the design, Flynn warned. Decisions based on timing requirement perceptions may have implications not only for the end performance of the chip, but also for the layout complexity and the amount of energy actually saved.

Voltage scaling of course requires level shifters between voltage regions. But if voltage is scaled dynamically, nets that cross the boundaries must be checked for timing, signal integrity, electro-migration and other issues across all the possible combinations of voltages. Clamps may be needed to hold the outputs of a block at a known level while the block is inactive. And if frequencies are scaled as well, signals may have to be resynchronized between blocks.

Even just turning the power off to a block can be complex, the researchers observed. Power gating can be done either on a very fine granularity, by placing a switch at the foot of each ground path, or on a block level, creating a virtual ground for each block. In the former case, the switch is now in the signal path, and must be sized to meet timing constraints. "That one transistor that turns off the power can be larger than a two-input NAND gate," Keating said.

In addition, state must be saved somehow. In this design, Artisan registers with low-leakage shadow flip-flops were used, so that on a signal the state of the register could be transferred to the shadow or restored from it. And output clamps are needed to keep outputs from a powered-down block from crow barring the next block down the line. Further, the only tool available today to predict the transient behaviour of the power grid is SPICE.

Altogether there is considerable energy expenditure in powering down a block. This makes it necessary to have enough application knowledge to know when the block can be inactive long enough to make the effort worthwhile.

The impression from the panel was that such aggressive techniques were feasible, and the rewards worth it, but today the undertaking is not for the faint-hearted. Major steps are being taken by both tool and library vendors to automate the hard spots, but it appears the architectural-level decisions, specifically about partitioning and knowing when a block can be slowed or shut down, will remain challenging."

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http://www.eetimes.com/news/design/technology/showArticle.jhtml?articleID=164900311
Power and energy management is an important aspect for consideration in any SoC or overall product design. As leakage current will play a more significant role in the future, measures must be taken to control leakage and ensure power and energy usage remain as low as possible. On the current generation of process technologies, leakage accounts for about 20% of the overall power/energy budget; on subsequent process geometries, this is nearing 40-50%. Future SoCs on process technologies of 60nm and beyond will require additional techniques in both hardware and software to manage leakage. This presentation explores some of the areas ARM is actively working on to minimize leakage current.

9.8B – International SOC Conference Panel, Nov 2005

Panel: Low Power Design Challenges in Complex SoC & ASIC Designs
Moderator: Ron Wilson, Editor, EE Times.
Panelists:
1. Sunil Balse, VP Marketing, K-Micro
2. David Flynn, Engineering Fellow, ARM
3. Steve Lefebvre, Technology Evangelist, Tensilica
4. Susan Runowicz-Smith, Cadence-Silicon Design Chain Initiative
5. TDO - Toshiba
6. Wing-Yu Leung, CTO, MsiSys.
Energy efficient SOC design technology and methodology

**ARM Developers Conference Leakage Mitigation presentation, Oct 2005**

This inaugural conference hosted in Santa Clara was targeted at both software and ASIC developers and engineers in the Silicon Valley area. Working with the product manager of the IEM embedded software and an EDA tools expert a presentation covering the extensions to the IEM product roadmap to support a range of leakage mitigation techniques was produced. See Figure 9-8A.

Without publicly naming the leakage projects at this stage the technology portion of the presentation covered the leakage mitigation techniques under evaluation:

- ARM926-based
  - Key to meeting shuttle die area targets (-> 4x4mm -> 3.5x3.5 mm)
  - Reuse Linux port and IEM ‘policy stack’ development environment
  - Reuse existing IEM evaluation and development systems

- Multiple voltage domains
  - DVFS support (more for 1.2V LP process than 1V G/OD)
  - Allow independent V/I measurement across domains

- Support power-gating (MTCMOS) strategies
  - RTL handshakes to drive distributed/fine-grain power switches
  - First prototype of IECv2 for intelligent leakage control
  - Support for novel Retention Registers for “Light sleep”
  - Support for novel AMBA-based block hibernate/wake “Deep sleep”

- Optional support of (VTCMOS) forward/reverse bias control
  - Despite lack of EDA multi-dimensional timing models

**3rd International SOC Conference panellist, Nov 2005**

The invitation to represent ARM at this SOC conference hosted in Newport Beach was accepted and the opportunity used to build credibility for the synergy potential for both physical and synthesizable IP from ARM in the year that Artisan Components had been acquired.

The panel was entitled “Low Power Design Challenges in Complex SOC and ASIC Designs”. See Figure 9.8B. The moderator was Ron Wilson who subsequently reported the highlights in EE-Times 7.

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NEWPORT BEACH, Calif. — A panel discussion at the 3rd International System-on-Chip Conference here this week attempted to skip past the academic science projects and the rosy vendor marketing and explore what was really feasible today in the challenging area of power management. ...

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Energy efficient SOC design technology and methodology

Fig 9.9A – Design Automation Conference Jul 2006 – ATLAS65LP presentations

2006 43rd DESIGN AUTOMATION CONFERENCE
July 24 - 28, 2006, Moscone Center, San Francisco, California

Leakage Power Analysis

- Correlating measurements
  - IV analysis for CPU+RAM
  - NB beyond functional range
- HALT
  - Std cell + RAM leakage
- LIGHT SLEEP
  - Lvl Std cell power gated
  - Retention registers active
  - + RAM leakage
- DEEP SLEEP
  - Just RAM leakage

Compared to ~0.3mW leakage power, 25C typical 65LP sample

ULTRA926 “IEM” Evaluation platform

- Fully function silicon
  - 128MByte SDRAM
  - 8 MByte FLASH
  - VGA display support
  - Measurable power rails

- Intelligent Energy Manager
  - Software MPEG-4 playback
  - Recalculate performance every frame of 25 frame-per second
  - Graph predicted versus actual 288/240/192/144MHz levels
  - Wait-for-Interrupt if any slack

Fig 9.9B – Design Automation Conference Jul 2006 – ULTRA926 presentations
Energy efficient SOC design technology and methodology

The Design Automation Conference in San Francisco in July 2006 proved to be an important showcase for the technology demonstrators developed with both TSMC on advanced 65nm-LP process and UMC on 130nm "Fusion" technology.

Screening the untested test chips and getting these assembled on surface-mount technology evaluation platforms proved very tight and the exhibition systems were hand-couriered out the weekend the exhibition was being set-up. Two sets each of TSMC and UMC evaluation systems were commissioned to allow for both the foundry partner and ARM to have systems and to provide some form of backup.

The ARM booth in the exhibition centre ran demonstrations of both ULTRA926 and ATLAS926 running IEM application workloads with voltage scaling and both TSMC and UMC exhibited systems running real-time dynamic performance scaling of MPEG video workloads.

Design Automation Conference 2006 – TSMC ATLAS926-65LP

The author presented the ARM evaluation results for the 65nm leakage and DVFS project at a number of TSMC-hosted customer presentations.

An example of the leakage results disclosed showing the leakage power reduction for the mitigation schemes implemented on this technology demonstrator is shown in Figure 9-9A.

Considerable customer interest and follow up resulted from these presentations.

Design Automation Conference 2006 – TSMC ATLAS926-65LP

The author presented the ARM evaluation results for the 130nm DVFS project at a number of UMC exhibition floor presentations.

Alongside the presentations a running evaluation system was displayed and the setup is described in Figure 9-9B.

Again considerable customer interest and follow up resulted from these presentations and a follow on technology demonstrator project requested by UMC.
Fast Track to Lower Power Luncheon Panel

Panel of experts in IP, tools and methodology will present the challenges and solutions for implementing high-performance, low-power SoCs that are fueling the growth of the electronic business, based on results from extensive collaborative technology development. In addition to explaining the science behind the architectural and design challenges, the panel will present examples of design solutions using special IP and design automation, which enable leading-edge product performance and battery life. The panelists will also share their insights into the future of ultra low-power and high-performance design and automation. Examples of topics to be covered include: dynamic voltage scaling, power gating, power grid creation and analysis, Intelligent Energy Manager (IEM) technology, verification, and physical IP.

Hosts:
John Chilton, General Manager, IP & Systems Group, Synopsys
Mike Muller, CTO, ARM

Panel Speakers:
Frederic Nyer, ST Microelectronics
Alan Gibbons, Principal Engineer, Synopsys
David Flynn, ARM Fellow
Stephen Meier, VP, Engineering, Synopsys
Rob Aitken, ARM Fellow

Technology Demonstrator Results So Far...

- Four primary levels of IEM leakage management:
  - HALT/SRPG/SCAN-HIBERNATE plus SHUTDOWN for CPU
- Working 65nm LP silicon evaluated (see on ARM Booth)
  - Supports DVFS for IEM dynamic energy saving
  - Important with 1.2V LP
  - SRPG Savings of 65% measurable
  - Compared to the static ~0.3mW leakage
- 90nm G project just out of fabrication
  - Distributed header power gating with inrush control
  - Dynamic threshold scaling leakage management
  - Both CPU plus USB subsystem leakage management
  - State retention noise immunity and safety measurement analysis
Energy efficient SOC design technology and methodology

The second ARM Developers Conference in Santa Clara provided the forum to showcase the ATLAS926 and ULTRA926 working silicon to the wider ARM developer community and to begin to reveal publicly details of the SALT926 project alluded to the year before. The original plan had been to have demonstrable silicon in time for this conference but at this stage the silicon had only just emerged from fabrication and was awaiting packaging.

With the aim of encouraging vendors and partners to present at the ARM conference rather than ARM staff a presentation was co-written with Synopsys that Alan Gibbons delivered for the system-level power management track:

Techniques for Aggressive Leakage Management in ARM Systems

Presented by Alan Gibbons, Synopsys

Room 210

3:00 PM - 3:45 PM

At 65nm and below, minimizing the static power dissipation through aggressive techniques such as coarse grain MTCMOS power gating and threshold voltage scaling can yield, the significant reductions in power consumption that are necessary to derive high-performance, complex applications on mobile platforms. ARM and Synopsys have jointly developed a comprehensive low power technology demonstrator that employs these advanced low power techniques. Various alternative approaches to MTCMOS power gating and threshold voltage scaling are discussed together with a detailed description of the implementation flow and the results.

ARM Developers Conference, Oct 2006 – Panellist

ARM and Synopsys jointly sponsored a low power panel to address the progress and remaining challenges in delivering synthesizable IP, methodologies, tools and physical IP libraries which provoked lively discussion and a lot of follow up questions and dialogue. See Figure 9-10A.

The System-level leakage management slides presented included a summary of the system control challenges, the analysis and verification tools EDA requirements and visibility of the R&D projects ongoing to come up with worked SOC examples - see Figure 9-10B for an example slide that showed the technology being evaluated in detail.

9-21
Energy efficient SOC design technology and methodology
10. Conclusions and Future Work

Evaluating the “Energy efficient SOC design technology and methodology” goals

The results for the work covered in this thesis are summarised in this chapter. The focus of the work has very much been building on the earlier academic research framework in order to demonstrate real-world applicability in standard EDA design flows. The applied R&D has resulted number of novel technology components and techniques have been developed that can now be reused with commercial customers and EDA partners.

In order to evaluate the value of the applied R&D portfolio of projects evidence has been gathered in the following areas:

- Licensable products resulting from the research projects
  - The “Intelligent Energy Controller” (IEC) hardware API to manage dynamic performance setting and monitoring in a SOC-reusable product[1]
  - The “Intelligent Energy Manager” (IEM) software product development platform, deployment model and OS/SOC portable interfaces[2]
  - The ARM1176EZ(F)-S CPU multi-voltage design partitioning and interface definition for DVFS SOC deployment, setting the foundation for the multi-voltage CPU specifications for the ARM “Cortex™” family.[3]
  - Physical IP specifications for the ARM/Artisan “Power Management Kit” in the form of level-shifters with integrated isolation functionality, and power-gating and state-retention standard cell components licensed to a number of foundries and customers[5]

- Results and expertise developed from the representative technology demonstrators
  - Functional, measurable silicon on technology nodes from 180nm to 65nm over 5 generations.[6][7][8]
  - Dynamic Voltage and Frequency Scaling designs that allowed precise power and energy measurement, analysis and quantifying energy savings. The designs drove the specifications of physical IP components and provided real-world world-examples for EDA companies to work with in order to develop methodologies suitable for non-expert customers.[7]
  - Leakage-management techniques that can be applied as a “standard-cell” design flow rather than requiring expert-level transistor level knowledge and visibility to support a number of system-level leakage mitigation schemes.[8]
Energy efficient SOC design technology and methodology

Figure 10.1A– Low Power Methodology Manual, Springer 2007

Figure 10.1B– Low Power Methodology Manual primary author contributions

Introductory chapters and USB IP Design example, authored by Mike Keating
- Chapter 1: Overview of the challenges and basic approach to low power design.
- Chapter 2: Basic power reduction techniques
- Chapter 3: Multi-voltage design, focusing on architecture and design issues.
- Chapter 8: IP design for power gating, a USB subsystem example.

Authored by David Flynn: Power Gating
- Chapter 4: Power gating Overview
- Chapter 5: RTL Design for power gating
- Chapter 6: Worked example of a power gated chip design at the RTL level
- Chapter 7: Architectural design issues in power gating.

Authored by David Flynn: Dynamic Voltage and Frequency Scaling
- Chapter 9: RTL and system design for dynamic voltage and frequency scaling
- Chapter 10: Worked examples of voltage and frequency scaling

Authored by David Flynn: Physical Library and Memory IP
- Chapter 12: Physical cell library and memory requirements for multi-voltage design
- Chapter 13 discusses retention register design and data retention in memories

Authored by Alan Gibbons:
- Chapter 11: Implementation issues in low power design: synthesis, place and route, timing analysis and power analysis

Authored by Kajian Shi:
- Chapter 14 The design of the power switching network
Conclusions and Future Work

- **Industry text book contributions**

- **Credibility with end-customers and EDA tools providers**
  - Increasingly the challenge of low-power has to be addressed as a system level problem and needs to span transistors/physical IP, RTL design, on- and off-chip power supply technology. But one also requires low-power implementation and analysis tools, as well as Operating System level software, device drivers and extensible control schemes. The SOC-level technology demonstrators have indeed provided several generations of hardware platforms that have enabled a number of OS providers to port and demonstrate their power-management schemes and measured energy savings [10][11]
  - As an IP company the technology demonstrator programme has been credibility to engage with expert OEMs and advanced technology licensees with regard to low power. The technology demonstrator programme has enabled ARM to share results and work closer with industry-leading mobile phone manufacturers to jointly understand the significant usage profiles that affect active and standby battery life and the value of different energy management approaches [12][13]
  - The board-level evaluation and development platforms were not only important and influential from an exhibition and trade-show perspective but also became a valuable "loan" resource to allow potential customers to benchmark their own proprietary and commercially sensitive workloads and benchmarks under the project's Linux OS environment. This was the key for some early adopters to evaluate the IEM software product
  - Following the acquisition of Artisan Components the programme has been a driver for "synergy" between the synthesizable IP (processor, data engines and AMBA bus components) and the cell library and memory enhancements to derive lower power, more energy efficient SOC implementations. The early "Multi-Voltage Kits" and subsequent "Power Management Kits" embody a number of the components and inventions developed under the auspices of research for this thesis [5]
Energy efficient SOC design technology and methodology
Conclusions and Future Work

Canonical SOC Design – 5 Generations
A number of ARM licensees and customers have show interest in joint development projects but the problem has always been that the data from such collaborations is typically always commercially restricted and non-shareable with other companies or EDA partners.
The major benefit to ARM of basing the research and development upon an in-house canonical design was that there was no dependence upon external commercially restricted customer IP which then meant that the results from analysis were under ARM's control. Rather than having to incorporate the full complexity of an end-product SOC design the research has been able to focus on representative complexity in terms of multiple clock domains, power domains and baseline operating system platforms sufficient to focus on best practice implementation methodologies. All the dynamic and leakage energy savings for an ARM926 processor core are of higher value for larger and more complex CPU cores that typically consume a greater proportion of the end-product power budget. Chapter 2 summarizes the successful evolution of the initial design across four more generations with increasing power management sophistication.

- SOC#1 – sARS2 “Audio Reference System Design”
  o 180nm TSMC standard low-power synthesis/place-and-route baseline design
- SOC#2 – DVS926 “Dynamic Voltage Scaling Demonstrator”
  o 130nm TSMC technology design for DVS and experimental Adaptive Voltage Scaling prototype, with Linux OS support
- SOC#3 – ULTRA926 “DVFS Reference System Design”
  o 130nm UMC technology higher performance design for DVS using a re-characterized Foundry CPU core plus AVS
- SOC#4 – ATLAS926-65LP “Leakage and DVFS Demonstrator”
  o 65nm TSMC Low-Leakage, 1.2V technology design for leakage mitigation and DVS with experimental leakage management control IP
- SOC#5 – SALT926-90G “Leakage/Physical-IP Demonstrator”
  o 90nm TSMC Low-Leakage, 1.0V technology design for aggressive leakage mitigation and with experimental State-Retention/Power-Gating control and analysis management IP

Best Practice Design for Low Dynamic Power – DVFS
The major achievements to grow out of the voltage scaling technology demonstrators designs described in Chapter 3 are summarized as

- Multi-voltage partitioning of DVS-enabled processor products, initially the ARM1176 with RAM, CPU and SOC power domains with asynchronous bus interface layering to support variable clock latency management
- Power/Test/Reset/Clocking Requirements in detail as developed with EDA partners and worked examples based on ARM926-based SOC
- The first realization of complete Linux-based Intelligent Energy Manager System-on-chip with IEC and IEM deployment
Energy efficient SOC design technology and methodology
Conclusions and Future Work

• Adaptive Voltage Scaling reference design for joint ARM/National Semiconductor engagement with customers
• Novel dynamic performance control techniques and prototypes

Best Practice Design for State-Retention Power-Gating – SRPG
The major achievements to grow out of the SRPG demonstrators designs described in Chapter 4 are summarized as

• Multi-level leakage management techniques transparently overlaid on ARM "wait-for-interrupt" instruction set support
• Leakage mitigation state machine controllers for safe SRPG sequencing
• Zero-area overhead state save and restore functionality re-using manufacturing scan
• State-retention register integrity analysis hardware checking
• Novel power gates, retention registers and isolation buffer cell designs
• Advanced 65nm TSMC ‘LP’ technology demonstrator to allow both leakage plus dynamic voltage scaling support for early customer evaluation of dynamic and static energy management techniques and relative benefits

Physical IP for Low Power Design
Chapter 5 includes the primary novel IP developed during the project

• Library IP support for DVFS – level shifters with integrated isolation clamps
• Library IP support for (MTCMOS) Power Gating – in the form of switches with integrated "always-on" control buffering
• Library IP characterization for Power Gating – de-rated for power gating IR-drop in order to facilitate timing closure when there are "standard cell" power gates in series with power rails
• Library IP support for State Retention – in particular for a novel design of scan-flop that reuses existing ports to control retention, in this case supports a standard design flow with the only requirement that the scan-enable network must be implemented with always-on low-leakage buffer cells
• Library IP support for dynamic well-bias – example worked design with well taps automatically placed within power gating cells
Energy efficient SOC design technology and methodology
Conclusions and Future Work

Evaluation Platforms
The evaluation boards developed as described in Chapter 6 were a major factor in being able to port operating systems (Linux in-house) and bring up measurable/demonstrable systems for detailed energy management and benchmarking. These are summarized as:

- 180nm sARS2 Evaluation Board
- Software Development Board for IEC
- 130nm DVS926 Voltage Scaling Test Platform
- 130nm DVS926 Voltage Scaling Demonstration Platform
- "IEM" Voltage Scaling Exhibition Platform
- 130nm ULTRA926 Voltage Scaling Demonstration Platform
- 65nm ATLAS926 DVS/Leakage Demonstration Platform
- (90nm SALT926 Leakage Test Platform during the writing up phase of this thesis)

Technology Demonstrator Evaluation and Analysis
All the technology demonstrators with the exception of the first (simple!) design were fully functional and together with the evaluation boards allowed dynamic and static power and energy analysis across a number of process technologies and geometries:

- sARS2 180nm “standard” low-power SOC flow [Suffered from a JTAG debug clock balancing fault that meant evaluation was based on Flash-ed EPROM monitor]
- DVS926 130nm Silicon DVFS Evaluation of 240MHz cached CPU
- DVS926 130nm DVFS Energy Savings and co-development of Adaptive Voltage Scaling
- ULTRA926 130nm Silicon Evaluation of 288MHz cached CPU
- ATLAS926-65LP Silicon DVFS and Leakage power/energy Evaluation
  - Analysis of SRPG leakage with virtual rail voltage scaling
  - Analysis of SRPG leakage across commercial temperature ranges

Patents Filed/Granted
A number of inventions have been patented from the dynamic and static energy management projects, of which 6 are public in that they are granted or have confirmation of grant notices, as described in Chapter 8:

- US 6,883,102 Power Management Control API
- US 6,950,951 RTL Power Control Interface
- US 2004/0153762 Bus Based State Save and Restore
- US 7,181,633 IEC Performance Available Response
- US 7,194,647 IEC PWM Dynamic Performance Scaling
- US 7,154,317 StateSaver Retention Register
Energy efficient SOC design technology and methodology
Publications and Conferences
For commercial reasons publications and papers have been limited. A number of the early engagements were under confidential arrangements with ARM partners, and some of the detailed technical work was held back while proceed with patent filing. Chapter 9 provides details of the conferences and articles that were public, many of which were invited as the work began to show credible results and working technology demonstrators were exhibited:

- Chapter for "Closing the Gap between Custom and ASIC", 2002
- Canadian Microelectronics Corp Keynote, Banff 2002
- Microprocessor Reports DVS/AVS Article, Jan 2003
- DesignCon 2003, SA2-3 Hardware/Software paper/presentation
- HotChips 2003, Intelligent Energy Management with ARM926
- EE-Times Jan 2004, Design and Evaluation of power-efficient SOCs
- DATE 2004, Energy Efficient SOC with Dynamic Voltage Scaling
- IEE/ACM Colloquium, SOC Design Test & Technology, Sep 2004
- Synopsys EDA Interoperability Conference, Oct 2004
- DAC 2005 All-day Low Power Tutorial - DVFS and Leakage
- ARM Developers Conference, Leakage Control, Oct 2005
- DAC 2006 Leakage Technology Demonstrators (TSMC & UMC)
- Primary author for "Low Power Methodology Manual", Springer 2007

Research contributions to knowledge and Industrial application
The identifiable contributions of the research can best be summarized as:

- An approach to RTL design for Multi-Voltage implementation where Isolation, Reset, Clocking, Retention and Test semantics are overlaid on a Power Domain and can be described in conventional synthesizable HDL coded design. This has proven to work well for a series of technology demonstrators and is shaping the future of how ARM can verify and deliver multi-voltage CPU designs and next generation designs with partial retention
- Novel system level interfaces and hardware abstractions for dynamic performance scaling appropriate to third-party voltage scaling technology
- Novel retention schemes and retention register designs with minimal implementation requirements in the form of control sequencing
- Software-transparent retention mechanisms demonstrable with both retention register designs (fast wake, higher area cost) and scan-based state save and restore (higher energy cost retention and wake-up latency at zero-area cost)

The approach by Springer to author the primary content for the "Low Power Methodology Manual" will hopefully enable a number of these techniques to become main-stream in the industry, and underpin much of the power format standardization work that the EDA companies are actively engaged in as the thesis is completed.
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Conclusions and Future Work

Future Work

Testability of power gating in production is an issue for high-volume customers. At-speed test techniques can be used to test for delay "hot-spots" where broken power gates result in excessive IR voltage drop. However, for battery-powered products, mal-formed switches that do not turn off would definitely cause standby life problems. Traditional leakage current tests are no longer able to discriminate accurately such failures on a tester due to the variation in die-to-die leakage.

- Research and develop on-chip sensing mechanisms to provide Built-In-Self-Test facilities for power gating designs.

Address the reliability of power gating transistors. A number of advanced customers have begun to express concern about the potential stress mechanisms on power gates.

- Research the reliability issues for the "header" and "footer" switch transistors to understand and develop techniques and mechanisms to mitigate against switch wear-out.

Fault tolerance to cope with errors at low voltage.

- Apply and extend the techniques developed in this thesis to "Razor" [14] collaboration research between ARM Ltd and the University of Michigan.

Silicon-on-Insulator (SOI). SOI is a specialized and currently expensive technology that has been optimized for higher performance than traditional bulk CMOS. As a result, SOI has a significant static leakage power problem that will affect standby battery life.

- Following on from ARM Ltd's acquisition of an SOI library business to develop optimized power gating and retention physical IP along the lines of the Power Management Kit components developed for bulk CMOS.

References

[12] DVS926 at PATMOS03 http://www2.polito.it/ricerca/eds/patmos03/Slides/Artun.pdf
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Appendix A. perl script for RTL emulation of SRPG

Chapter 4 introduced the concept of post-processing synthesizable RTL to emulate the behaviour of both power gating and state retention control for simulation. A technique was jointly developed with Mike Keating at Synopsys to parse and annotate RTL as described in chapter 4. This chapter documents the author’s script developed for RTL designed for the SALT926 project for use with the single-pin NRETAI N controlled retention register IP.
#!/usr/bin/perl
use strict;

# File: conv_retl_flop.pl
# Purpose: To make each register in the input Verilog file have an additional retention register
# Note: This script can't handle memory array
# Usage: % conv_retl_flop.pl file1.v file2.v file3.v
# --> ret_file1.v, ret_file2.v, ret_file3.v
# Writer: dflynn based on an original by trihn

#--These variables are for customizing the generated output file-----
my $sim_flag = "RTL_PG_EMULATE";
my $nretain = "NRET";
my $power = "PWR";
my $postfix = "_RET"; # postfix for retention registers
my $ret_file = "ret_" # prefix for the new output file

# global vars
my @ff = ();
my %signal_size = (); # store all signals (type reg or integer) and their sizes
my $local_signals = ""
my $if_block = "";  # if block that resets register
my $count = 0;  # count line number
my $tmp = "";
my @arrayl = ();
my $size = "";
my $always = "";
my $new_always = "";
my $line = "";
my $file = "";

# regexpr for terms in verilog
my $s = "(\\s|\\t)*";  # space, tab, endline
my $id = "(\\w)*";  # my $range = "(\\[[s$id$s]\]) | (\\[[s$id$s \: s$id$s]\])";
my $range = "(\\[[+.]\]) | (\\[+.\:+.\])";
my $var = "s$id$s($range)";
my $concat = "(\{$var$s ( $s $var$s).\})";
my $term = "(\$var) | ($concat)";
my $local_declaration = "(integer\|reg) ($range)? $s $term ($s , $term) ;";

foreach $file (@ARGV) {
    &add_retention_register ( $file);
}

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sub add_retention_register {
    open INFILE, "@_[0];
    open OUTFILE, ">$ret_file" ."@_[0];
    #reset all of the variables
    @ff = ();
    %signal_size = ();
    $local_signals = ""
    $if_block = ""
    $count = 0;
    $tmp = ""
    @array1 = ();
    $size = ""
    $always = ""
    $line = ""

    while ($line = <INFILE>) {
        $count++;
        #Insert 3 new input ports
        if ($line =-/ (module) $s ($term) $s \(//x) {
            $tmp = $line;
            $line =- s/(module) $s ($term) $s \(//x;
            print "$3 \n";

            print OUTFILE "\n`ifdef $sim_flag\n";
            print OUTFILE "module $3 (";
            print OUTFILE "$power, $nretain, \n";
            print OUTFILE "`else\n";
            print OUTFILE "$tmp";
            print OUTFILE "`endif\n";
            while ( not ($line =-/ \\s ; Ix) ) {
                $line = <INFILE>;
                $count++;
                print OUTFILE "$line";

                #-------try to handle v2k port declaration here--------
                if ($line =-/ (output) $s
                    (reg) $s
                    ($range)? $s
                    ($term) $s
                    ./x) {
                    $line =- s/'Ss
                    (output) Ss (reg) \\
                    )/; #remove reg or integer from the string
                    $line =- s/([^().]//; #remove everything after the ','
                    if ( $line =- s/\[\[.]+\]//) { $size = $&; } #remove the range
                    else { $size = "";}
                    @array1 = split(/,/, $line);
                    for($tmp = 0; $tmp < scalar(@array1); $tmp++) {
                        $array1[$tmp] = s/$s//g; #remove space, tab, ...
                        $signal_size{ $array1[$tmp] } = $size;
                    }
                }
                #-------------------------------------------------------------------
                print OUTFILE "\n`ifdef $sim_flag\n";
                print OUTFILE "input $power, $nretain;\n";
                print OUTFILE "`endif\n";
            }
        }
    }
}
Appendix  Script for RTL emulation of SRPG

#find and store registers' name and registers' sizes
elsif( $line =~ /\$s(reg)\s+$s\(range\)?\s+$s\(term\)\s+($\s+\s*$term\s+)$s\)*\(/x) {
    print OUTFILE "$line";
    $line =~ s/A$s(reg)\s+\(\sl*t\t\l\n\)/,;/;
    if( $line =~ /\$s\(range\)?\s+$s\(term\)\s+($\s+\s*$term\s+)$s\)*\(/x) {
        print OUTFILE "$line";
    }
}

#find reset block
elsif ( $line =~ /\$s(always)\s+$s\(\@\)\s+$s\(\()\s+$s\(\posedge|\negedge\)\s+$s\(\(\term\)\s+($\s+\s*$term\s+)$s\)*\(/x) {
    print OUTFILE ""---$count----
    if( $line =~ /\$s(always)\s+$s\(\@\)\s+$s\(\()\s+$s\(\posedge|\negedge\)\s+$s\(\(\term\)\s+($\s+\s*$term\s+)$s\)*\(/x) {
        print OUTFILE ""---$count----
    }
#Local signal like integer for 'for' loop
if( $line =~ /\$s\(local_declaration\)\s+x\)/x) {
    $local_signals .= $line;
}
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`
else {
    $if_block .= $line;
}

# Find the end of the reset block (it is ended with "else" or "end")
while (not ($line =~ /(\s|\r|\n|\t)(else|end)(\s|\r|\n|\t)/)) {
    $count++;
    $line = <INFILE>;

    # Local signal like integer for 'for' loop
    # they need to be placed outside of reset block
    if($line =~ /$/local_declaration/x) {
        $local_signals .= $line;
    } else {
        $if_block .= $line;
    }
}

# Find non-blocking assignment in reset block
while ($if_block =~ /$term/ $s
    (<=) $s
    (\.)+$ $s
    (/)/xg) {
    push @ff, $1;
}

print OUTFILE "-ifdef $sim_flag
"$tmp = &process_reset($ff);
print OUTFILE "-endif
";

print OUTFILE "-ifdef $sim_flag
"print OUTFILE "$new_always"
print OUTFILE "$alwaysn" else
print OUTFILE "$alwaysn" endif
print OUTFILE "$local_signals
"print OUTFILE "$sim_flag
"while ((<$k, $v>) = each %signal_size) {
    print "$k ----------->$v
";
}

close INFILE;
close OUTFILE;

# For debugging
my $k = "";
my $v = "";
while ((<$k, $v>) = each %signal_size) {
    print "$k "
    print "$v
";
}
# This procedure takes an array of ff and add power up/down, retain
# conditions for those signals
sub process_reset {
    my @ff_list = ();
    my $tmp = "";
    my @tmp_array = ();
    my $ret_ff = "";
    my $str = "";
    my $bare_name = "";

    foreach $tmp (@_) {
        if ( $tmp =~ /$concat/x ) {
            #if $tmp is a concat of signals { x, y , z , ...
            #then it is splitted into individual signals
            @tmp_array = split(/,|\{|\}|\/, $tmp);
            foreach $tmp (@tmp_array) {
                $tmp =~ s/$s//g;
                if( $tmp ne "") {
                    push @ff_list, $tmp;
                } else {
                    $tmp =~ s/$a//g;
                    push @ff_list, $tmp;
                }
            }
            #create some shadow ff for each ff
            foreach $tmp (@ff_list) {
                if ($tmp =~ /(.+) ($range)/x) {
                    $ret_ff = $1 . "$postfix";
                    $bare_name = $1;
                    #$tmp =~ s/\[(.*)\]//; #remove the range from the signal name
                } else {
                    $ret_ff = $tmp . "$postfix";
                    $bare_name = $tmp;
                }
                if($signal_size{$bare_name} ne "already_declared") {
                    print OUTFILE "reg $1 ;
                    print OUTFILE " $signal_size{$bare_name} ";
                    print OUTFILE "$ret_ff;";
                    $signal_size{$bare_name} = "already_declared";
                }
            }
            #generate a SAVE process
            print OUTFILE "always@(negedge $nretain)\n";
            print OUTFILE "begin\n";
            foreach $tmp (@ff_list) {
                if ($tmp =~ /(.+) ($range)/x) {
                    $ret_ff = $1 . "$postfix";
                    $bare_name = $1;
                    #$tmp =~ s/\[(.*)\]//; #remove the range from the signal name
                } else {
                    $tmp =~ s/$a//g;
                }
            }
        }
    }
}

Appendix: Script for RTL emulation of SRPG

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$ret_ff = $tmp . "$postfix";
$bare_name = $tmp;
}
print OUTFILE = " ";
print OUTFILE = $ret_ff <= $bare_name;\n"

} 
print OUTFILE "end \n";

$str = "if (I$power) begin\n";
foreach $tmp (@ff_list) {
    $str . = " $tmp <= 32'bx;\n";
}
$str . = "end\n";
$str . = "else if (I$retain) begin \n";
foreach $tmp (@ff_list) {
    if ($tmp == /\$\d+/($range)/) {
        $ret_ff = $1 . "$postfix" . "$2";
    } else {
        $ret_ff = $tmp . "$postfix";
    }
    $str . = "$tmp <= $ret_ff;\n";
}
$str . = "end else\n";
return $str;
}
Appendix: Script for RTL emulation of SRPG
Appendix B. External non-confidential publications

**DVS926 130nm project and Adaptive Voltage Scaling**

DesignCon 2003 ................................................................. B-3
   ARM / National Semiconductor joint paper
Microprocessor Reports Jan 2003 ........ ... .................................. B-21
   ARM material authored for Max Baron article
Hot Chips 2003 (presentation) ........ ........................................... B-27
   Intelligent Energy Manager DVFS presentation
Design Automation and Test in Europe, DATE 2004 ......................... B-39
   DVFS results published with measured energy savings

**ULTRA926 130nm project and DVFS Methodology**

San Jose Synopsys Users Conference 2005 panel (presentation) .......... B-43
   Joint project disclosed
Synopsys Advanced Technology Group (invited presentation) ....... ... B-47
   Guest presentation at a 45nm off-site meeting
Design Automation Conference DAC 2005 low power tutorial (presentation) B-63
   Design for DVFS (morning) tutorial
Design Automation Conference DAC 2005 low power tutorial (presentation) B-79
   Design for Leakage (afternoon) tutorial
Design Automation Conference DAC 2005 low power panel (presentation) B-87
   Joint ARM/Synopsys/UMC panel announcing collaboration progress
European Synopsys Users Group, ESNUG 2005 ............................... B-93
   Joint paper with Synopsys and UMC on ULTRA926 implementation

**ATLAS926 65nm LP project and Leakage Mitigation**

Design Automation Conference, DAC 2006 low power panel (presentation) B-115
   Joint ARM/Synopsys/TSMC panel, ATLAS project announcement

**Leakage Mitigation and early SALT926 90nm disclosures**

ARM Designers Conference 2006 ARM/Synopsys (presentation) .......... B-119
   Joint ARM/Synopsys announcement of joint leakage R&D project
Boston Synopsys Users Group 2005 (ARM contributor)....................... B-141
   Joint author for ARM/Synopsys presentation on SALT implementation
Appendix B: External non-confidential publications
A Combined Hardware-Software Approach for Low-Power SoCs: Applying Adaptive Voltage Scaling and Intelligent Energy Management Software

Krisztián Flautner
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Mark Rives
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Abstract

Increased functionality and performance demands are challenging System-on-Chip (SoC) designers to seek better methods for optimizing available battery power in portable applications. Key areas of exploration include dynamic voltage scaling and improved software algorithms for the control of power modes. Dynamic voltage scaling can be improved by adaptively monitoring hardware performance to minimize the applied supply voltage for any given clock frequency. While adaptive voltage scaling optimizes power use based on temporal environmental conditions, Intelligent Energy Management (IEM) algorithms optimize power consumption based on the dynamic workload of the processor. IEM software and hardware monitor the execution and communication characteristics of workloads and predictively set the performance of the processor to the level that minimizes energy use, while still meeting application deadlines. The combined use of adaptive voltage scaling and IEM provides the optimum trade-off between performance and battery life for portable devices.

Authors' Biography

Krisztian Flautner, Principal Research Engineer, ARM, holds a Ph D degree in Computer Science and Engineering from the University of Michigan. His thesis explored the relevance of multithreading for interactive desktop workloads and described the implementation of an automatic power-management algorithm for processors supporting dynamic voltage scaling. Dr. Flautner's research interests are focused on simple ideas that enable high-performance low-power computers to support advanced software environments. In the research group at ARM Limited, he is currently working on the next generation ARM architecture.

David Flynn has been with ARM for 11 years and is a Fellow in the Research and Development group based in Cambridge, UK, specializing in System-on-Chip IP deployment and methodology. He is the original architect behind ARM's synthesizable CPU family and the AMBA on-chip interconnect standard. His current research focus is low-energy system-level design. He holds a number of patents in on-chip bus, low power and embedded processing sub-system design (8 US, 21 worldwide) and has a BSc (1st) in Computer Science from Hatfield Polytechnic, UK.

Mark Rives, Principal Applications Engineer, National Semiconductor Corporation, joined National in 1995 where he is responsible for supporting advanced development projects in the Portable Power Group. His previous experience includes the design and support of National's direct IF-sampling Diversity Receiver Chipset in addition to a wide range of both system level and IC design projects from pro audio gear to pacemakers. He received his B.S in Electrical Engineering from Mississippi State University in 1987.
Appendix B  External non-confidential publications

Introduction

Low power consumption is arguably the most important feature of embedded processors, which significantly impacts the cost and physical size of the end device. Even though the processor may not be the most power-hungry component of a system, it is essential to manage processor power in order to reduce overall system power consumption. Better processor power efficiency can increase the available power budget for features such as color screens and backlights, which are growing in popularity on portable devices.

Historically, low power consumption in embedded processors has been achieved through simple designs, limited use of speculation, and employing a number of low-power sleep modes that reduce idle-mode power consumption. Embedded processors are now performing more sophisticated tasks, which require ever-higher performance levels. As a result, new processor designs are more dependent on sophisticated architectural techniques (such as prediction and speculation) to achieve high performance. Unfortunately, such techniques can also significantly increase the processor's power consumption.

Process technology trends are also complicating the power story. Until recently, CMOS transistors consumed negligible amounts of power under static conditions. However, as process geometries shrink to provide increasing speed and density, their static (leakage) power consumption has also increased. Current estimates suggest that static power accounts for about 15%-20% of the total power on chips implemented in 0.13 μm high-speed processes. Moreover, as process technology moves below 0.1 μm, static power consumption is set to increase exponentially, and will soon dominate the total power consumed by the processor.

Figure 1. Normalized leakage power through an inverter

The circuit simulation parameters including threshold voltage were obtained from the Berkeley Predictive Spice Models [1]. The leakage power numbers were obtained by HSPICE simulations.

Figure 1 shows projections for leakage power increase in future process technologies. There is a strong correlation between the operating temperature and the amount of leakage power. However, regardless of the temperature, all lines exhibit exponential trends. In embedded processors, where the majority of transistors are usually dedicated to...
memory structures (such as caches), leakage is a particularly important problem to attack, since the static power consumption of these structures can dominate overall power consumption.

**Power Saving Opportunities**

A way to bridge the gap between high performance and low power is to allow the processor to run at different performance levels depending on the current workload. An MPEG video player, for example, requires about an order of magnitude higher performance than an MP3 audio player. Even greater savings can be achieved by reducing the processor's supply voltage as the clock frequency is reduced. Dynamic Voltage Scaling (DVS) exploits the fact that the peak frequency of a processor implemented in CMOS is proportional to the supply voltage, while the amount of dynamic energy required for a given workload is proportional to the square of the processor's supply voltage [2]. Reducing the supply voltage while slowing the processor's clock frequency yields a quadratic reduction in energy consumption, at the cost of increased run time.

Often, the processor is running too fast. For example, it is pointless from a quality-of-service perspective to decode the 30 frames of a video in half a second, when the software is only required to display those frames during a one second interval. Completing a task before its deadline is an inefficient use of energy [3]. The key to taking advantage of this trade-off is the use of performance-setting algorithms that aim to reduce the processor's performance level (clock frequency) only when it is not critical to meet the application's deadlines. Figure 2 illustrates a significantly lower total energy consumption using dynamic voltage scaling compared with traditional gated-clock power
management, for the same workload. Note that with DVS, the lower supply voltage reduces static power even when the clock is gated off.

Static leakage power can also be substantially reduced if the processor does not always have to operate at its peak performance level. One technique for accomplishing this is adaptive reverse body biasing (ABB). Combined with dynamic voltage scaling, this can yield substantial reductions in both leakage and dynamic power consumption [4]. The key enabler for controlling both DVS and ABB is knowledge about how fast a given workload needs to run. This information can be provided by performance-setting algorithms that take various operating system and optional application-specific information into account to provide an estimate for the necessary performance level of the processor.

Just as performance-setting algorithms optimize power consumption based on workload variations, significant power efficiency can also be gained if the processor does not have to operate under worst-case assumptions but can tune its operating parameters to temporal environmental conditions [5]. Processors are designed to operate reliably over a wide range of temperature levels and variations of the silicon substrate. Increased voltage levels must be used to assure the large safe-operating range at the cost of reduced power efficiency. By monitoring the margin between expected and actual operating conditions, the voltage level of the processor can be reduced without sacrificing operational stability. This closed-loop monitoring of system margin will be referred to as adaptive voltage scaling (AVS).

While DVS, AVS, and ABB are effective ways of managing the processor's power consumption, integrating these ideas into SoC designs has proven to be a significant challenge. The key issue is that not all parts of the SoC can be scaled in equal measure. Consequently, multiple voltage and frequency domains with asynchronous interfaces are required. Moreover, these extra parameters complicate testing and validation processes and require special support from synthesis tools.
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System-on-Chip Implementation

Figure 3 depicts the system architecture required to implement the systemic power reduction schemes in a SoC design combining Intelligent Energy Management (IEM) with Adaptive Power Control (APC). The IEM interfaces with the CPU through the AMBA Peripheral Bus allowing it to be easily added to any ARM-based SoC design.

![Diagram of IEM + AVS Architecture]

The IEM software and hardware monitor the system workload to generate a performance request. The APC can then set the correct operating voltage in either open-loop or closed-loop mode without processor intervention. The APC will transparently provide the fastest possible response while assuring that the processor will always receive the minimum safe operating voltage for any given clock frequency. The APC would also coordinate all clock switching including the verification of stable supply voltage. The IEM provides a uniform software interface to simplify implementation and reuse. The APC provides an open-standard interface to the external power supply.

ARM Limited and National Semiconductor Corporation have agreed to work together to offer synthesizable intellectual property (IP) to implement the IEM and AVS functionality for SoC designers. Work is underway to assure support from both design tool vendors and operating system vendors to allow SoC designers to implement this power saving technology transparently. The following sections provide more detail on the key components of the solution.

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Intelligent Energy Management

Completing a task before its deadline, and then idling, is significantly less energy efficient than running the task more slowly so that the deadline is met exactly. The goal is to reduce the performance level of the processor without allowing applications to miss their deadlines. The central issue is how the right level of performance can be predicted for the application.

The Intelligent Energy Management (IEM) framework provides a hardware and software mechanism for achieving these goals: it standardizes the interface for setting the processor’s performance level, specifies counters for measuring the amount of work that is being accomplished, and includes operating system and application-level algorithms for predicting future behavior.

The IEM software layer has the ability to combine the results of multiple algorithms and arrive at a single global decision. The policy stack illustrated in Figure 4 supports multiple independent performance-setting policies in a unified manner. The primary reason for having multiple policies is to allow the specialization of performance-setting algorithms to specific situations, instead of having to make a single algorithm perform well under all conditions. The policy stack keeps track of commands and performance-level requests from each policy and uses this information to combine them into a single global performance-level decision when needed.

The different policies are not aware of their positions in the hierarchy and can base their performance decisions on any event in the system. When a policy requests a performance level, it submits a command along with its desired performance to the policy stack. The command specifies how the requested performance should be combined with requests from lower levels on the stack: it can specify to ignore (IGNORE) the request at the current level, to force (SET) a performance level without regard to any requests from below, or set a performance level only if the request is greater than anything below.
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(SET_JFGT) When a new performance level request arrives, then the commands on the stack are evaluated bottom-up to compute the new global performance level. In Figure 4, the evaluation would yield the following: at level 0 the global prediction is set to 25; at level 1 it remains at 25, and level 2 changes the prediction to 80.

Using this system, performance requests can be submitted any time and a new result computed without explicitly having to invoke all the performance-setting policies. While policies can be triggered by any event in the system and they may submit a new performance request at any time, there are sets of common events of interest to all. On these events, instead of recomputing the global performance level each time a policy modifies its request, the performance level is computed only once after all interested policies' event handlers have been invoked. Currently the set of common events are reset, task switch, task create, and performance change. The performance change event is a notification which is sent to each policy and does not usually cause any changes to the performance requests on the stack.

There are significant benefits in using multiple performance-setting policies, each optimized for a particular situation, instead of a single one that needs to be optimal under all circumstances. Figure 5 provides some qualitative insight into the characteristics of the IEM algorithm vs LongRun, a conventional algorithm implemented in the Crusoe processor's firmware. The biggest difference between the two algorithms is that while LongRun keeps on ramping the performance level up and down in fast succession, the IEM algorithm stays close to a target performance level.
To achieve the most effective energy reduction with minimal intrusion, application monitoring and performance-setting decisions need operating system involvement.

Figure 5. Performance-setting during MPEG video playback of Red's Nightmare
Figure 6 illustrates the fraction of time spent at each of the processor’s four performance levels (300, 400, 500, and 600 MHz) using the Crusoe’s built-in LongRun power manager, contrasted with IEM during playbacks of two MPEG movies. The data for both algorithms were collected on the same hardware. However, during the IEM measurements, the built-in LongRun power manager was disabled. While the playback quality of the different runs was identical, it can be seen that IEM spends significantly more time below peak performance than LongRun. During the first movie, IEM switches mostly between two performance levels. The machine’s minimum 300 MHz and 400 MHz clock frequencies are sufficient for the first movie, while during the second, it settles on the processor’s third performance level at 500 MHz. LongRun, on the other hand, chooses the machine’s peak performance setting for the dominant portion of execution time during both movies.
Voltage Scaling Methods and Benefits

Currently, proprietary dynamic voltage scaling (DVS) solutions offer improved performance by reducing the supply voltage as the clock frequency is reduced. Open-loop DVS, as shown in Figure 7, allows the processor to set the supply voltage based on a table of frequency/voltage pairs. This table must be determined by characterization to assure sufficient margin for all operating conditions and process corners.

In operation, the processor must determine the desired operating frequency, request a new voltage, wait for the voltage to stabilize, and then switch itself to the new frequency. The switch may be made immediately when changing from a higher frequency to a lower frequency. When switching from a lower frequency to a higher frequency, the power supply voltage must be high enough to support the new frequency prior to changing the clock. Power supply stability can be assured either by a time delay or by an analog measurement. Use of a time delay is risky, since there will always be a desire to implement the minimum possible delay for enhanced processor response time.

Open-loop operation can be simplified by creating an Adaptive Power Controller (APC) module to off-load the voltage scaling and clock management from the processor. The APC approach supports a common software API allowing the DVS function to be easily accessed by applications or the operating system. Providing a standard interface to the external power supply also simplifies system design and facilitates second-source options for the power supply component. An architecture using an APC is shown in Figure 8.
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Closed-loop or Adaptive Voltage Scaling (AVS) is a new approach, which offers improved performance and ease of implementation compared to open-loop DVS. In the closed-loop system shown in Figure 9, the voltage is set automatically by monitoring the system's performance margin and adjusting the supply voltage adaptively.

Since the system is closed-loop in nature, a much finer degree of control over the voltage is possible when compared to the discrete table values in an open-loop system. Response time of the AVS system can be much faster, since it is limited only by the external power supply. The performance measuring circuitry can be used to verify the power supply stability to offer the fastest possible switching from one clock frequency to the next.
Closed-loop operation also offers improved power savings since the operating voltage margin may be reduced due to the continuous voltage updates. Any temperature effects are inherently compensated by the necessary change in supply voltage. This allows the AVS-equipped SoC to be operated at a lower voltage at room temperature since the voltage will be increased automatically as the temperature increases.

For example, in a 1.8V system with +/-5% tolerance, the system must operate at 85°C and 1.71V. For a 200mA load, this equates to 342mW. Even though the system will operate at a lower voltage at 25°C (say 1.5V), normally at least 1.71V must be provided to assure 85°C operation. With closed-loop AVS, the system can be run on 1.5V at 25°C with no problems since the AVS technology will increase the voltage if necessary. This allows a 25°C power of 300mW, a saving of 42mW or 14%, even at the maximum clock frequency.

Figure 10 shows measured data for a closed-loop AVS system running at 32MHz, 16MHz, 8MHz, and 4MHz. The plot shows voltage vs. time where the highest voltage is associated with 32MHz operation. The three traces show how the closed-loop AVS voltage is automatically adjusted with changing temperature.

![Graph showing AVS voltage vs. Temperature](image)

**Figure 10. AVS Voltage vs. Temperature**

Figure 11 compares the power used by a system with a fixed 3.3V supply with the power used with AVS. The effect of reduced margin at 25°C can be seen in reduced power, even at the highest clock frequency.
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Figure 11. Power Reduction with AVS

Figure 12 shows the percentage of power used by the AVS system relative to that used by the fixed 3.3V system. As the clock frequency is decreased, the power savings provided by AVS can increase to 80% or more when using a switching regulator for the power supply.

Figure 12. Relative Power Usage of AVS vs. a 3.3V Fixed Supply
SoC Design Flow Issues

Until now, dynamic voltage scaling has only been commercially exploited in stand-alone CPU integrated circuits. To support voltage scaling of processing sub-systems within a system-on-chip design requires enhancements to both EDA tools and design methodology. Key issues include:

- Multiple physical power domains
- Synchronous clock relationships across boundaries
- Standard-cell library and RAM compiler design views
- Static timing verification
- Manufacturing test

Multiple power domains require careful handling at interfaces where some form of analog level-shifting is required between different voltages. Also, many EDA tools treat voltage rails as special global resources which are implicitly connected, which makes separating voltage domains a manually intensive design step.

Best-practice SoC design flows typically assume synchronous clocking relationships between sub-systems in order to allow top-level static timing-closure and analysis, automatic test structure insertion and test pattern generation. Ideally, multiple voltage domains should be treated as asynchronous because the tolerancing of buffered clocks across the top-level system becomes near-impossible where sub-systems can have variable voltage with respect to each other. Different sub-systems have inherently variable clock buffer latencies.

Cell libraries and memory compilers are normally characterized and modeled for a process and temperature range acrossa tightly tolerated (+/- 5% to +/- 10%) supply voltage. To ensure design integrity with voltage scaling, more comprehensive timing models are required. The design tools make this harder because in order to design for multiple performance levels, the target sub-system frequency must first be specified. Then, the power supply requirements must be determined to provide sufficient voltage to maintain operation, either statically or adaptively. However, from a design-flow perspective, it is necessary to work the other way around: start with a defined voltage and then calculate the achievable performance from the static timing analysis at this precise voltage. Characterizing RAMs at low voltage is complicated by the fact that sense amplifier performance degrades non-linearly with respect to logic gate speeds.

Verification of static timing and functional test are complicated with voltage scaling of parts of the SoC design. The EDA tools need to be guided.
Energy efficient SOC design technology and methodology

Implications for Front-end Design

Front-end design tools typically read in RTL descriptions in Verilog or VHDL of the hardware design, for both simulation and synthesis. Such HDL descriptions have no concept of multiple power rails, a global view of power and ground are assumed. Similarly, clocks and resets are treated as ideal signals in the HDL. These are later buffered as carefully balanced high-fanout buffer-tree networks.

The boundaries between voltage domains must be handled with detailed management of hierarchy and the instantiation of explicit voltage level-shifter cells between different voltage rails. The onus is on the designer to carefully abstract out the top-level management of clocks, resets, test scan chains and power management such that individual sub-systems can be synthesized and even hardened independently using standard ASIC design flows.

Implication for Back-end Design

The layout tools need to understand separate voltage rails and this may require manual intervention and careful inspection and review of conversion from the front-end logical design flow to the place and route implementation phase.

In the worst-case, the cell library may need to be replicated with special cell and power-rail naming schemes to ensure that optimization, setup and hold timing fixes applied to the post-routed top-level design do not accidentally stray over voltage domains or level-shifter boundaries.

Design verification needs to be extended beyond standard ASIC design flows to cover the extra complication of analog level-shifter integrity. This is especially relevant to power domains that can be powered off completely. These must not draw static currents from driven inputs, and need outputs clamped during power down and power up (i.e., operating outside valid logic state operation).

An ARM926EJ-S based design with independent voltage scaling of the cached CPU, which tackles all these design tool issues is scheduled for fabrication in February 2003.

Conclusions

The ARM Intelligent Energy Manager (IEM) provides continuous predictive monitoring of the CPU workload. It attempts to run the clock frequency at the lowest available value while still completing the work prior to its deadline. The correct performance level is set by predictive algorithms that are embedded in the operating system kernel to monitor all processes.
Appendix B  External non-confidential publications

National Semiconductor Corporation’s AVS technology accepts the IEM’s performance request and sets the lowest possible operating voltage for any resulting clock frequency. Sufficient margin is always present to assure proper operation. Since National’s hardware performance monitor is always adjusting the voltage for sufficient margin at any given clock frequency, the effects of process and temperature variation are inherently corrected. If the temperature rises, the margin will decrease and the voltage will be increased to compensate.

The combination of these two technologies will provide optimum power savings for embedded processors in portable systems.

The proposed dynamic voltage scaling system also forms the basis for techniques that address a chip’s static (leakage) power consumption. Some of our initial investigations are described in [4].

References

Energy efficient SOC design technology and methodology
Memory speed is no longer guilty of limiting processor performance. The infamous title has been awarded to battery capacity. Cellular telephones, PDAs, notebooks, and portable multimedia devices could bring higher microprocessor revenues and more rewarding improvements in performance and functions—if only batteries could be made to last longer. Increases in battery capacity are still creeping along the roadmap—a line of progress that, if plotted, would look almost horizontal compared with one charting the evolution of microprocessors. Until a small, practical fuel cell or similar miracle comes along, microprocessor developers must come up with power-reduction methods.

Answering the call to arms National Semiconductor Corp. and ARM announced, in November 2002, a strategic business relationship to jointly develop and market power-efficient systems that, they claim, will increase the battery life of handheld portable devices in several stages—from 25% to as much as 400%. The two companies' joint effort will leverage ARM's penetration in the mobile phone market and National Semiconductor's expertise in analog design and power management.

The overall handset market—including mobile phones, smart phones, and handheld devices—is expected to grow to more than 525 million devices by 2006, an increase of 31% from 2002 according to market researcher In-Stat/MDR.

Power Management Beyond Clock Gating

Faced with the need to find sockets in portable-device markets, microprocessor and ASSP vendors have used clock gating to temporarily turn off unneeded peripherals, blocks of on-chip memory, and, during idle periods, even the processor itself. ARM and NSC propose to obtain further power reductions by intelligent control of frequency, supply voltage, and leakage current.

Combined control of frequency and voltage can reduce both power and energy requirements. Frequency reduction alone contributes linear savings in power but does not, by itself, reduce the amount of energy required to complete a task. Reducing frequency is justified, however, whenever a task's early completion will not improve perceived performance or, because of dependencies on other tasks, will even yield incorrect results. Lower frequencies can be supported by lower voltage levels, which have a quadratic effect on reducing power requirements and contribute to lowering energy consumption. In most current schemes that use frequency-voltage power reduction, the voltage is delivered in open-loop mode, sans feedback from chip internals.

Companies such as AMD, Intel, and Transmeta have obtained good results using this type of frequency-voltage management in addition to clock gating. Intel has used the approach in its PXA250 chip, which can be switched through several frequencies and voltages, depending on workload and peripheral activity. For IA-32 chips, Intel uses its SpeedStep.
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technology, which establishes two frequency-voltage points to save battery power. For its Crusoe chip, Transmeta has introduced LongRun, a table-based set of multiple frequency-voltage points that helps Crusoe track workloads more efficiently than by using a few steps AMD, with Power Now, uses an approach that is similar to Transmeta's.

As always, a few problems must be overcome. Accurate frequency points can be obtained by reference to a system clock, and good power supplies can provide reliably accurate voltage. Nevertheless, operating frequency must be guarded and ensured by using a few steps AMD, with Power Now, uses an approach that is similar to Transmeta's.

To avoid misinterpretation, MPR will define chip areas under the control of one clock frequency as "frequency domains" and will similarly define "voltage domains" as areas supplied with a common voltage. A "power domain" is one whose power can be turned off to minimize a system on chip's leakage current. Chip areas can belong to one or more domains.

The Hardware-Software, Mixed-Signal Solution
NSC and ARM's joint project aims to create circuits, software, and tools that address three energy-consumption tasks. First, the seemingly trivial problem of matching frequency to workload must be solved. Second, the approach must determine the absolute minimum supply voltage needed over process and temperature variations to generate reduced-width voltage guard bands. Third, the end result must support creation of power domains used to minimize leakage current.

Figure 1 shows a conceptual block diagram of power management by matching frequency and voltage to workloads. The first product, based on NSC's PowerWise technology, targets embedded SoC devices in mobile phones. The power-reduction architecture uses an ARM-designed Intelligent Energy Management (IEM) block that combines software and hardware to monitor the system workload and generate appropriate performance/frequency requests. The IEM interfaces with the CPU through the AMBA peripheral bus, allowing it to be added to AMBA-based SoC designs.

Using a performance request from the IEM, an Adaptive Power Controller (APC) can set the correct operating voltage in either open-loop or closed-loop mode and, in its turn, interface with the clock-management unit to enable transitions to new frequencies.

The APC receives commands from the Hardware Performance Monitor (HPM) when new, higher frequencies can be deployed and enables the new clock frequencies on the CPU core and, if applicable, on on-chip cache, memory, and peripherals. The HPM can require new voltage levels and fine-tune them by communicating to the external power supply and its PowerWise-compliant power-management chips. The HPM is implemented as an on-chip, 3,000-gate microcell, but little else is known about its internals, which NSC is keeping confidential. Nevertheless, enough background on this topic is publicly available to let us fill in some of the likely principles of operation and the components that may be used to implement them.

Can You Hear Me Now?
The problem of defining a minimal guard band for voltage can be stated in a few words: Ensure that voltage levels support frequencies across the core. But efficient solutions can become very sophisticated.

The simplest solution is to deliver open-loop voltage levels that are high enough to ensure across-the-chip operation at every frequency—essentially, the open-loop solution used today. A turner can replace the HPM to enforce a delay from a new voltage-level requirement to stable conditions that can support a higher frequency. This rather primitive solution will reduce consumed energy compared with the absence of voltage control, but it will be inferior to results obtained by feedback from the powered circuits to the power supply.

An improved approach based on local sensing of voltage in one or more spots and analog feedback to the power supply may sound attractive. The sensor and its analog output will be subject to high-frequency interference from surrounding digital circuits. It may not function at all, since low core voltages will require feedback accuracy in the millivolt range.

A feedback that is easier to implement could measure local propagation delays to determine when local voltage is

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Figure 1 Frequency-voltage power-management block diagram shows policy using ARM's Intelligent Energy Management (IEM) unit and the Adaptive Power Controller (APC) and Hardware Performance Monitor (HPM) that help reduce voltage guard bands.
Appendix B External non-confidential publications

Analog and CPU Wizards Reduce Digital Power

Policies can be recorded by tracing the execution of workloads and thus appear to be automatic, they can also be demanded by programmers of applications and by system processes. The final decision-maker must be the operating system. ARM has very wisely refrained from introducing as architecture extensions any of the counters/timers it uses for performance monitoring. At this time (January 2003), for general-purpose computing, the policy features are good beta- (if not alpha-) level starting points, since the industry still has much to learn about power-management policy-setting algorithms. Right now, however, cellular telephones with fewer applications and with known system processes may be a good fit.

Power Domains Reduce Leakage Current

The best way to reduce leakage current is to turn off the power supply, and that's exactly the idea behind an architecture that uses power domains. SoC blocks that are not being used can be turned off under operating-system control. The implementation of power domains is similar to hot-swapping boards and requires special on-chip interfaces.

Figure 3 shows an example of a typical SoC using power domains to control an ARM926E core's leakage current. The design defines the ARM core and its cache RAMs as a power domain that can also be a voltage domain. A tightly coupled memory with state retention (TCMS) must be used to restore processor state upon power-up, following a period during which the processor's power was turned off.

TCMS must belong to a different power domain, it can be maintained at a lower level of voltage—enough to keep the data intact while the core is turned off in its suspend mode. The TCMS, however, belongs to the same voltage domain as the ARM926E to enable, when required, correct operation with the core at frequency and voltage. A logic-level clamp between the core and TCMS ensures correct operation during power up and power down. Logic-level clamps are also used to avoid driving large currents into the core as it goes down and to minimize the probability of latch-up. One should note that a logic-level clamp is really an AND gate forced into a given state during power transitions, it is not a voltage clamp in the context of linear circuits.

The process of turning off power to the CPU involves saving machine state and placing the CPU in reset mode.

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Figure 2 ARM's Intelligent Energy Management (IEM) conceptual block diagram shows prioritizing policy-stack and policy-event handlers.

<table>
<thead>
<tr>
<th>Policy (performance control) stack</th>
<th>Policy event handlers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 2  SET_IFGT  8D</td>
<td>Common events</td>
</tr>
<tr>
<td>Level 1  IGNORE  0</td>
<td>• On reset</td>
</tr>
<tr>
<td>Level 0  SET  25</td>
<td>• On perf switch</td>
</tr>
</tbody>
</table>

Figure 2 ARM's Intelligent Energy Management (IEM) conceptual block diagram shows prioritizing policy-stack and policy-event handlers.
Clocks that could enable the CPU to read and use incorrect logic levels from TCMS memory are turned off. CPU power-up follows the inverse procedure. With clocks and interfaces enabled, coming out of reset state, the CPU can use a vector that points it to the correct TCMS address, from which it can start restoring its state.

The SoC uses four voltage domains: CPU core and cache RAM; TCMS; on-chip bus and peripherals; and I/O to external logic. Closed-loop adaptive voltage is provided only for the CPU/TCMS domains. This simple approach is justified because most peripherals operate at lower frequencies and voltages, and some peripherals count on frequency stability. I/O voltage levels must be kept within specifications to conform to external voltage standards.

The CPU and TCMS domains are connected to system signals and clocks via level-shift clamps to compensate for voltage changes in different domains. These are different from the logic-level clamps that must be used at boundaries of power domains. In addition to level-shift clamps, connections to the AMBA bus must use retiming interfaces to deal with changing frequencies.

The EFM implements the programmer's model and performs dynamic performance monitoring to assist the policy-stack software. The performance monitor hardware counts cycles received by the CPU to estimate the amount of real work that has been done during the elapsed time. The EFM block also outputs the required performance setting for the target rate of workload execution.

Putting it All in Perspective

The architects at ARM and NSC claim that, on the basis of existing silicon, they expect to see energy savings of 30% for peak workloads and 60% for midrange workloads over energy use in fixed-voltage schemes. Energy savings from reduced guard bands will depend on the particular design but will deliver further gains of 10–15%.

Figure 4 shows ARM's estimate of power distribution for the ARM920T processor, in which instruction and data caches consume 44% of total power. The remaining 56% is split among the integer core, memory management units, bus interface unit, and other essential CPU circuitry. The relationships among CPU, peripherals, and caches may change in the future, to the detriment of the CPU. Higher operating frequencies will exact larger cache RAM and consume more energy. Commercially viable ASSPs already have tens of peripherals on chip.
high enough to support a higher frequency. A ring oscillator suggests itself, its frequency measured between two docks of a known period and sent as digital feedback to the power supply.

National Semiconductor seems to have opted for yet a different approach: while the core is still operating under its previous stable frequency, the next-higher test frequency is sent to the HPM, its results checked again and again. Voltage is increased in steps until the HPM reports that the test frequency yielded a correct result by issuing a vdd_ok signal to the APC.

NSC's choice may yield more information than a ring oscillator does, since, hidden in the HPM, it may have placed bistables, parasitics, and maybe even a hot spot, the better to simulate conditions across a wider area of the chip. The test frequency yields a go/no-go answer. It must be augmented by additional HPM logic that can deliver voltage adjustments as the chip's temperature rises and IR drops change, owing to changing demands in supply current. Feedback to the external power supply is based on a local spot on the chip only and may require several sensors for the tightest voltage performance. Downward frequency shifts are less problematic, since the lower frequencies are supported by higher voltages.

The combined function of IEM, HPM, and APC circumvents differences in process, fabrication, and environmental condition; providers of synthesizable microprocessors will use it to advantage. The closed-loop adaptive-voltage feature can also improve upon the results obtained by fully integrated semiconductor houses.

**Policies, Policies, Who Set the Policies?**

Having selected NSC's adaptive voltage scaling (AVS) architecture and ARM's IEM, one must next be concerned with selecting and applying the appropriate frequency for each workload. The architects at ARM have introduced a system-architecture stack that provides hardware/software support for the IEM. The IEM comprises a set of counters, timers, and other undisclosed logic that can be used to monitor the workload and the processor's performance. The IEM also includes operating-system and application-level algorithms for predicting future behavior.

Figure 2 diagrams ARM's concept of the IEM performance-policy stack, most of which is implemented in software. Its purpose is to store multiple algorithms that can best minimize energy consumption for given workload behaviors. The IEM software is intended to examine several algorithms suggested by active workloads and system processes—and generate the best SoC-wide control policy, based on their combined requirements. The approach is general enough to support specialized coprocessors and multiple processors.

IEM policy descriptors contain one field that defines the way they should affect decisions and one that indicates the level of performance that must be delivered. Mnemonic SET is a unilateral request to deliver the associated performance; SET_IFT requires that the associated performance level be delivered only if it is the greatest performance level required by the policies suggested by the active processes.

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Appendix B: External non-confidential publications

Analog and CPU Wizards Reduce Digital Power

![Pie chart showing power distribution in an ARM920T processor](image)

**Figure 4.** ARM920T power distribution shows dominant power consumption attributed to cache RAM and ALU.

A cellular phone may be able to use the technology to affect 40% of its active devices' power. Assuming a 50% average energy reduction using NSC and ARM's short-term product, the overall savings are a significant 20%, considering that turning the devices off completely would improve consumption by only 40%.

**Price & Availability**

The collaboration between National and ARM includes a licensing agreement to enable easy deployment of APC. Under the terms of the agreement, ARM will license National's APC along with its Intelligent Energy Manager to key customers, beginning in 2Q03. National will also market and license its APC. License terms have not been disclosed. For more information please visit [www.nsc.com](http://www.nsc.com) and [www.arm.com](http://www.arm.com).

Closed-loop adaptive voltage is only one component in the project ARM and NSC have undertaken. Clock gating, new cell libraries to minimize leakage current, and power domains to turn it off will further reduce consumed energy.

Microarchitecture control based on workload behavior will play a major role: for example, partitioning cache RAM into power domains can trim active cache size to match active applications, drastically cutting consumption.

Power-efficient technology involves process, physical design, logic, microarchitecture, operating-system and applications software, and, now, analog expertise. ARM and NSC have embarked on an important project. An equally gifted software company should join them.

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HOT Chips 2003

Intelligent Energy Management:
An SoC design based on ARM926EJ-S

Need for Energy Management

- Today's mobile consumers want:
  - longer battery life and
  - smaller, lighter products
- Manufacturers are adding new features and applications to add product appeal:
  - media players (audio, video)
  - gaming
  - video capture

- Increasing processing power requirements and longer battery life are conflicting requirements
- Battery technology alone offers only incremental improvement over the next several years
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**Intelligent Energy Management (IEM)**
- Conserving power whilst running = saving energy
- Running only fast enough to do the work just in time
- Adapting to changing software workloads

- **Conventional On/Off Power Management**
  - Processor Utilization
  - 100% - Energy Used
  - 0% - Energy Used

- **Dynamic Voltage Scaling**
  - 100% - Energy Used
  - 0% - Energy Used

**Dynamic Voltage Scaling (DVS)**
- Voltage is the only parameter that affects all types of power consumption:
  - Dynamic
  - Static leakage
  - Gate oxide leakage

- Intelligent control of DVS designs will bring energy savings
Appendix B: External non-confidential publications

Energy Management System

- IEM and IEC components work together to predict lowest acceptable processor performance level
- Power Controller, PMU and Clock Generator work together to deliver that lowest performance level

IEM: prediction software

- IEM software uses custom hooks in OS kernel to instrument application software activity
- Multiple algorithms determine performance level requirement for different classes of activity
- Best global performance determined dynamically
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IEC: control and monitoring hardware

- Delivers an abstracted view of the power control and delivery components of the device
- Supplies a 0-100% performance level request to the
  - Power Controller and
  - Dynamic Clock Generator
- Plugs into SoC design as a using a standard ARM AMBA compliant interface (APB)
- Provides hardware assist to IEM software
  - Dynamic performance counters
  - Reduces the monitoring software overhead

Adaptive Voltage Scaling (AVS)

- AVS is a closed loop control mechanism
- Feedback from the PMU indicates the earliest opportunity to change processor frequency based on the voltage levels being output to the SoC
- APC monitors the difference between the requested performance level and the actual level achieved
- Taking into account variations due to differences in process technology and ambient temperature the system dynamically changes the voltage applied
- The lowest energy consumption is achieved OR
- A specified performance level can be met
Appendix B: External non-confidential publications

AVS Energy Management System

- APC operates in closed loop control mode using HPM to adapt to actual process and temperature
- PowerWise™ Interface provides fast control of EMU and feedback of status for optimum control

PowerWise™ technology

- Adaptive Power Controller (APC)
  - Manages performance level requests
  - Uses hardware monitor to reduce safety margins
- PowerWise Interface (PWI)
  - High-speed, low-power 2-wire communications interface between APC and SoC-wide power supplies
  - To be published as open standard (9/03)
- Power Management Unit (PMU)
  - High-performance, off-chip power supply
  - Interfaces using PWI
  - Supports open and closed loop control
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**Integration challenges**

- Multiple voltage domains (and interfaces)
  - Commercial voltage scaling exploited at chip not SOC level
  - Level-shifter technology abstraction required
  - Builds on power-down and state-retention 'islands'
- Multiple (asynchronous) clock domains
  - Real-time domains typically require fixed clocks
  - Variable voltage domains quantize frequency
  - External memory clock rates often fixed
- External power-control interface handshakes
  - Efficient management of voltage/frequency (PLL) settling times
- Design verification and test
  - Gap between RTL (ideal clocks, implicit power) and layout
  - Static timing analysis and clock distribution in particular
Appendix B: External non-confidential publications

**Collaborative SoC Design**

Complete Energy Management solution requires:
- (Off-chip) Power switcher technology
  - Responsive and controllable
- Semiconductor cell/RAM library technology
  - Characterization across voltage/process
  - Level-shifter technology
- On-chip power control technology
- System level design methodology/EDA tools
- Software/API support for OS
  - Predictive performance setting algorithms

> Partnership approach to implementation

**Prototype IEM test chip**

- ARM926EJ-S core
- Multiple power domains
- Voltage and frequency scaling of CPU, caches and TCMs
- First full DVS silicon with National Semiconductor PowerWise™ technology
- NSC Adaptive Power Controller (APC) implemented in FPGA

- Delivered from TSMC 0.13μm fab. in July 2003
- Developed by ARM and National Semiconductor using Synopsis EDA tools
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**IEM test chip power domains**

- CPU domain
- Peripheral bus domain
- Async. domain
- System bus domain

- Dynamic Voltage RAM with state retention
- Dynamic Voltage CPU with power-down

- Dynamically scale voltage to both CPU and RAMs
- But support state save to RAM and power-down of CPU
- Level-shifter cells interface to always-powered SOC logic
- Clamps hold signals low when domain voltage "unsafe"
Appendix B: External non-confidential publications

Benchmarking

- Clear requirement to develop benchmarks
- Standby time taken care of by conventional power management schemes (run/idle/sleep)
- Focusing on applications processors and smartphone functionality (more “running” time)
  - MP3 players – sound recording
  - MPEG4 video clip players/capture
  - Games – graphics accelerators
  - E-mail and web access (WAP), messaging
- Need to measure energy saving and quality
- No established benchmarking standards exist today that show quality at low performance
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Energy Management in Action

Wrap Up

- Dynamic performance control is an attractive way of achieving energy management in battery-powered embedded devices **BUT**
  1. There are many challenges at the SoC design level in implementing multiple power domains:
     - Interfacing between power domains
     - EDA tools support
  2. Maximising the benefits of techniques like Dynamic Voltage Scaling requires:
     - SoC designs that include appropriate controls
     - Advanced software to manage performance
     - Standard s/w and h/w interfaces to allow reuse
Appendix B: External non-confidential publications

Intelligent Energy Management

Thank you for listening.

Any Questions?

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ARM
THE ARCHITECTURE FOR THE DIGITAL WORLD™
Energy efficient SOC design technology and methodology
IEM926: An Energy Efficient SoC with Dynamic Voltage Scaling

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Abstract

One of today's most successful embedded devices, the mobile phone, embodies a set of challenging design requirements: long battery life, small size, high performance and low cost. The processor parameter that complicates the simultaneous fulfillment of all of these design goals is energy efficiency of the system, since batteries only hold a finite amount of charge. To operate within the allotted energy budget, systems must be optimized for energy consumption during design and also at run-time. Increasingly it is not sufficient to statically optimize for worst-case conditions but designers must enable systems to adapt to conditions at run-time. The Intelligent Energy Manager® (IEM) technology provides an integrated solution for addressing energy management of SoC devices. In this paper, we present data about the energy consumption characteristics of a multiple power-domain based SoC which includes PDM functionality built around an ARM926EJ-S core.

1. Introduction

Power consumption is arguably the most important feature of embedded processors with significant impact on the cost and physical size of the end device. Historically, low power consumption in embedded processors has been achieved through simplicity, limited use of speculation, and through the use of low-power sleep modes that reduce idle-mode power consumption. Embedded processors are now performing more sophisticated tasks, which require even higher performance levels. As a result, new processor designs are more dependent on sophisticated architectural techniques (such as prediction and speculation) to achieve high performance. Unfortunately, such techniques can also significantly increase the processor's power consumption.

One way to bridge the gap between high performance and low power is to allow the processor to run at different performance levels depending on the workload's requirements. An MP3 audio player, for example, requires about an order of magnitude less performance than an MPEG video player. The difference in performance requirements can be exploited to save energy with the use of dynamic voltage scaling (DVS). DVS exploits the fact that the peak frequency of a processor implemented in CMOS is proportional to the supply voltage, while the amount of dynamic energy required for a given workload is proportional to the square of the processor's supply voltage. Reducing the supply voltage while slowing the processor's clock frequency yields a quadratic reduction in energy consumption, at the cost of increased run time [5].

The IEM technology includes software components that can accurately predict the minimum necessary performance level of the processor for the running workload, thus a reduction of performance does not necessarily imply any degradation of quality [3]. In this paper we show the potential energy savings that can be achieved on a real SoC using dynamic voltage scaling.

2. The IEM926 test chip

The IEM926 test chip was explicitly designed to support DVS and fast clock-switching and includes on-chip peripherals that are similar to the ones found on PDA devices. The test chip includes the following components, graphically illustrated in Figure 1:

- ARM926EJ-S processor with caches (16K I and D)
- 16K I and D Tightly Coupled Memories (TCMs)
- 240, 180, 120, 60, 0 MHz processor performance levels
- A DMA subsystem
- The Intelligent Energy Controller prototype
- SDRAM and Flash memory controllers and basic peripherals (including on-board audio) to support a minimal Linux environment
- Interface to National Semiconductor's PowerWise™ controller to support open- and closed-loop DVS [6]

The SoC is partitioned into three power domains. The system bus and peripheral bus subsystems are in a single power domain supplied with a fixed 1.2V. The CPU domain is the only domain whose frequency and voltage can be varied dynamically and it includes a separate power domain for the TCMs which can be placed in a low-power state retention mode while the main processor is powered off. The design includes clamps between the TCMs and the core to

---

FIGURE 1 Components of the IEM926 SoC
support this mode of operation, however, when running, both the TCM and core run at the same voltage and frequency.

The test chip was manufactured using the TSMC 0.13G process. A picture of the 5x5mm die is shown in Figure 2 without the processor (middle box), two PLLs (top left and right corners) and instruction and data TCMs (middle right box). The system includes two PLLs, one controls the frequency of the processor and another provides a fixed frequency for the peripherals.

2.1 Clocking strategy

The two main challenges of the SoC design were to support fast switching between the available frequency levels and to support dynamic frequency changes on a core with only synchronous bus interfaces. The first issue was solved by the use of frequency division of one of the PLLs running at 480 MHz to four frequency levels: 240, 180, 120, and 60 MHz. On the other hand, the chips successfully operate at 300, 225, 150, and 75 MHz by running the PLL at 600 MHz. To simplify the system design, the system bus and peripherals run at a fixed 25% of the peak frequency of the processor. Generating a frequency at 75% of peak is a challenge with a single PLL, further complicated by the need for synchronous interfaces to the buses. The solution employed in this chip relies on a skew clock that has an uneven duty cycle (3/8 comprised of 1 1 5, 1 1 5, 1 2 core to PLL clock ratios), ensuring that the bus and core clocks are aligned on the rising edge of each bus clock transition. In the following figures, the data points corresponding to a wide variety of frequencies were generated by under- and over-driving the 480 MHz PLL by -10% to +25% in 5% increments and then dividing by the four ratios (1, 3/4, 1/2, 1/4).

2.2 Voltage levels

Figure 3 shows the minimum voltage levels sufficient for sustaining a wide range of frequencies on the core at room temperature. The peak frequency of the core is set between 215 and 390 MHz and scaled to 75%, 50%, and 25%. Theoretical models suggest a linear relationship between voltage and frequency. Our measurements broadly confirm these expectations with two important differences in voltages for frequencies corresponding to 75% of peak. Above the linear predictions and voltages for minimum (25%) frequencies do not substantially decrease below the levels at 50% and in fact show an increase for lower frequencies.

The former irregularity is explained by the clocking technique employed on the SoC at the 75% peak frequency. The core is actually operating slightly (a little over 6%) faster than 75% due to the interface with synchronous buses. The higher actual frequency in turn necessitates a higher operating voltage, which explains the divergence. The irregularity at low frequencies is as yet unexplained but is likely to be caused by the level-shifters employed in the system. We have also observed that the voltage characteristics when caches are turned off are substantially the same as in the graph above, thus in this case, the sense-amplifiers are not the cause of the lower limit on voltage scaling.

3. Power and energy

Figure 4 shows that there is a linear relationship between the core's frequency and the amount of work done per unit time in a processor-bound workload. As expected, running at 25% of peak frequency causes this workload to
run four times longer. In general, bus-bound applications exhibit a flatter slope, meaning that due to the uneven scaling of bus frequencies, with reduced frequency the workloads' run-time increase at a lower rate than that of processor-bound applications.

Figure 5 shows the ARM926EJ-S core's power consumption and energy use (including on-chip cache and RAM structures) when running Dhrystone on a wide range of frequency and voltage levels. Energy consumption is normalized to the amount used at the statically characterized maximum operating point (240MHz at 1.2V). Our results show that a factor of 10 (90%) power and more than a factor of two (65%) energy saving is achievable by running the cores at their minimum levels (25% of peak frequency). However, there is very little pay back on running the core below the half-frequency point since voltage cannot be significantly reduced and consequently the energy consumption remains about the same. On the other hand, if heat management (thus average power consumption) is an issue, then more power savings can be achieved by further lowering the frequency—this behaviour is shown at the bottom of the power curve.

Our measurements match the theory; the power consumed during a workload is proportional to the frequency times the square of the voltage at which it is run. Since energy is the integral of power consumption, the longer execution time due to lowered operating frequency cancels out the frequency term and thus energy consumption is proportional to the square of the operating voltage.

The amount of energy saved for a given workload depends on the peak frequency and voltage levels of the core. Table 1 illustrates our results when running a workload at the minimum 25% (second column) and 50% (third column) for three maximum frequencies. Results in the second column show that there is more energy reduction if the peak frequency and voltage levels are higher. One reason for this is that our hardware does not function below 0.7V and this voltage level can already be achieved at 50% of maximum frequency for the 240MHz and 216MHz configurations. Thus implies that the 25% frequency levels of these configurations do not significantly reduce energy consumption any further.

However, even on cores with lower minimum voltage levels, the primary benefit of voltage scaling is towards the top end of the frequency range. This is a consequence of the scaling equations and the quadratic relationship between energy consumption and operating voltage [4]. The third column of Table 1 shows the energy savings for workloads running at half of maximum frequency. While the difference between the reported energy savings in each row is less than in the first case, the trend is clear: higher maximum frequency and voltage enables more energy savings when slower operating levels are used.

### 3.1 Operating margins

Data in the previous sections were collected for minimum voltages at room temperature. However, there is no guarantee that the same voltage levels would be sufficient to run the processor at the specified frequencies under different conditions (or that different chips would behave the same way). To deal with uncertainty and variations due to the ambient environment, silicon, IR-drop, etc., designers include operating margins in the voltages that are specified for each frequency level.

The first graph in Figure 6 shows the energy impact of the operating margins on the JEM926 processor running at the four different frequency levels that are achievable in a single configuration. For each frequency, the energy consumption of the Dhrystone workload is plotted using five different voltage levels. The limit voltage—below which the system fails to operate—and at 5%, 10%, 15%, and 20%

---

**TABLE 1 Energy savings at different (f, V) points**

<table>
<thead>
<tr>
<th>Max speed (MHz)</th>
<th>Workload speed (MHz)</th>
<th>Energy reduction</th>
<th>Workload speed (MHz)</th>
<th>Energy reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>75</td>
<td>66%</td>
<td>150</td>
<td>54%</td>
</tr>
<tr>
<td>240</td>
<td>60</td>
<td>56%</td>
<td>120</td>
<td>48%</td>
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<tr>
<td>216</td>
<td>54</td>
<td>46%</td>
<td>104</td>
<td>45%</td>
</tr>
</tbody>
</table>
FIGURE 6 The energy impact of operating margins

above the minimum. The knee in the line at 120MHz shows the limited energy savings at the 60MHz level due to the hard limit on minimum voltage that is near the same level as at 120MHz. Typical tolerance levels on supply voltages are between 10%-15%, which translates into 20%-25% energy overhead when the processor is not running close to worst-case conditions. The energy consumption of the different configurations is normalized to the amount consumed at the statically characterized level (240MHz at 1.2V), which corresponds closely to the line with 15% voltage overhead. The second graph in Figure 6 shows the energy consumption of the workload without voltage scaling. In these experiments, the operating voltage was kept at the statically characterized level and at levels 5% and 10% above and below for all frequency points. The results show that without voltage scaling the energy consumption for a workload is not reduced and in fact may increase at lower frequencies. We believe that this behavior is due to on- and off-chip bus interactions and extra overhead incurred during some memory transactions. While the +5% and +10% voltage levels may be beyond the amounts that are incorporated into the processor's operating margins, such overshoots may be a function of the power regulator. Accurate power delivery is an important component of an energy efficient system as even a small increase over the necessary voltage level incurs significant energy overhead.

4. Conclusion and future work

Our results show that voltage scaling enables significant reduction of the energy consumption of the core implemented in a 130nm process. Our ongoing work quantifies the system-wide impact on energy consumption under real workloads, operating systems, and performance-setting policies. Our initial results indicate that when running at the peak level, the processor accounts for 75% of the energy used on the IEM926 SoC. Our data confirms that while designing with worst-case parameters may be necessary, actually running a chip with worst-case voltage levels wastes energy in our case up to 25%. Our ongoing research explores on-chip structures [1] and microarchitectural techniques [2] for reducing operating margins.

5. Acknowledgements

The IEM926 design was done as a joint project between ARM, Synopsys, and TSMC. We thank Anwar Awad and Han Pin-Hung Chen of Synopsys for their implementation work.

References

Appendix B: External non-confidential publications

ARM Perspective

"Intelligent Energy Manager"

Implementation = IP + Libraries + Tools + Flow
(oh yes + PSU + SW + OS + effort!)

David Flynn
ARM Fellow, R&D Cambridge UK

ARM1176EJZ Implementation

"Reference Methodology"

IP/RTL Design
- Hierarchical structuring
- DVFS Interfaces
- Isolated voltage islands

Multi-voltage implementation
- Floor-planning
- MV-timing constraints and STA
- ARM (Metro™) Physical IP
Summary: IEM/DVFS challenge

IP design and RTL
- Multiple voltage domains -> multiple clock domains
- Partitioning and interfaces require special care
- What clock frequency/voltages are energy efficient?

Library enhancements
- Level Shifters, Isolation cells
- Multi VDD Characterization (Std Cells and Memories)
- Multi VT Cells

Tools
- Multi-Voltage aware Galaxy Platform
- Multi-VT Optimization

Jointly developed IEM Reference Methodology

Cached CPU DVS Analysis

Full (tedious!) transistor level PathMill/NanoSim

(1) Timing/Power: Analysis across all corners:

(2) Energy efficiency: Additional analysis for typ si:
Appendix B: External non-confidential publications

Joint IEM technology project ARM
ARM/Synopsys/National Semiconductor/UMC “ULTRA926”
- IEM technology demonstrator
- ARM926-based SOC
  - 144-288MHz DVFS
- DVS and AVS support

Detailed power and energy simulation
Correlate with Silicon plan late Q2

IEM Leakage mitigation next... ARM
Customers want ARM to support many of the following:

1. Mixed Vt libraries (2, 3 even 4 VTs!)
   - EDA tools support now
2. Multi-rail switched domains
   - External power down of sub-systems
3. On-chip Power Gating (MTCMOS)
   - Local fine/coarse grain power header/footer switches
4. Retention Registers (a.k.a. “Balloon Flops”)
5. Reverse Bias memory leakage support
6. Dynamic Threshold Scaling (VTCMOS)
   - Support for both forward and reverse bias operation
Energy efficient SOC design technology and methodology
Appendix B: External non-confidential publications

Synopsys ATG 45nm offsite
ARM IP and design perspective

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ARM R&D (Cambridge)

Overview

- R&D Technology demonstrators
  - System level design, implementation, analysis
  - Representative EDA and customer issues
  - IP design and integration investigation
- Leakage Mitigation approaches
  - Power Gating and Retention Registers focus
- Transistor analysis of std-cell designs
  - Predicting energy efficient modes of operation
- “Razor” fault-recovery design
  - Early work...
- EDA challenges
Energy efficient SOC design technology and methodology

Technology and Implementation

- Battery products require industry-wide partnership:
  - Technology/library optimization for 'leakage control'
  - EDA: implementation, modelling and analysis
  - PSU: Dynamic power/bias rails, Power-switch
  - OS: architected API’s for 'sleep-depth' modes
  - IP: architected control interfaces
- Evolving approaches to leakage mitigation...
  - Re-evaluate every technology/product node
    - Threshold scaling, retention Flops, power switching
    - RAM state save/retain/restore
- **System level evaluation prototypes from ARM seen as industry-leading application benchmark platforms**
  - Significant high-profile collaboration potential...

Technology Demonstrators

- Small enough to fit low(er) cost fab shuttle runs
  - Typically 4x4 -> 3.5x3.5mm dies size 65nm...
  - Modest complexity
- Multiple Power Rail
  - Separate supplies for measurement/control
  - DVFS interface support between regions
- "Representative" design architecture
  - Applications processor+L1 cache
  - Low power system with L2 memory
  - Linux environment for SW evaluation
  - Methodology and power management prototype
Appendix B: External non-confidential publications

**Technology Demonstrator architecture**

**IEM DVS Technology Demonstrator**

- Three primary on-chip voltage domains
Energy efficient SOC design technology and methodology

**Leakage Reduction – Customer view**

*Customers prefer varying options, ARM need to address all:*

1. Mixed Vt libraries
   - EDA tools support now
2. Multi-Rail Power-Switched domains
   - Externally power-down of subsystems
3. Switched 'Virtual' Power Rails (MTCMOS etc)
   - On-chip power-gating
4. Retention Registers (a.k.a. 'Balloon flops')
   - Preserve register state, power down logic
5. Reverse Bias Retention Domains
6. Additional leakage current reduction
7. Dynamic Threshold scaling (VTCMOS etc)
   - Dynamically change threshold (and supply) voltage

---

**Leakage Reduction – SOC Implications**

*IP implementation and deployment challenges:*

1. Mixed Vt libraries
   - Reduce leakage on non-critical paths, no system issues
2. Multi-Rail Power-Switched domains
   - Clamp interfaces, long power ramp times, state save req.
3. Switched 'Virtual Rail' Power-Gating
   - Clamps, area cost and delay analysis, state save/restore
4. Retention Registers
   - Area cost, extra power routing, but energy efficient re-start
5. Reverse Bias Power Switching
   - Area/power cost, superior leakage, VBB generation req.
6. Dynamic Threshold scaling (VtCMOS etc)
   - Well/Bulk routing overheads, triple-well process, PSU+
Appendix B: External non-confidential publications

**Multi-Threshold CMOS (MTCMOS)**

- Multi-threshold CMOS
  - Dual-Vt technology...high-Vt transistors gates power supplies
  - Per-cell (very area expensive)
  - Characterize within the cell
  - Add extra sleep ‘mode’
  - Shared (less area expensive)
    - Virtual power rails shared
    - Distributed power switches
      - Rows/columns/grids
      - I/R-analysis serious challenge
- Issues:
  - tx sizing, distribution strategy, analysis flows, tool flow support, loss of state, ...
  - Safe power switch-on (in-rush current, phased control timing)

**MTCMOS power architecture**

- 'Footer' switches added to high-speed domain
Energy efficient SOC design technology and methodology

**State Retention Registers**

- Retention flops (aka Balloon flops)
  - High-Vt slave latch on separate power
  - Seek to minimize CK->Q delay
  - State retained
  - Issues: extra power rail support implementation, analysis, ...
- EDA front end support
  - ‘sleep’ attributes
- In-rush currents/ noise immunity challenge for production

IEM: Architected Sleep/Wake + PSU handshakes

**Retention Register power architecture**

- Retention Register supports state save/restore

![Diagram of retention register power architecture](image)
Appendix B: External non-confidential publications

"ULTRA926" IEM technology project

- UMC collaboration
  - ARM design and Metro physical IP
  - National Semiconductor Adaptive Power IP
  - Synopsys SPS multi-voltage implementation
- IEM technology demonstrator
- ARM926-based SOC
  - 144-288MHz DVFS
  - Pre-hardened CPU core
  - DVS and AVS support
- Detailed power and energy simulation
- Correlate with Silicon plan late Q2

Standard-cell design, Tx analysis

- Usual design challenge (for CPU) is to attain $F_{\text{MAX}}$ for worst case process/temp/VDD$_{\text{NOM}}$-10%
- Applications processors compete on MHz etc.
- Re-characterizing library and memories at extended PVT operation points is tough
  - AND pessimism tends to scale (better or worse?)!
- So take the Std-Cell/RAM synthesized design and resort to HPSICE transistor level analysis
  - PathMill, TimeMill, NanoSim...
  - Very long machine run-times, full cache memories require large memory machine
Energy efficient SOC design technology and methodology

Voltage/Power level analysis (MHz/V)

- Given PVT derive accurate cycle time
- Approx 1 day per analysis point

Detailed leakage analysis (µA/°C)

- Given PVT derive accurate leakage prediction
- Only 3-4 hours per point
Appendix B: External non-confidential publications

**Voltage scaling limit analysis (F/V/°C)**

- To understand typical silicon limit of DVS
- ~3 days per analysis point
- Understand the temperature inversion point

**Typical Power analysis (uW/MHz/V)**

- To understand typical silicon DVS power
- ~3 days per analysis point
- Key to understanding energy efficient frequencies
- Leakage
Combining the WC/Typ analysis

- Energy analysis finally built up from all the data
- Open-loop voltage scaling (WC Si) and AVS
- Typical silicon power->energy analysis

Robust Design for Low Power Applications

Low power antagonistic to robust design
- Increased sensitivity to Vt variation in low voltage operation
- Dynamic voltage scaling
- Subthreshold voltage operation
- Clock gating and low power modes increase power grid noise
- Power optimization equalizes circuit delay

Fundamental challenge in nanometer design: Robust and Low Power Design
Robust Low Power Design

- Worst-case conditions highly improbable
  - Many sources of variability are independent (process, noise, SEU, supply drop)
  - Probability of all sources simultaneously having worst-case condition very low
  - "guaranteed correct" design highly inefficient
- Common case design paradigm
  - Significant gain for circuits optimized for common case
  - Efficiency mechanisms needed to tolerate infrequent worst-case scenarios
- In-situ error detection and correction
- Dynamic runtime adjustment to silicon and environmental conditions

Self-Regulating DVS with Razor

- Goal: reduce voltage margins with in-situ error detection and correction for delay failures

- Proposed Approach:
  - Tune processor voltage based on error rate
  - Eliminate safety margins, purposely run below critical voltage
    - Data-dependent latency margins
    - Trade-off: voltage power savings vs. overhead of correction
  - Analogous to wireless power modulation
Razor Flip-Flop Implementation

- Compare latched data with shadow-latch on delayed clock

- Upon failure: place data from shadow-latch in main latch
  - Ensure shadow latch always correct using conservative design techniques

- Key design issues:
  - Maintaining pipeline forward progress - Recovering pipeline state after errors
  - Short path impact on shadow-latch - Meta-stable results in main flip-flop
  - Power overhead of error detection and correction

Centralized Pipeline Recovery Control

- Once cycle penalty for timing failure
- Global synchronization may be difficult for fast, complex designs
- Implementation currently being explored for ARM 926 commercial core
Appendix B: External non-confidential publications

### Distributed Pipeline Recovery Control

- Builds on existing branch / data speculation recovery framework
- Multiple cycle penalty for timing failure
- Scalable design since all recovery communication is local
- Prototype chip results available

### Trade-Off in Razor DVS

- Pipeline IPC
- Total Energy
- Recovery Energy
- Processor Energy
- Energy w/ overhead
- Optimal Voltage
- Supply Voltage
Energy efficient SOC design technology and methodology

**ARM Razor SOC Prototype**

ARM9 based CPU prototype in development
- Cut-down feature set of ARM926EJ-S
- 5 stage pipeline, I&D caches, MMU
- no TCM, coprocessor or ETM interface
- check-pointing features added to micro-architecture
- More real life example than original Alpha
- (data-path) prototype
- Allows comparison with existing ARM926 technology demonstrators

**Razor Design Flow**

- Tools and Design Flow
  - Automatic insertion of razor flops into physically optimized netlist
  - Hold fixing (up to a phase extra hold required)
  - Insertion of error gather OR tree
    - Large OR tree, pipelined to avoid critical error path
  - Analysis of propagation of unknown state
    - Architectural state must be preserved
    - Must not propagate to I/O
Appendix B: External non-confidential publications

**EDA challenges / Conclusion**

- **Models**
  - Scalable Polynomial Models (future after CCS?)
    - Expensive to generate, valuable for operating points
  - Supply and Threshold Scaling
    - multi-dimensional model challenge for leakage

- **Enhanced EDA support:**
  - "GALS" EDA support (test/BIST, verification)
    - Subsystem timing closure, async interconnect
  - Energy analysis support for designers
    - Entry/exit cost to dynamic/standby power modes
  - Collaboration (Academic/EDA/Library/IP)
    - (oh yes + PSU + SW + OS + methodology)
Energy efficient SOC design technology and methodology
Appendix B: External non-confidential publications

SOC and IP Design challenge

Advancements in Energy-Efficient Design

System Level Dynamic Power/Energy Management

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Overview

- Systems level challenge
  - SW/SOC/PSU design, EDA/Library implications
- Dynamic Power/Energy Management
  - Dynamic Voltage and Frequency Scaling
  - Real-world design issues
- Static/Leakage Power Management
  - Multiple power management states
- Work in progress...
CMOS Power and Energy in a Nutshell

- Power and Energy consumption trends of a workload running at different frequency and voltage levels.
  - DFS: frequency scaling only
  - DVFS: frequency & voltage scaling

\[ f = \left( \frac{V_{dd} - V_t}{V_{dd}} \right)^{1.3} \]

\[ P = CV_{dd}^2f + V_{dd} I_{leak} \]

\[ E = \int P dt \]

Must reduce voltage to save energy and extend battery life!

Performance scaling for energy efficiency

- Reduced processing rate enables more efficient operation
  - Need software intelligence to meet (multiple) task deadlines
Design for DVFS

• Need to determine set of energy efficient performance points / clock frequencies
  ▪ Not easy: EDA tools will give you 1/frequency (eventually) from set of Process/Voltage/Temperature conditions
  ▪ Voltage headroom on sub 1.2V process technologies needs great care – especially RAM
• Energy efficiency is product of power x time to complete workload to a deadline
  ▪ Leakage impact must be factored

Design for DVFS – stage 1A

• Determine $F_{\text{MAX}}$ at worst case conditions
  ▪ Worst case process/temperature
  ▪ $V_{\text{NOM}} - 10\%$ voltage
  ▪ Standard Cell-based set-up timing sign-off
  ▪ (Confirm with Transistor-level simulation)
• Analyse clock latency for synchronous design interfacing
• Repeat analysis at wider operating voltages
  ▪ Transistor simulation of caches for accuracy
Design for DVFS – “Slow” analysis

Design for DVFS – stage 1B

- Determine typical silicon characteristics
  - Typical process/room temperature
  - $V_{NOM}$ initial voltage
  - Standard Cell-based power sign-off corner
  - (Confirm with Transistor-level simulation)
- Also analyse clock latency for synchronous design interfacing
- Repeat analysis at wider operating voltages
  - Transistor simulation for accuracy...
Appendix B: External non-confidential publications

Design for DVFS – “Typ” analysis

Design for DVFS – stage 1C

• Determine fast corner characteristics
  ▪ Fast silicon / lowest rated temperature
  ▪ \( V_{NOM} +10\% \) initial voltage
  ▪ Standard Cell-based hold-time sign-off corner
  ▪ (Confirm with Transistor-level simulation)
• Also analyse clock latency for synchronous design interfacing
• Repeat analysis at operating voltage extremes
  ▪ Transistor simulation for accuracy...
Energy efficient SOC design technology and methodology

Design for DVFS – “Fast” analysis

![Graph of UMC HS130 DVFS Analysis](image1)

DVFS Frequency range analysis

![Graph of DVFS Frequency range analysis](image2)
Power Analysis – stage 2

- Typical silicon power analysis is most important to understand for product design
- Dynamic power analysis requires representative workload code/vectors
  - Application dependent in final product
- Static power analysis requires representative halt-state vectors
  - Data dependent analysis
- Prerequisite to determining energy efficiency
  - Run at lower power for longer to complete workload...
Dynamic Power Analysis

- Boot cached system and cache test code
  - Infamous Dhrystone benchmark, etc...
  - Need to ensure cached behaviour analysed
- Normalise the results as power/MHz
  - To facilitate
- Subtract out the leakage component
  - .. To factor back in for final power
- Slow and tedious simulation job...

Typical Power analysis (uW/MHz/V)

- To understand typical silicon DVS power
  - ~3 days per analysis point (NanoSim)
  - Key to understanding energy efficient frequencies
  - Leakage component subtracted

![Average power graph]

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Detailed leakage analysis (μA/°C)

- Given PVT derive accurate leakage prediction
  - 3-4 hours per point to simulate (NanoSim)

![Leakage current vs temperature graph]

Safe Voltage Scaling Range? (stage 3)

- Memory typically the critical limitation
  - Write operation margins
  - Sense-amp read safety
  - Soft Error Rate highly voltage sensitive
  - Off-chip supply and load regulation
- Beware “temperature inversion” point where slow and fast timing cross over
  - Ensure minimum operating voltage above this
Analysing delay versus temperature

Typ/Typ Silicon scaling with Temperature

Operating Frequencies – Stage 4

- Key characteristics now understood (at last!):
  - $F_{\text{MAX}}$ determined by worst case silicon
  - Understand DVFS frequency/voltage
  - Understand DVFS power scaling
- Clock generation choices:
  - Fast-switching PLLs to switch frequencies
  - Master PLL with digital divider alternative
  - Must handle clock/voltage switching carefully
  - Clocking while changing voltage desirable
    - Serious real-time impact otherwise
Appendix B: External non-confidential publications

Worked example

• In this case FMAX worst case 288MHz/“100%”
• Below 144MHz/50% no safe voltage headroom
• Instant-switching clock generator chosen
  ▪ Single PLL at multiple of SDRAM/bus speed
• 4 levels of frequency scaling chosen (plus 0%)

<table>
<thead>
<tr>
<th>Performance Level</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>288</td>
</tr>
<tr>
<td>83%</td>
<td>240</td>
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<tr>
<td>67%</td>
<td>192</td>
</tr>
<tr>
<td>50%</td>
<td>144</td>
</tr>
<tr>
<td>0%</td>
<td>0</td>
</tr>
</tbody>
</table>

Determining Energy Efficiency

• DFS simply scales workload over time
  ▪ Lower temperature is a benefit
  ▪ But beware leaking for longer period...
• DVFS analysis takes product of time to complete workload and power consumed
  ▪ Benefits from dominant $V_{dd}^2$ term scaling
  ▪ For “open-loop” control need worst-case Si
  ▪ For “closed-loop” control can compensate for actual process and temperature and benefit from typical Si.

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Energy Saving Analysis – Stage 5

![Graph showing voltage headroom/energy savings compared to WC 1.08V 125C](image)

DVFS Design Requirements

- DVFS requires detailed analysis work
  - Slow/Fast analysis required for timing as usual
  - Extra Typical analysis required to understand battery life implications and sensible operating performance points
- Energy savings – for the DVFS sub-system can be significant and important for designers who stay on lower-cost 130nm+ technologies
  - Compete on Max MHz and Average battery life
Appendix B: External non-confidential publications

Standard-cell design plus Transistor-level analysis?

- Usual design challenge (for CPU) is to attain $F_{MAX}$ for worst case process/temp/VDD$_{NOM}$-10%
  - Applications processors compete on MHz etc.
- Re-characterizing library and memories at extended PVT operating points is tough
  - AND pessimism tends to build up
- So take the Std-Cell/RAM synthesized design and resort to HPSICE transistor level analysis
  - PathMill, TimeMill, NanoSim...
  - Very long machine run-times, full cache memories require workstations with large physical memory

Joint IEM technology project

ARM/Synopsys/National Semiconductor/UMC “ULTRA926”

- IEM technology demonstrator
- ARM926-based SOC
  - 144-288MHz DVFS
- DVS and AVS support

- Detailed power and energy simulation
- Correlate with Silicon plan late Q2
Energy efficient SOC design technology and methodology

**DVFS Implementation challenges**

- IP design and RTL
  - Multiple voltage domains -> multiple clock domains
  - Partitioning and interfaces require special care
  - What clock frequency/voltages are energy efficient?
- Library enhancements
  - Level Shifters, Isolation cells
  - Multi VDD Characterization (Std Cells and Memories)
  - Multi VT Cells
- Tools
  - Multi-Voltage aware synthesis/verification/STA/test
  - Multi-VT Optimization requires extra care
- IP requires implementation methodology

**ARM1176EJZ Implementation**

"Reference Methodology"

IP/RTL Design
- Hierarchical structuring
- DVFS Interfaces
- Isolated voltage islands

Multi-voltage implementation
- Floor-planning
- MV-timing constraints and STA
- Physical IP "Multi Voltage Kits"
Intelligent software control is key

"Intelligent Energy Manager" resides in the OS kernel and derives task performance requirements from kernel calls

Key is not having to change/touch the applications
But if you can, then can do even better "prediction"!

DVFS in summary!

Implementation = IP + Libraries + Tools + Flow
(oh yes + PSU + SW + OS + effort!)

• Significant energy efficiency gains in many products
  ▪ e.g. Smartphone an MP3 player 95% of on-time?
• Requires voltage headroom and careful production support
• Design for worst case, optimize for typical Si
Energy efficient SOC design technology and methodology
SOC and IP Design challenge

Advancements in Energy-Efficient Design

System Level Leakage Mitigation

David.Flynn@arm.com

Overview

• Systems level challenge
  ▪ SW/SOC/PSU design, EDA/Library implications
• Dynamic Power/Energy Management
  ▪ Dynamic Voltage and Frequency Scaling
  ▪ Real-world design issues
• Static/Leakage Power Management
  ▪ Multiple power management states
• Work in progress...
Energy efficient SOC design technology and methodology

IEM Leakage mitigation next...

*Customers want ARM to support many of the following:*

1. Mixed Vt libraries (2, 3 even 4 VTs!)
   - EDA tools support now
2. Multi-rail switched domains
   - External power down of sub-systems
3. On-chip Power Gating (MTCMOS)
   - Local fine/coarse grain power header/footer switches
4. Retention Registers (a.k.a. "Balloon Flops")
5. Reverse Bias memory leakage support
6. Dynamic Threshold Scaling (VTCMOS)
   - Support for both forward and reverse bias operation

Leakage Reduction – SOC Implications

*IP implementation and deployment challenges:*

1. Mixed Vt libraries
   - Reduce leakage on non-critical paths, no system issues
2. Multi-Rail Power-Switched domains
   - Clamp interfaces, long power ramp times, state save req.
3. Switched ‘Virtual Rail’ Power-Gating
   - Clamps, area cost and delay analysis, state save/restore
4. Retention Registers
   - Area cost, extra power routing, but energy efficient re-start
5. Reverse Bias Power Switching
   - Area/power cost, superior leakage, VBB generation req.
6. Dynamic Threshold scaling (VtCMOS etc)
   - Well/Bulk routing overheads, triple-well process, PSU+
Appendix B: External non-confidential publications

**Multi-Threshold CMOS (MTCMOS)**

- Multi-threshold CMOS
  - dual-Vt technology ...high-Vt transistors gates power supplies
- Per-cell (very area expensive)
  - Characterize within the cell
  - Add extra sleep 'mode'
- Shared (less area expensive)
  - Virtual power rails shared
  - Distributed power switches
    - Rows/columns/grids
  - IR-analysis serious challenge
- Issues:
  - tx sizing, distribution strategy, analysis flows, tool flow support, loss of state, ...
  - Safe power switch-on (in-rush current, phased control timing)

---

**MTCMOS power architecture**

- e.g. 'Footer' switches added to high-speed domain

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State Retention Registers

- Retention flops (aka Balloon flops)
  - High-Vt slave latch on separate power
  - Seek to minimize CK->Q delay
  - State retained
  - Issues: extra power rail support implementation, analysis, ...

- EDA front end support
  - 'sleep' attributes

- In-rush currents/ noise immunity challenge for production

System: Architected Sleep/Wake +PSU handshakes

Retention Register power architecture

- Retention Register supports state save/restore

Un-switched Supply Rail
Variable Threshold CMOS (VtCMOS)

- Substrate Bias control, Dynamic/Adaptive Body Bias, etc.
  - State retained...
  - Leakage reduced with reverse bias voltage
  - (Peak processing potentially using forward bias)
  - Triple-Well process cost/complexity
  - On-chip VBB generator(?)
  - Off-chip Bulk/Well voltage controller:
    - Need carefully managed handshakes
  - Issues: Library support, implementation tool flows, complex multi-dimensional timing models

- Voltage scaling orthogonal
  - Timing analysis becomes 'multi-surface'
  - Valuable to address gate leakage

---

Energy Profiles – 1 (state loss)

- Cost of State Save
- Cost of Reset + State Restore
- Real-Time Impact
- Minimal Leakage

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Energy Profiles - 2 (state retention)

IEM Dynamic and Static Power States

- Run states (IEM-Dynamic Performance Control)
  - TURBO – operate at 'maximum' performance
    - "Forward-biased" thermally controlled (e.g. docked)
  - NORMAL – operate at 'standard' performance
    - Standard active state (normal battery operation)
  - SLOW – battery saving reduced performance
    - "Reverse-biased" reduced leakage operation
- Sleep states (IEM-Leakage control, Wake-on-Interrupt)
  - HALT – clocks stopped, static leakage, quick wake
  - SNOOZE – local power gating, retention regs
  - HIBERNATE – state save/restore, ext PSU switching
  - OFF – explicit state restore required, turn cache RAMs off
Appendix B: External non-confidential publications

Leakage Summary + wrap up

- Many leakage mitigation techniques
  - IP providers must support many
- Software need unified OS API
  - To hide the hardware specific sleep states
- Analysis must take into account:
  - Leakage power reduction for each sleep state
  - Energy cost of each sleep state entry/exit
  - Real-time impact of each sleep state entry/exit
  - State-dependent leakage 'bounds'
  - Effect of the thermal profile of run-states

*Key to product battery life...*
Energy efficient SOC design technology and methodology
Appendix B: External non-confidential publications

What’s Hot/Cool in Low-Power Solutions

Sponsored by:

ARM Synopsys

Dynamic Voltage and Frequency Scaling:
The “IEM” System Design Perspective

David Flynn
ARM
Energy efficient SOC design technology and methodology

**Hot performance in Cool products**

“What I need (to compete) is (peak) performance but not at the expense of great battery life…”

- Performance challenge is worst-case timing closure
- Need $F_{\text{MAX}}$, but run as an MP3 player most of the time

“I need to port OS quickly and to run 3rd party software”

- Products typically differentiated by the software
  and 3rd party applications cannot be profiled in advance
- Applications need to run without instrumentation/rewrite

Dynamic Voltage and Frequency Scaling is attractive but a complex systems problem...

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**CMOS Power and Energy in a Nutshell**

Power and Energy consumption trends of a workload running at different frequency and voltage levels.

DFS: frequency scaling only, DVFS: frequency & voltage scaling

- **Voltage vs. Frequency**
  - $f \sim \frac{(v_{dd} - \alpha v)}{v_{dd}}$
  - $\alpha = 1.3$
  - $v_{f} / v_{\text{max}} = 0.3$

- **Power vs. Frequency**
  - $P = C v_{dd}^2 f + v_{dd} I_{\text{leak}}$
  - Avg. power ~ heat

- **Energy vs. Frequency**
  - $E = |P_{\text{ult}}|$
  - Need DVS to save energy

Must reduce voltage to save energy and extend battery life!
Appendix B: External non-confidential publications

**ARM Perspective**

"Intelligent Energy Manager"

Implementation = IP + Libraries + Tools + Flow

(oh yes + PSU + SW + OS + effort!)

**ARM1176EJZ Implementation "RM"**

- Hierarchical structuring
- DVFS Interfaces
- Isolated voltage islands

Multi-voltage implementation

- Floor-planning
- MV-timing constraints and STA
- ARM (Metro™) Physical IP
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Summary: IEM/DVFS challenge

IP design and RTL
- Multiple voltage domains -> multiple clock domains
- Partitioning and interfaces require special care
- What clock frequency/voltages are energy efficient?

Library enhancements
- Level Shifters, Isolation cells
- Multi VDD Characterization (Std Cells and Memories)
- Multi VT Cells

Tools
- Multi-Voltage aware Galaxy Platform
- Multi-VT Optimization

Jointly developed IEM Reference Methodology

Cached CPU DVFS Analysis
Full (tedious!) transistor level PathMill/NanoSim

(1) Timing/Power: Analysis across all corners:

(2) Energy efficiency: Additional analysis for typical si/conditions:
Appendix B: External non-confidential publications

Joint IEM technology project

IEM technology demonstrator
ARM926-based SOC
- 144/196/240/288MHz DVFS
DVFS control/analysis support
(plus Adaptive Voltage Scaling)

Detailed power and energy simulation
Correlate with Silicon early Q3
Energy efficient SOC design technology and methodology
Appendix B  External non-confidential publications

RTL to GDSII Design Methodology for Dynamic Frequency and Voltage Scaling Enabled SoC – A Case Study

Dave Scott and Sachin Idgunji  
Staff Design Consultants  
Synopsys Professional Services  

Dar-Sun Tsien, Ph D  
Sr Director of Design Methodology, UMC  

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ABSTRACT

As the merits of dynamic frequency and voltage scaling for SoC energy efficiency are becoming more widely known, design teams are updating their methodologies to accommodate the requirements of variable supply voltage. Two of the most important methodology areas to consider are power planning and static timing analysis. A recent demonstration SoC shows how these parts of the design flow can be tailored to achieve significant power savings.

Synopsys Professional Services and UMC collaborated to create this technology demonstrator SoC based on ARM’s Intelligent Energy Management solution that uses dynamic frequency and voltage scaling on the ARM926EJ-S processor core. The demonstrator chip contains internal memories and peripherals in addition to the processor core that makes the chip a good representative of a typical SoC. The technology demonstrator chips fabricated in UMC 130nm CMOS technology are expected to be available in June 2005.

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Energy efficient SOC design technology and methodology

This paper describes the design challenges of frequency and voltage scaling and the applied design flow from RTL to GDSII, with special focus on design methodologies for power planning and static-timing analysis
1. Introduction

To demonstrate power-management capabilities for a UMC 130nm fabrication process, five partners collaborated in designing the ULTRA926 technology demonstration chip. This paper describes the design methodology used to implement the chip.

Each of the five partners supplied key technology for the complete SoC solution. ARM Ltd provided the Intelligent Energy Manager (IEM) technology. Artisan (now part of ARM) provided the standard cell Metro libraries. National Semiconductor provided the PowerWise™ Advanced Power Controller (APC). Synopsys Inc provides the Galaxy Design Platform and the resources of Synopsys Professional Services to implement the design from RTL to GDSII. Finally, UMC provided the 130nm Fusion process, which is specifically designed for the integration of high-speed and low-leakage transistors in a single SoC die.

The SoC is based on an ARM926EJ-S™ processor and incorporates most of the building blocks typical of today’s SoCs. This technology demonstrator is therefore an accurate representation of the most common types of SoC in development today.

Implementing a device of this type poses many challenges. Some of these challenges are generic to all VDSM SoC developments. Others are specific to the dynamic frequency- and voltage-scaling (DFVS) technology implemented in this device. This paper focuses on two of the most critical DFVS challenges: power planning and static timing analysis.

2. Background on Energy-Efficient SoC Design

Power consumption has become increasingly important for a variety of reasons. Power issues in mainstream deep submicron designs may limit functionality or performance and severely affect manufacturability and yield. Higher power dissipation increases junction temperature, which slows transistors and increases interconnect resistance. Design techniques aimed at improving performance may therefore fail short if power is not considered. Lower-than-expected performance decreases device yield. Additionally, higher power dissipation requires more elaborate system-level measures for thermal management. In general, these power issues are increasing SoC and system costs. Managing power consumption at appropriate points in the SoC design flow keeps these costs under control.

As processes shrink, the problem of power and thermal management grows, and the relative impact of these effects begins to dominate the more traditional tradeoffs of speed and area. At a higher level, the applications that SoCs enable are requiring more energy efficiency as consumers demand longer battery life and more functionality in mobile and hand-held equipment.
Energy efficient SOC design technology and methodology

The ULTRA926 technology demonstrator is designed to show that energy-efficient design is possible within a mainstream design methodology. Compared to conventional designs, ULTRA926-type SoCs can reduce power consumption by as much as 60 percent with no performance compromises.

2.1 Sources of energy consumption

CMOS SoCs consume two types of power: dynamic and static. Dynamic power is the power consumed in switching logic states, both internal to the cells (internal power) and for driving the chip’s nets and external loads (switching power).

\[ \text{Dynamic power} \propto CV^2F \]

where \( C \) is the load (capacitance), \( V \) is the voltage swing and \( F \) is the number of logic-state transitions.

As semiconductor structures become smaller, device and interconnect capacitances decrease, allowing for higher performance and lower power. Countering these factors are power increases due to larger designs and higher switching rates.

Static power (leakage power) is consumed while transistors are not switching.

\[ \text{Static power} = V \text{I}_{\text{STAT}} \]

Although transistors have some reverse-biased diode leakage from drain to substrate, the larger portion of leakage power is due to the sub-threshold current through a transistor that is turned off. This sub-threshold current results from the conduction between source and drain through the transistor channel.

The sub-threshold leakage current is problematic because it increases as transistor threshold voltages (\( V_{th} \)) decrease. In fact, the move to 130 nm and beyond could boost leakage power in some designs as high as 50 percent of the total chip power.

3. Strategies for reducing power consumption

As CMOS technologies scale down, the main approach for reducing power consumption has been to scale down the supply voltage \( V_{DD} \). Voltage scaling is a good technique for controlling a chip’s dynamic power because of the quadratic effect of voltage on power consumption. However, just reducing the power supply degrades circuit speed because the switching delay time is proportional to the load capacitance and the ratio \( V_{th}/V_{DD} \). To maintain sufficient drive strength for fast switching, \( V_{th} \) must also decrease. This decrease leads to the leakage power increase. Fortunately, a power-aware design flow can balance timing requirements with various power goals.

---

1 Analyses for the ARM926 core are presented in appendix A

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The ULTRA926 project minimized power consumption by using multiple $V_{\text{DD}}$ levels and multiple threshold voltages. The design also uses high-level power-management techniques such as a power-aware operating system, sleep mode, compiler optimizations and low-power memory access strategies.

### 3.1 Dynamic strategies

While these traditional methods are effective, the innovative aspects of the ULTRA926 design lie in the use of methodologies and IP associated with dynamic frequency and $V_{\text{DD}}$ scaling. This article therefore focuses on these aspects of the design.

To understand the high-level strategy applied to the ULTRA926 chip, consider the traditional approach outlined in Figure 1. In this approach, parts (or all) of a chip have their clocks turned off when not in use. When the parts are in use, they run at full speed.

![Figure 1 Traditional System Power Management](image)

Figure 2 contrasts this all-or-nothing approach with a strategy of intelligent energy management, in which a task runs only fast enough to meet the application requirement. Reducing both clock speed and $V_{\text{DD}}$ as appropriate for each task saves more power than the full-speed/idle approach\(^2\). Determining the appropriate reduction requires a prediction of how soon the application needs a task to complete.

\(^2\) Assume a task requires 1000 clock cycles to complete, but 2000 clock cycles of time are available. The run/idle method will have 1000 $V_t$ transitions consuming power and 1000 cycles consuming no power. The scaling method will scale both the frequency and the voltage so that it has 1000 $V_t$ transitions consuming power and 0 cycles consuming no power. As long as $V_t$ is less than $V_{\text{DD}}$, the scaling method will consume less power than the run/idle method.
Energy efficient SOC design technology and methodology

Figure 2 Intelligent Energy Management concept

3.2 Potential power reduction from dynamic strategies

While the actual power of the ULTRA926 chip has not yet been measured, results from similar designs indicate that the reductions should be significant compared to devices that use non-dynamic strategies. Reducing clock speed from 288 to 144 MHz obviously cuts power requirements by half, for example. Not quite as obvious are the magnitude of the reductions due to scaling the supply voltage to the minimum acceptable level at the same time. This dual approach cuts power consumption to about 40 percent of full power.

Note that these power reductions apply only to the chip’s dynamic-voltage-and-frequency-scaling subsystems. Normally in such SoCs, some of the chip will not be voltage scalable. Components such as external memories typically operate at a fixed voltage, for example, so design partitioning and planning must take into account the system-level power savings.
Appendix B: External non-confidential publications

4. The ULTRA926 SoC

As Figure 3 shows, the ULTRA926 SoC features an ARM926EJ-S™ processor core connected to an AMBA bus system. The latter comprises high-speed AHB and lower-speed APB peripheral buses. The AHB subsystem contains the interfaces to the external static and dynamic memory subsystems, while the APB connects to a wide range of common peripheral devices such as timers, UARTS, real-time clock and interrupt controller. Clock speeds are 288, 240, 192 and 144 MHz.

Figure 3 ULTRA926 test chip architecture

The chip is partitioned into three primary power domains: voltage/frequency-scaled CPU and memory power domains and a standard fixed-voltage domain for the rest of the chip. The independent power domains allow precise voltage control and current measurement for the CPU and RAM. Standard cells and level shifters operate in the 0.7-1.2V (V_{DD}) range. The project used two libraries characterized for different threshold voltages, and each of these libraries was characterized over the required V_{DD} range.
4.1 The SoC’s power-control elements

The chip’s power-control elements include the ARM Intelligent Energy Controller (shown at upper right in Figure 3) that works with energy-management software to balance processor workload and energy consumption. Other ARM power-related elements include a dynamic clock generator and a unit for power, clock, reset and test.

Additionally, the ARM core’s voltage domain includes a hardware element from National Semiconductor that monitors performance and communicates with voltage regulators to scale the supply voltage to the minimum operating level at each operating frequency. This monitor hardware essentially consists of a delay line to measure the minimum acceptable performance level. The monitor thus calibrates the control system with the actual performance of the silicon. This approach compensates for silicon performance variations due to the manufacturing process as well as run-time performance changes due to temperature fluctuations.

5. RTL to GDSII Implementation

The ULTRA926 SoC implementation methodology followed the traditional 6-step approach consisting of logic synthesis, floorplanning (including power planning), cell placement, clock tree synthesis, routing, analysis and signoff. While each step required the design team to take some account of the multi-voltage nature of the design, this paper focuses on design planning and static timing analysis.
Note that Synopsys now offers tool features specifically targeted at multi-$V_{DD}$ designs. Because these tools were not available to the ULTRA926 team, this project used methodologies that are now included in the latest tool revisions.

6. Design Planning

The implementation of multiple $V_{DD}$ domains in the ULTRA926 chip require that the domains be planned with separate power grids and include the ability to power-down a grid altogether to eliminate leakage power. Note that multiple supply voltages must be provided either through separate power pins or by analog voltage regulators that are integrated into the device. The ULTRA926 chip uses the former approach.

Completely powering-down a logic domain requires the use of power isolation cells, because the outputs from a powered-down section into an active power domain should never be allowed to float. Power isolation logic ensures that all inputs to the active power domain are clamped to a stable value.

To meet system requirements with multiple voltage domains, it is necessary to evaluate whether interfaces between different domains require level shifters (for signals) and/or power isolation cells. Additionally, a state-retention technique may be required in blocks that are powered-down so that these blocks can resume operation when powered-up. Powering-down various domains’ voltages or scaling their voltages dynamically may also require power-sequencing circuitry to ensure correct operation of the chip. The processor core in the ULTRA926 chip can be powered-down, but the chip’s internal RAM is always powered so that it can save the processor state.

The multi-voltage concept can range from a set of fixed voltages to a fully adaptive approach. In between is a dynamic approach in which the voltage is scaled to predetermined levels, with no regard to the actual silicon performance. The adaptive approach uses the hardware performance monitors described earlier to ensure that voltage levels meet performance targets rather than simply predetermined levels that should work for most implementations. Note that these alternatives can be combined in a single SoC and include low-leakage/high-speed tradeoff methodologies.

Both level shifters and isolation cells created design planning issues that the ULTRA926 team had to handle. For level shifters, the cell height differed from that of the other standard cells, so the level shifters were placed manually between power domains. Isolation cells had to be placed at the right voltage domains, so both cell orientation and location were important.

7. Static Timing Analysis

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While traditional sign-off requires the use of a best- and worst-case corner value around a nominal timing corner, multi-voltage designs have many more corners. The design's various regions have different libraries, different and/or variable operating voltages and different operating conditions. Thus, timing varies from one voltage value to another and from one block to another. Multiple STA runs are therefore needed to cover all the possible corners.

The design was implemented in UMC L130E HS FSG process. Two Liberty timing models are provided with the standard Foundry design kit for the LF027 core.

Worst case for static timing analysis of setup times and output settling times (design critical paths):
- 1.2V - 10% = 1.08V
- 125 degrees C (commercial grade hot)
- slow-slow process corner

Best case for static timing analysis of hold times and input arrival times (to fix any race conditions):
- 1.2V + 10% = 1.32V
- -40 degrees C (commercial grade cold)
- fast-fast process corner

Based on the system requirements to process workloads, the following voltage and frequency points were used:

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Latency (max) (ns)</th>
<th>Latency (min) (ns)</th>
<th>Latency Spread (ns)</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.730</td>
<td>slow/slow</td>
<td>7721</td>
<td>3826</td>
<td>3237</td>
<td>0.389</td>
<td>129.5</td>
</tr>
<tr>
<td>0.800</td>
<td>slow/slow</td>
<td>6198</td>
<td>2963</td>
<td>2635</td>
<td>0.327</td>
<td>161.3</td>
</tr>
<tr>
<td>0.940</td>
<td>slow/slow</td>
<td>4442</td>
<td>2187</td>
<td>1931</td>
<td>0.256</td>
<td>225.1</td>
</tr>
<tr>
<td>1.080</td>
<td>slow/slow</td>
<td>3472</td>
<td>1741</td>
<td>1531</td>
<td>0.210</td>
<td>288.0</td>
</tr>
<tr>
<td>1.320</td>
<td>slow/slow</td>
<td>2645</td>
<td>1333</td>
<td>1162</td>
<td>0.171</td>
<td>378.1</td>
</tr>
</tbody>
</table>

Table 1

Due to the wide spread in both timing characteristics and buffer tree latencies, the typical process, room temperature and nominal 1.2V operating voltage are useful to understand for voltage scaling. The latency variations in the above table bring out the impact of scaling voltages on the clock tree within the ARM926 core.

Besides the intra voltage domain STA, the timing analysis required careful analysis of paths across the 3 voltage domains:

1. SoC level from and to ARM926 Core
2. SoC level from and to the RAM (tightly coupled memories - TCM)
3. ARM926 Core from and to the RAM

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For paths 1 and 2 above, this was achieved by running the ARM926 Core and the RAM (TCM) at 6x (288 MHz/1.08V), 5x (240 MHz/0.95V), 4x (192 MHz/0.85V) and 3x (144 MHz/0.8V) of the AHB clock (48 MHz/1.08V). The retiming interface between the SoC level domain and the scaled voltage domains (ARM926/RAMs) was designed to account for the skew/delay variation resulting from the scaled voltage points.

The paths between the ARM926 Core from and to the TCM were timed with the above corner points. Even though both the voltage domains operated at the same voltage level, the clock tree segments were separately built, and to account for any variation in skew resulting from differences in the clock tree topology, it was essential to run STA across the 2 interfaces at each operating voltage point.

\(^3\) When the ARM926 core is in the active state the core and RAM domains are at the same voltage, but the core domain can be switched off completely whilst the RAM domain remains powered to save processor state.
Energy efficient SOC design technology and methodology

Table 2 shows the other corner values for the ULTRA926 design. The operating voltage points for the ARM926 core and the RAM move together, although the ARM core can also be powered-down completely while the RAM cannot. Each of the sets of values in the table requires a separate STA run. Additionally, timing analysis begins with a base STA run at the process’s highest voltage (1.32V for the UMC 130nm process) for all blocks to check the design’s best timing.

<table>
<thead>
<tr>
<th>Corner</th>
<th>Soc Level</th>
<th>ARM Core</th>
<th>RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>WC</td>
<td>1.32V, 125C, SS</td>
<td>1.32V, 125C, SS</td>
<td>1.32V, 125C, SS</td>
</tr>
<tr>
<td>WC</td>
<td>1.2V, 125C, SS</td>
<td>1.2V, 125C, SS</td>
<td>1.2V, 125C, SS</td>
</tr>
<tr>
<td>WC</td>
<td>1.08V, 125C, SS</td>
<td>1.08V, 125C, SS</td>
<td>1.08V, 125C, SS</td>
</tr>
<tr>
<td>WC</td>
<td>0.92V, 125C, SS</td>
<td>0.92V, 125C, SS</td>
<td>0.92V, 125C, SS</td>
</tr>
<tr>
<td>WC</td>
<td>0.80V, 125C, SS</td>
<td>0.80V, 125C, SS</td>
<td>0.80V, 125C, SS</td>
</tr>
<tr>
<td>WC</td>
<td>0.75V, 125C, SS</td>
<td>0.75V, 125C, SS</td>
<td>0.75V, 125C, SS</td>
</tr>
<tr>
<td>BC</td>
<td>1.32V, -40C, FF</td>
<td>1.32V, -40C, FF</td>
<td>1.32V, -40C, FF</td>
</tr>
<tr>
<td>BC</td>
<td>1.20V, -40C, FF</td>
<td>1.20V, -40C, FF</td>
<td>1.20V, -40C, FF</td>
</tr>
<tr>
<td>BC</td>
<td>1.08V, -40C, FF</td>
<td>1.08V, -40C, FF</td>
<td>1.08V, -40C, FF</td>
</tr>
<tr>
<td>BC</td>
<td>0.92V, -40C, FF</td>
<td>0.92V, -40C, FF</td>
<td>0.92V, -40C, FF</td>
</tr>
<tr>
<td>BC</td>
<td>0.80V, -40C, FF</td>
<td>0.80V, -40C, FF</td>
<td>0.80V, -40C, FF</td>
</tr>
<tr>
<td>BC</td>
<td>0.75V, -40C, FF</td>
<td>0.75V, -40C, FF</td>
<td>0.75V, -40C, FF</td>
</tr>
</tbody>
</table>

Table 2 STA corner values

Dynamic Voltage and Frequency Scaling in the ULTRA926 required the following clocks and control logic in the design:

- Free running AMBA clocks for AHB HCLK (also serves as APB PCLK in this design). This runs continuously and the processor and debug clocks are phase-aligned to this primary clock. All the synthesizable memory controllers and peripherals use this primary clock in the SOC design.
- Independent target processor clock frequency required to support Adaptive Power controller module with the frequency under the control of an external (asynchronous) dynamic power controller. This target frequency is set by the Intelligent Energy Controller to the desired processor frequency and used as a part of the voltage control feedback loop to determine if the voltage is sufficient to safely support operation at this target performance level.
- Dynamically switching, glitch-free CPU clock carefully controlled to align with AHB transfer HCLK edges using HCLKEN enable. The CPU frequency is independently switched in frequency under control of the Intelligent Energy Controller in a phase-aligned manner to the free-running AMBA clock.
- Power management protocol support for isolation (interface signal clamping) and CPU sequencing and synchronous de-assertion of reset.

One of the key challenges in the design was to meet timing requirements on specific paths from the DVFS control logic (at the SoC level) to the ARM926 core / TCM.
memory macro because of the spread between the setup and hold margins on certain pins on ARM926 timing models and the memory timing models inside the TCM. The hold requirement dictated the final operating frequency of the interface. As the ARM926 and the TCMs were scaled down in voltage, the increase in the hold requirement due to increase in clock latency inside these blocks required the reset sequencing and the clamp control signaling to operate at a lower frequency.

Multi Voltage STA was performed using PrimeTime. PrimeTime provides several features that simplify multi-voltage analysis and signoff. Though instance specific operating conditions could be applied to this design, with the given libraries that were characterized for each voltage corner, a link-path per instance approach was used to setup the operating conditions for the cells that ran on different rail voltages.

A set of NLDM libraries, one library per operating point as described in Table 2 was used during STA. Because NLDM libraries have limited accuracy for multi-rail cells, each library used was characterized at the required PVT to run STA.

To specify different NLDM library cells for different instances in the design the following is required. Set the variable link_path_per_instance to a list. Each list element consists of a list of instances and the corresponding link paths that override the default link path for each of those instances. An example is provided below.

```
pt_shell> set link_path_per_instance [list
    [list "U_ULTRA_SOC"
    [list "U_ULTRA_SOC/U_ARM" "umc_130_hs_0.9_slow"
    [list "U_ULTRA_SOC/U_TCM" "umc_130_hs_0.8_slow"]]
```

The listed instances in the case of the ULTRA926 were the hierarchical blocks that represent individual voltage islands.

The STA was very similar to a single voltage run. The cells were also applied the operating conditions that were part of the library that the cells were linked into.

PrimeTime STA uses the input slew, output load, and operating conditions of each cell to calculate slew and delay for the cell. It also reports transition times in terms of local-library thresholds.

To check the settings, the command `report_cell` lists the specific operating conditions for each cell along with the supply voltage information, and `report_port` lists the conditions for each port. For further setup analysis, the shell command `check_timing -signal_level-verbose` finds nets for which the driver signal level matches the load signal level. Since this command reports violating driver/load pairs, it shows nets where the user might need to insert level shifters. This feature also makes it possible to diagnose inconsistencies based on input_voltage and output_voltage groups and inconsistencies based on rail voltages or input/output `signal_level`.

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8. Conclusions

By combining key technology from five collaborating companies we have implemented ULTRA926—a technology demonstration vehicle that will show how energy savings of up to 60 percent may be achieved with the UMC 130nm fabrication process. This level of energy savings is vitally necessary to enable SoC designers to increase battery life while supplying the desired functionality in mobile and hand-held devices. The technology described here allows the industry to migrate to smaller process geometries, where power and thermal-management would otherwise pose significant hazards.

9. Acknowledgements

The authors would like to thank the many people at the five partner companies whose hard work and dedication made the implementation of the ULTRA926 device possible.

Special thanks should also go to the SNUG reviewers for their kind guidance during the writing of this paper.
Appendix B. External non-confidential publications

A. Analyses for the ARM926EJS_1616 core

ARM926EJS_1616 Frequency and Voltage analysis

The ARM926EJS_1616 processor core was synthesized for a 288MHz target frequency – for 1.2V – 10% voltage tolerance, slow silicon worst case temperature. Detailed PathMill simulations were performed at different operating process/voltage/temperature points to allow the characteristic for dynamic voltage and frequency scaling to be derived. This is required to work out what frequencies are energy efficient in the overall system-on-chip design.

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Process</th>
<th>Period (ns)</th>
<th>Fmax (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.730</td>
<td>ss</td>
<td>7.721</td>
<td>129.5</td>
</tr>
<tr>
<td>0.800</td>
<td>ss</td>
<td>6.198</td>
<td>161.3</td>
</tr>
<tr>
<td>0.940</td>
<td>ss</td>
<td>4.442</td>
<td>225.1</td>
</tr>
<tr>
<td>1.080</td>
<td>ss</td>
<td>3.472</td>
<td>288.0</td>
</tr>
<tr>
<td>1.320</td>
<td>ss</td>
<td>2.645</td>
<td>378.1</td>
</tr>
<tr>
<td>0.660</td>
<td>tt</td>
<td>6.172</td>
<td>162.0</td>
</tr>
<tr>
<td>0.730</td>
<td>tt</td>
<td>4.803</td>
<td>208.2</td>
</tr>
<tr>
<td>0.800</td>
<td>tt</td>
<td>3.920</td>
<td>255.1</td>
</tr>
<tr>
<td>0.940</td>
<td>tt</td>
<td>2.896</td>
<td>345.3</td>
</tr>
<tr>
<td>1.080</td>
<td>tt</td>
<td>2.357</td>
<td>424.3</td>
</tr>
<tr>
<td>1.200</td>
<td>tt</td>
<td>2.075</td>
<td>481.9</td>
</tr>
<tr>
<td>1.320</td>
<td>tt</td>
<td>1.882</td>
<td>531.3</td>
</tr>
<tr>
<td>0.730</td>
<td>ff</td>
<td>3.287</td>
<td>304.2</td>
</tr>
<tr>
<td>0.940</td>
<td>ff</td>
<td>2.100</td>
<td>476.2</td>
</tr>
<tr>
<td>1.320</td>
<td>ff</td>
<td>1.468</td>
<td>681.2</td>
</tr>
</tbody>
</table>

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Frequency Analysis

![Frequency Analysis Graph](image)

**ARM926EJS_1616 Dynamic Power**

The following dynamic power values for ARM926EJS_1616 were obtained from nanosim simulations using a range of $V_{DD}$ values. All simulations were carried out at 25degC using typical SPICE models for the UMC 130nm HS process. The simulations used a standard “Dhrystone” vector set running with a clock frequency of 10MHz, and average power was measured during the fourth dhrystone loop in these vectors (by which time the instruction sequence is loaded into the cache). These figures exclude leakage current.

<table>
<thead>
<tr>
<th>$V_{DD}$</th>
<th>Average Current</th>
<th>Average Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75v</td>
<td>193.2uA/MHz</td>
<td>144.9uW/MHz</td>
</tr>
<tr>
<td>0.90v</td>
<td>237.2uA/MHz</td>
<td>213.5uW/MHz</td>
</tr>
<tr>
<td>1.08v</td>
<td>291.8uA/MHz</td>
<td>315.1uW/MHz</td>
</tr>
<tr>
<td>1.20v</td>
<td>333.1uA/MHz</td>
<td>399.7uW/MHz</td>
</tr>
<tr>
<td>1.32v</td>
<td>372.7uA/MHz</td>
<td>491.9uW/MHz</td>
</tr>
</tbody>
</table>

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Appendix B: External non-confidential publications

![Average vdd current](image)

![Average power](image)

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ARM926EJS_1616 Leakage Power

Leakage current was measured by running nanosim in highest accuracy mode, and recording $V_{DD}$ current at $t=0$. It is appreciated that leakage current is state-dependent, but previous experiments have shown that this method gives fairly consistent results when measurements are taken at different times in the simulation. Once again these simulations were run using the typical models at 25degC.

<table>
<thead>
<tr>
<th>$V_{DD}$</th>
<th>Leakage Current</th>
<th>Leakage Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75v</td>
<td>512.7uA</td>
<td>384.5uW</td>
</tr>
<tr>
<td>0.90v</td>
<td>680.4uA</td>
<td>612.4uW</td>
</tr>
<tr>
<td>1.08v</td>
<td>955.9uA</td>
<td>1032.4uW</td>
</tr>
<tr>
<td>1.20v</td>
<td>1201.5uA</td>
<td>1441.8uW</td>
</tr>
<tr>
<td>1.32v</td>
<td>1517.6uA</td>
<td>2003.2uW</td>
</tr>
</tbody>
</table>

VDD 0.75v 0.90v 1.08v 1.20v 1.32v

Leakage current vs vdd

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Leakage power vs vdd

![Graph showing leakage power vs vdd](image-url)
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ARM926EJS_1616 Open-loop (DVFS) and Closed-loop (AVS) Energy analysis

The worst case frequency analysis sets the operating frequencies for the system-on-chip design. In this case a set of fixed frequency dividers was chosen to avoid significant phase-locked-loop relock delays.

The frequencies selected are:

<table>
<thead>
<tr>
<th>Performance Level</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>288</td>
</tr>
<tr>
<td>83%</td>
<td>240</td>
</tr>
<tr>
<td>67%</td>
<td>192</td>
</tr>
<tr>
<td>50%</td>
<td>144</td>
</tr>
<tr>
<td>0%</td>
<td>0</td>
</tr>
</tbody>
</table>

Using the worst-case frequency analysis the minimum voltages required to operate the processor relative to the worst-case 1.08V FMax 288MHz are derived and interpolated.

Energy to complete a task is the product of the power to complete the task at a particular frequency and voltage and the time or duration to complete the task. The open-loop voltage scaled power and duration for workloads are derived graphically from the simulation analysis to predict the typical silicon/room temperature energy savings for table look-up power supplies able to support worst case process and temperature.

Finally the analysis of predicted energy savings when using the on-chip Adaptive Voltage Scaling closed-loop control is also shown in the graph below. The effect of reducing voltage to match the process and temperature for typical silicon at room temperature is derived from the typical silicon voltage and power analysis. Note that in this case the energy efficiency at the lowest performance point (144MHz) is in fact no better than at 192MHz because there is no voltage headroom left for typical silicon and the lower dynamic power at 144/192MHz is counteracted by the 192/144 scaling in duration to complete the task.

For all the predicted energy savings a safe operating margin must be added for safe operation and IR-drop effects. However by referencing all the savings back to 1.08V WC rather than a nominal 1.20V operating point the relative savings for real-world power supply tolerance are not unduly optimistic.
Appendix B: External non-confidential publications

Voltage headroom/Energy savings (compared to WC 1.08V 125C)
Energy efficient SOC design technology and methodology
System Design for Leakage Mitigation

Fast Track to Low Power

David Flynn
ARM Fellow, Cambridge R&D
ARM Ltd.

Leakage Mitigation

- Leakage mitigation is a SYSTEM-level problem
  - OS + software policies
    - Entry/Exit energy/real-time cost functions
  - Control IP roadmap for Intelligent Energy Manager (IEM)
    - IP interface/partitioning enhancements to facilitate clean control
  - EDA challenge
    - Implementation/verification and significant analysis issues
  - Physical IP
    - Additional standard cells, enhanced RAM, power gates
  - External Power supply control IP etc...
    - Voltage scaling and well bias
Appendix B: External non-confidential publications

Joint Best Practice MV Reference Designs

- **ARM926EJ-S™ technology-based IEM SoC**
  - Dual 16K caches, performance-tuned leakage-managed CPU system
  - Linux support platform (SDRAM/Flash/Peripherals integrated)
  - IEM controller enhanced for leakage/back-bias control (plus DVFS)
- **Target technologies (TSMC)**
  - "Generic" 90nm 1-volt, good performance but leaky process technology
  - "Low Leakage" 65nm 1.2V portable lower performance technology
- **Multiple implementation approaches**
  - Shared Header switches on 90nm, intra-cell Footer switches at 65nm
- **Lots of “science experiments” for real-world analysis**
  - Support detailed evaluation of power gating and state retention quality
  - Representative MV design exploration vehicle with Synopsys

Technology Demonstrator Results So Far...

- **Four primary levels of IEM leakage management:**
  - HALT/SRPG/SCAN-HIBERNATE plus SHUTDOWN for CPU
- **Working 65nm LP silicon evaluated (see on ARM Booth)**
  - Supports DVFS for IEM dynamic energy saving
  - important with 1.2V LP
  - SRPG Savings of 85%+ measurable
  - compared to the static ~0.3mW leakage
- **90nm G project just out of fabrication**
  - Distributed header power gating with inrush control
  - Dynamic threshold scaling leakage management
  - Both CPU plus USB subsystem leakage management
  - State retention noise immunity and safety measurement analysis
Energy efficient SOC design technology and methodology

What ARM's Customers Need...

- Help architecting “sleep” states onto SRPG technology
  - Evaluating the leakage savings versus design complexity
  - Evaluating the real-time costs for entry & exit from deeper sleep states
  - Evaluating the energy-savings achievable depending on usage profiles
  - What to do in the RTL...

- Physical IP components that work well with tools
  - Extra components to support Power gating, Isolation and State retention

- Proven implementation and verification methodologies
  - Power Gating is just as much Multi-Voltage design as Dynamic Voltage Scaling
  - Anything that reduces risk in production
  - Better design-for-battery-life support a.s.a.p.
Aggressive Leakage Management for ARM Based Systems

Alan Gibbons
Synopsys Inc.

David Flynn
ARM Ltd.

Agenda

- Overview of ARM’s Intelligent Energy Manager (IEM) technology
- Leakage power challenge and mitigation techniques
- Synopsys-ARM Technology Demonstrator (SALT)
- Driving new capability into ARM IP and Synopsys’ Galaxy Design Platform
- Summary
Energy efficient SOC design technology and methodology

What Consumers Care About

- Users want more features in their mobile devices
  - MP3, Camera, Video, GPS...
- But also need long battery life
  - Convenient form factor, affordable price
- Battery technology is not evolving fast enough!
  - Need to conserve energy

The Performance vs. Power Dilemma

Maintain Battery Life
- Wireless handheld
  - Lowest leakage and/or dynamic power

Increase Performance
- 3D Graphics / Multimedia
  - Thermal management
  - Packaging, cooling, cost

Lower Cost
- 130nm, 90nm, 65nm Technology

Increased leakage
- IR-drop
- Electromigration
Appendix B: External non-confidential publications

Power Dissipation

\[ E = \int_0^t (CV^2_{DD} f_e + V_{DD} I_{Irk}) dt \]

Total Power Dissipation

\[ \int_0^t V_{DD} I_{Irk} dt \]
Static Power Dissipation

\[ \int_0^t CV^2_{DD} f_e dt \]
Dynamic Power Dissipation

- Minimize \( I_{Irk} \) by:
  - Reducing operating voltage
  - Fewer leaking transistors

- Minimize \( I_{switch} \) by:
  - Reducing operating voltage
  - Less switching capacitance
  - Less switching activity

Improving Dynamic Energy Efficiency

- Dynamic Frequency Scaling (DFS)
  - Reduce operating frequency if possible
  - Reduces average power (but not task energy)
  - Eliminates NOPs

- Dynamic Voltage & Frequency Scaling (DVFS)
  - Requires DFS
  - Reduces voltage if frequency is reduced
  - Reduces task energy
  - Based on characterized frequency – voltage pairs (lookup table)

- Adaptive Voltage Scaling (AVS)
  - Closed loop optimization of VDD at run-time
  - Can save energy even at fixed frequency
Energy efficient SOC design technology and methodology

**ARM IEM Technology**

- Hardware and software solution for energy management
- Dynamic control of voltage and frequency scaling.

- **IEM™** software connects to OS kernel and collects data.
- Multiple policies categorize the software workload.
- Prediction of future performance requirement is made.
- Suitable operating point (Voltage and Frequency) is set.

**ARM IEM Principles**

- Batteries have finite amounts of energy stored in them
- Running fast and then idling waste energy

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IEM System Implementation

Agenda

- Review of ARM's Intelligent Energy Manager (IEM) technology
- Leakage power challenge and mitigation techniques
- Synopsys-ARM Technology Demonstrator (SALT)
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Energy efficient SOC design technology and methodology

Trends in power dissipation

- Static power dissipation can not be ignored
  - It is significant at 90nm and dominant at 65nm
- Leakage currents are rising fast
  - Must be controlled by circuit design and optimization tools
- Transistors are not perfect switches
  - They always "leak" ®
  - Especially high performance (low Vt)
- Currently sub-threshold leakage ($I_s$) dominates
  - Multi-threshold and Power Gating most effective
- However gate leakage ($I_g$) is becoming significant
  - Mitigated by high K dielectric material?

Leakage Mitigation Challenges

- Leakage mitigation is a system-level problem
  - Operating System and software policies
    - Entry and exit procedures
    - Energy and real-time cost functions
  - Control IP
    - "Intelligent Leakage Control" (part of roadmap for IEM)
    - IP interface and partitioning enhancements to facilitate clean control
  - EDA challenge
    - Implementation and verification with support for in-depth analysis
  - Physical IP
    - Additional standard cells, enhanced memories, power gates
  - External Power supply control IP
    - Voltage scaling and well bias
  - Etc.
Some Leakage Mitigation Techniques

- Lower Operating Voltage
- Power Gating
- Multi Vt
- Cell sizing
- Non minimum size gate lengths
- VTCMOS
- Stack Effect

Power Gating: Coarse Grain vs. Fine Grain

- Fine grain: one switch per cell
  - Simple to implement
  - Large area overhead on cells
    - Switch adds 2-4x area of original cell
    - Clamps needed in every cell
    - Effect on timing easy to characterise

- Coarse grain: distributed switches shared by many cells
  - More complex to implement
  - Reduced area overhead
    - Switches are shared – so can be smaller
    - Clamps only needed at macro cell outputs
  - Effect on timing harder to characterise
  - Less performance impact
Energy efficient SOC design technology and methodology

State Retention Control

- IP design assumes explicit clock and reset in RTL coding
  - Implicit always-on power and state preservation between clocks
- Designer needs to add RTL control of SRPG sequencing
  - Typically as part of the clock/reset/test/isolation/power control per MV domain
  - Ideally transparent to the (legacy) RTL IP subsystem

Agenda

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Appendix B: External non-confidential publications

SALT - Technology Demonstrator

- ARM-Synopsys R&D partnership program
- ARM926EJ-S™ based system within integrated USB PHY and sub-system
- Support for AMBA®-based block hibernate and wake "Deep sleep"
- Real silicon (TSMC90G) for evaluation and further tool/IP development
- Linux OS platform using IEM 'policy stack' development environment

- Leakage Power Management
  - Coarse grain MTCMOS power gated CPU and USB core
  - Multiple Vt library
  - On-chip power-gating with PMOS header switches and retention registers – "light sleep"
  - Off-chip power-gating with scan-based save/restore to RAM – "deep sleep"
  - Dynamic threshold scaling

SALT Architecture

[Diagram of SALT Architecture]
Energy efficient SOC design technology and methodology

Power Gating Considerations

- Impact to design performance and size
  - Maintain design performance while gaining power savings
    - Coarse Grain MTCMOS with PMOS header switch
- Course grain power switches for leakage mitigation
  - Disconnect local power from global power via power gates (MTCMOS switches)
  - Different switch topologies possible (columns, rings)
    - Maximize control over voltage drop (regularly spaced columns of switches)
- System overhead of state retention
  - Protocol management for scheduling sleep states
  - Managing depth of sleep states
  - Energy impact of state save and restore
    - Intelligent reuse of existing scan structures to facilitate state saving
- Controlling wake-up
  - In-rush current management with synchronization of state save and device reset
    - Closed loop analog voltage sensing, coupled with extensive PrimeRail analysis

Processor Implementation

- Favour header switches for system reasons
  - Suit active-high interface protocols
  - Output isolation matches external power-down (deep sleep support)
  - Strained silicon offers potential for high-mobility P-channel devices
- Switch columns placed every 50\(\mu\)m
  - Starter columns every 10 switch columns (500\(\mu\)m)
  - Route start signal up and down "starter" columns
- State retention synthesis with Power Compiler™
  - All state retained within the CPU
- IR drop analysis with PrimeRail
  - IR drop analysis across switched power mesh
  - Power-on sequence analysis
Appendix B: External non-confidential publications

In-Rush Current Management

- Closed loop, sequenced power-up of the design
- Combination of regular and 'starter' switch columns
- Analog voltage-sense cell (Schmitt Trigger) for the Virtual-VDD supply rail. Generate a "Ready" signal when start-up voltage reaches 90%

- Power-Up Sequence Analysis (PrimeRail)
  - Rush current, wake-up time calculation and IR drop analysis
  - What-if analysis to fine tune power-up sequence

SALT Header Switch Columns
Determine Header Pitch

- Built a representative test circuit and ran lots of HSPICE
  - Varied the load and also the number of headers
  - Measured effects on signal-delay, IR drop and leakage.
- Layout sweet spot of 30 headers in a double height cell
  - Need header cell every 50um for <5% IR drop at 250MHz

AHB Based Scan-Hibernate

- Bus transaction based save & restore to memory
- Bus Master implements CRC-32 on the fly
- Useful diagnostic check for "soft errors" whilst power gated
  - Can be used to explore effects of in-rush current induced voltage drop
  - Could also be used to restore a check point
Appendix B: External non-confidential publications

Agenda

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ARM Power Management Kit (PMK)
Energy efficient SOC design technology and methodology

ARM Artisan™ Physical IP for ARM IEM

- IEM methodology optimizes energy consumption using DVFS
- ARM® Artisan® Physical IP used for implementation in Galaxy™
  - Power Management Kit to support power islands with different voltage levels and power down Standard cell library and memories optimized for dynamic and leakage power
  - Standard cells and memories characterized over extended operating range, including low voltages

Comprehensive Low Power Kit

<table>
<thead>
<tr>
<th>Feature</th>
<th>Dynamic Power Control</th>
<th>Leakage Power Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock gating standard cells</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>Voltage level shifters</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Extended operating range</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Multi VT support in standard cells</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power gates</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>Retention flip-flops</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>Back-bias support</td>
<td>-</td>
<td>✓</td>
</tr>
</tbody>
</table>

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Synopsys' Galaxy™ Low Power Design Platform

Galaxy™ Low Power Solution

RTL Synthesis
- Voltage aware power synthesis
- Power & Voltage aware test
- MTCMOS shutdown synthesis

Physical implementation
- Power-aware Placement
- Low-Power CTS
- Concurrent MCMM
- MTCMOS Shutdown

Verification & Analysis
- Power aware functional verification
- Static MV compliance checks
- Full chip power analysis
- Dynamic IR Drop & EM analysis
- In-rush current analysis
Energy efficient SOC design technology and methodology

Multi-Vt Leakage Optimization

- Gate Delay
  - Meet timing with lowest % of Low VT cells – It's all about the quality of timing optimizations

Supporting MTCMOS Power Gating

- Power gating representation
  - Library, RTL, constraints modeling
- Optimization
  - Power gating representation understood throughout flow
  - Leakage optimization
- Power gating verification
  - HDL syntax checker
  - Functional verification
  - Formal verification
Appendix B: External non-confidential publications

Implementation of MTCMOS Power Gating

- Inference of power intent from RTL
- Specification of power domains
- Mapping to a state retention style
- Always-on network synthesis
- Multi-voltage design planning
- Power gating switch cell placement
- Sleep net and always-on net buffering
- Power domain aware placement
- Multi-voltage placement optimization
- Rush current management
- Sleep/Wake timing protocol
- Static and dynamic IR drop analysis
- Multi-voltage design integrity

State Retention Synthesis

```bash
set target_library "retention.db"
set power_enable_power_gating true
read_verilog RTL.v
set_power_gating_style -type DRFF
circle

hookup_power_gating_ports
report_power_gating_style
```

Power Compiler Script Sample
Energy efficient SOC design technology and methodology

Predictable Power Synthesis

Power QoR during implementation is not enough, it must correlate @ signoff

Predictable Power Network Design

Low Power Design

MT-CMOS Planning

In-rush current analysis

IR-Drop Correlation

PNA: 150mV

Sign-off: 141mV
Appendix B: External non-confidential publications

PrimeRail Power-Up Analysis Flow

- Power management cell modeling
  - I-V curve characterization w/ HSPICE
  - Power-up sequence description
- Power net extraction and net merge
  - Extraction for both PG & virtual PG nets
  - Net merge with PM cell circuit model
- Rail analysis
  - Rush current, wake-up time calculation
  - Voltage drop analysis with rush current
- What-if analysis
  - Power-up sequence Vs. number of PM cells, peak current and peak voltage drop

Power Specification @ RTL

- Modeling Logical Power Domains @ RTL
  - Simulate power down of a block
  - Infer physical information such as power rail connection
  - Infer consistent constraints as early as possible.
  - Reason & Verify possible states of power networks.
  - Infer sub-circuit paths with targeted cell types to model “always on” structures
  - Manage this intent through the entire flow.

Synopsys Donates Technology for Low Power Design to Accellera Standards Organization

Technology Paves the Way to Help Customers Achieve Ultra Low Power IC Designs

ROSTIN (VIR: Calif., September 12, 2006) - Synopsys, Inc. (Nasdaq:SNPS), a world leader in semiconductor design software, today announced that it has donated power management technology to Accellera, the Electronic Design Automation (EDA) organization focused on electronic design automation standards. The donation includes power management components, SystemVerilog constructs, VDSL constructs, and the Switching Netlist Interface (SNI). The donation is in support of Accellera’s Ultra Low Power (ULP) technical subcommittee efforts. Under the unified leadership of Accellera’s ULP technical subcommittee, these groups are working together to produce an open and extensible standard for low power design by January 2007.
Energy efficient SOC design technology and methodology

Open Power Standards

Summary

- By working through a real comprehensive technology demonstrator we are now in an excellent position to:
  - Quantify the benefits of various leakage mitigation techniques in ARM based systems.
  - Enhance ARM’s Intelligent Energy Manager technology with support for leakage mitigation.
  - Drive increased automation into Synopsys' Galaxy Design Platform for the rapid implementation and deployment of high performance with low power ARM based system chips.
  - Provide a comprehensive low power physical IP portfolio through ARM’s Power Management Kit.
  - Define a set of best practices that provide a complete low power design solution based on open industry standards.
Appendix B: External non-confidential publications

SYNOPSYS®

Predictable Success
Energy efficient SOC design technology and methodology
Aggressive Leakage Management in ARM Based Systems

John Biggs - ARM
Alan Gibbons - Synopsys

ABSTRACT

The management of power consumption for battery life is widely considered to be the limiting factor in supporting the concurrent operation of high performance, complex applications on mobile platforms. At 65nm and below, minimizing the static power dissipation through aggressive techniques such as coarse grain MTCMOS power gating and threshold voltage scaling can yield these significant reductions in power consumption that are necessary. ARM and Synopsys have jointly developed a comprehensive low power technology demonstrator that employs these advanced low power techniques. Various alternative approaches to MTCMOS power gating and threshold voltage scaling are discussed together with a detailed description of the implementation flow and the results.

NOTE:
Although this was presented by a colleague in the research and development group, John Biggs, the primary content for the State Retention and Power Gating was provided by the Author (see the acknowledgment in Section 5.)

One of the Engineering Doctorate programme goals is to mentor and encourage others to present the R&D work to wider audiences.

In follow on, the Author co-presented a Tutorial (MC4) with Alan Gibbons at the San Jose Synopsys Users Group conference on April 2, 2007.
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1 Introduction

Managing the power dissipation of complex SoCs has been a prime design consideration for some years now. It is well understood that reducing both the peak and average power consumption will reduce the manufacturing and packaging costs as well as improve the reliability and battery life.

However, the thriving market for ever more sophisticated mobile wireless devices such as cell phones, media players, PDAs and cameras is placing ever increasing demands on the battery. Consumers want more and more features in their mobile devices but still demand a convenient form factor and long battery life. Unfortunately battery technology is not developing fast enough to meet this demand and this shortfall is what is driving the demand for cheap, low power, energy efficient SoCs.

1.1 Power Dissipation

There are three major sources of power dissipation in digital CMOS circuits and they can be broken down into dynamic power dissipation \( (P_{\text{switching}} + P_{\text{short-circuit}}) \) and leakage power dissipation \( (P_{\text{leakage}}) \) as summarized by equation (1).

\[
P_{\text{average}} = \frac{a C_L V_{DD}^2 f_{\text{clk}}}{P_{\text{switching}}} + \frac{V_{DD} I_{\text{SC}}}{P_{\text{short-circuit}}} + \frac{V_{DD} I_{\text{leak}}}{P_{\text{leakage}}}
\]

1.2 Dynamic Power

In order to minimise the dynamic power dissipation term of equation (1) then not only should the clock frequency \( (f_{\text{clk}}) \) be lowered but also the switching activity \( (a) \) and where possible the supply voltage \( (V_{DD}) \) should be reduced too.

One of the simplest ways to reduce the switching activity \( (a) \) is to inhibit registers from being clocked when it is known that their output will remain unchanged. In a typical SoC as much as 30% of the switching power is dissipated in the clock tree so this technique, known as Clock Gating (CG), can yield a significant saving in both power dissipation and energy consumption\(^1\).

As power is the rate of doing work then the average power dissipation of a system can be reduced by slowing the rate at which work is done. In practice this means lowering the clock frequency \( (f_{\text{clk}}) \) when the maximum system performance is not required. This technique, known as Dynamic Frequency Scaling (DFS), leads to a linear reduction in average power dissipation but unfortunately does not reduce the energy consumption for a given task as the work done remains a constant. For some very “leaky” processes, the total energy consumption may in fact increase due to spending longer in active mode.

However, if at the same time as reducing the clock frequency, the voltage is also reduced to a level that is just high enough to support this lowered clock frequency, then there is less work to do in charging the internal capacitances to the supply voltage \( (V_{DD}) \) and so less energy is consumed. This technique, known as Dynamic Voltage and Frequency Scaling (DVFS), leads to a quadratic reduction in energy consumption and a cubic reduction in average power dissipation\(^2\). It should be noted that, as it is not possible to dynamically scale the voltage and

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frequency instantaneously, there is some energy overhead in moving between the various performance levels.

1.3 Leakage Power

The other source of power dissipation is leakage power which is predominately due to the fact that transistors are not perfect switches and so can never be completely turned off.

Although leakage power used to be considered insignificant when compared to dynamic power at 90nm, it has become significant and at 65nm, it is dominant and so can no longer be ignored.

Leakage power is dissipated in both active mode and standby mode and the currents which go to make up the total leakage are increasing fast (Figure 1). In some applications, it may be more energy efficient to run fast and stop rather than to lower the voltage and frequency due to the high active leakage currents.

There are four main sources of leakage currents in a CMOS transistor (Figure 2)

1. Sub-threshold Leakage ($I_{\text{SUB}}$): the current which flows from the drain to the source current of a transistor operating in the weak inversion region.

2. Gate Leakage ($I_{\text{GATE}}$): the current which flows directly from the gate through the oxide to the substrate due to gate oxide tunneling and hot carrier injection.

3. Gate Induce Drain Leakage ($I_{\text{GIDL}}$): the current which flows from the drain to the substrate induced by a high field effect in the MOSFET drain caused by a high $V_{DG}$.

4. Reverse Bias Junction Leakage ($I_{\text{REV}}$): caused by minority carrier drift and generation of electron/hole pairs in the depletion regions.

Figure 1 - Trends in Power Dissipation$^{[3]}$

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\[ I_{\text{LEAK}} = I_{\text{SUB}} + I_{\text{GATE}} + I_{\text{GIDL}} + I_{\text{REV}} \] (2)

**Figure 2 - Components of leakage current in an NMOS transistor**

Of the various components which go to make up the total leakage current \( I_{\text{LEAK}} \) it is currently the sub-threshold leakage \( I_{\text{SUB}} \) which is dominant. However, the gate leakage \( I_{\text{GATE}} \) is becoming significant but may yet be mitigated by high K dielectric material such as TiO\(_x\) and TaO\(_x\).[4]

The most effective techniques for mitigating sub-threshold leakage are Power Gating and VTCMOS, both of which will be described later.

1.4 Leakage Power Mitigation Techniques

There are a number of leakage mitigation techniques available to reduce the various leakage currents in both active and standby mode[3]. Some techniques such as Dual \( V_T \) and VTCMOS rely on additional support in the manufacturing process to lower the leakage whilst others such as Power Gating and Stack Effect are stand-alone circuit techniques.

1.4.1 Lower \( V_{DD} \)

Again by referring to equation (1), it can be seen that leakage power will reduce with the lowering of the supply voltage \( (V_{DD}) \). However, any reduction in \( V_{DD} \) also reduces \( V_{GS} \) which impacts the MOSFET gate drive \((V_{GS}-V_T)\). It can be seen from equation (3) that a reduction in \((V_{GS}-V_T)\) significantly reduces the MOSFET’s drive strength \((I_{DS})\).

\[ I_{DS} = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T \right)^2 \] (3)

Some of this loss in performance can be regained by lowering the threshold voltage \((V_T)\) to restore the loss in gate drive, however lowering the threshold voltage \((V_T)\) results in an exponential increase in the sub-threshold leakage current \( I_{\text{SUB}} \) and hence overall the leakage power increases - see equation (4). So, in order to manage the overall leakage power, the number of high leakage low \( V_T \) transistors should be kept to a minimum

\[ I_{\text{SUB}} = \mu C_{ox} V_T^2 \frac{W}{L} \cdot e^{\frac{V_{GS}-V_T}{nV_T}} \cdot \left( 1 - e^{-\frac{V_D}{V_T}} \right) \] (4)

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1.4.2 Dual \( V_T \)

It is now quite common to use a “Dual \( V_T \)” flow during synthesis to ensure that the total number of low \( V_T \) transistors is kept to a minimum by only deploying low \( V_T \) cells when required.

This usually involves an initial synthesis targeting a prime library in the conventional manner followed by an optimization step targeting one (or more) additional libraries with differing thresholds\(^{[5]}\).

As more often than not there is a minimum performance which must be met before optimizing power then in practice this usually means targeting the high performance, high leakage library first and then relaxing back any cells not on the critical path by swapping them for their lower performing, lower leakage equivalents.

If however minimizing leakage is more important than achieving a minimum performance then this process can be done the other way around by targeting the low leakage library first and then swapping in higher performing, high leakage equivalents in speed critical areas.

1.4.3 Power Gating

A far more aggressive and effective technique for leakage mitigation is to simply cut the power supply to any inactive transistor.

Fundamentally, this is done by placing switches in the power network, the ground network, or both. However, the exact placement and sizing of these switches must be done with great care so as not to have an adverse impact on performance. These switches are known as “power gates” and can be distributed throughout the power/ground network in either a “coarse gain” or a “fine gain” manner.

**Fine Grain** power gating is when the switch is placed locally inside every standard cell in the library (Figure 3). Since this switch must supply worst case current required by the cell, it has to be quite large in order to not impact performance. In order to keep this area overhead to a minimum, fine grain power gates are usually implemented as “footer” switches in the ground as NMOS transistors have a lower on-resistance than PMOS and so will be smaller.

![Figure 3 – Fine Grain Power Gating](image-url)
Although the area overhead of each cell is quite large (often 2x-4x the size of the original cell), overall the area overhead of fine grain power gating will be much less as it is only necessary to power gate the high leakage, low threshold cells.

As not all cells are power gated and some will remain powered, it is important to ensure that the inputs to these cells do not float in order to avoid crowbar currents. This means that every power gated cell must have additional circuitry to “clamp” its outputs to a valid CMOS logic level. In the case of fine grain power gates this means adding a weak PMOS pull up on each output (Figure 3).

The key advantage of fine grain power gating is that the timing impact of the IR drop across the switch and the behavior of the clamp is easy to characterize as they are contained within the cell. This means that it is still possible to use a traditional design flow to deploy fine grain power gating although care must be taken over the routing of the sleep signal. However, the larger footprint of the power gated cells means that swapping between high threshold (non power gated) and low threshold (power gated) cells is more complex than that of the traditional Dual $V_T$ flow.

**Coarse Grain** power gating is when the switch is placed such that it is shared amongst a number of cells (Figure 4). The sizing of a coarse grain switch is much more difficult than a fine grain switch as the exact switching activity of the logic it supplies is not known and can only be estimated. Also, it is common to have distributed coarse grain power gating where the outputs of all the switches are joined to create a “virtual” power or ground. This just complicates the switch sizing calculations still further as each power gated cell is in fact fed by a number of switches connected in parallel.

![Figure 4 - Coarse Grain power Gating](image)

The size of a coarse grain switch will be much less than the sum of the equivalent fine grain switches of the logic it supplies. This is because for a given block of logic the switching activity will not only be far less than 100% but due to the propagation delay through the cells the...
switching activity will be distributed in time. As coarse grain power gating switches do not have the same area overhead as fine grain it is possible to use the slightly larger “PMOS “header” switch in the power supply instead. This not only has the advantage of a common ground plane but also means that the outputs of power gated blocks can be clamped to this common ground, which is convenient for multi voltage design. Also, with coarse grain power gating, not as many clamps are needed as they are only required at the block outputs rather than on every cell.

Unlike fine grain power gating, when the power is switched in coarse grain power gating, the power is disconnected from all logic, including the registers, resulting in the loss of all states. If state is to be preserved whilst the power is disconnected then it must be stored somewhere which is not power gated. Most commonly this is done locally to the registers by swapping in special “retention” registers which have an extra storage node that is separately powered. There are a number of retention register designs which trade off performance against area. Some use the existing slave latch as the storage node whilst others add an additional “balloon” latch storage node. However, they all require one or more extra control signals to save and restore the state[7].

The key advantage of retention registers is that they are simple to use and are very quick to save and restore state. This means that they have a relatively low energy cost of entering and leaving standby mode and so are often used to implement “light sleep”. However in order to minimize the leakage power of these retention registers during standby, it is important that the storage node and associated control signal buffering is implemented using high threshold low leakage transistors.

If very low standby leakage is required then it is possible to store the state in main memory and cut the power to all logic including the retention registers. However, this technique is more complex to implement and also takes much longer to save and restore state. This means that it has a higher energy cost of entering and leaving standby mode and so is more likely to be used to implement “deep sleep”.

One of the key challenges in power gating is managing the in-rush current when the power is reconnected. This in-rush current must be carefully controlled in order to avoid excessive IR drop in the power network as this could result in the collapse of the main power supply and loss of the retained state.

In summary, although fine grain power gating is easier to implement, it has the disadvantage of requiring a completely new cell library with the integrated power gates which have a significant area impact. Coarse grain power gating on the other hand is more complex to implement and verify[7]. It may require special tooling but has the advantage of less area overhead and only requires the addition of retention registers, isolation clamps and power gates to the library.

1.4.4 VTCMOS

Variable Threshold CMOS (VTCMOS) is another very effective way of mitigating standby leakage power. By taking advantage of the body effect and reverse biasing the substrate, it is possible to reduce the standby leakage by up to three orders of magnitude. However, VTCMOS adds complexity to the library views and requires two additional power networks to separately control the voltage applied to the wells. Unfortunately, the effectiveness of reverse body bias has been shown to be decreasing with scaling technology[9].
1.4.5 Stack Effect

The Stack Effect, or self reverse bias, can help to reduce sub-threshold leakage when more than one transistor in the stack is turned off. This is primarily because the small amount of sub-threshold leakage causes the intermediate nodes between the stacked transistors to float away from the power/ground rail. The reduced body-source potential (more This results in a slightly negative gate-source drain voltage (which reduces the sub-threshold leakage) as well as a reduced drain-source potential (less DIBL) which, together with body effect), increases the threshold, again lowering leakage. The leakage of a two transistor stack has been shown to be an order of magnitude less than that of a single transistor[10]. Also this stacking effect makes the leakage of a logic gate highly dependant on its inputs and so there is a minimum leakage state for a particular circuit which could be applied just prior to halting the clocks.

1.4.6 Long Channel Devices

Using non-minimum length channels will reduce the active leakage as well as standby leakage by avoiding the $V_T$ roll off that occurs in short channel devices. Unfortunately, long channel devices have larger area and therefore greater gate capacitance which has an adverse effect of performance and dynamic power consumption. This means that there may not be a reduction in total power dissipation unless the switching activity of the long channels is low. Therefore, switching activity must be taken into account when choosing gates whose transistor lengths are to be increased. However, the properties of long channel devices make them very suitable for the implementation of power gates.

2 Synopsys ARM Leakage Technology Demonstrator

Synopsys and ARM have a long history of working together on lowering the barriers to the adoption of advanced methodologies for the rapid deployment of ARM synthesizable IP with Synopsys tools[2][3][11][12][13].

The Synopsys ARM Leakage Technology demonstrator known as “SALT” was an R&D collaboration implemented in TSMC90G to explore the practical details of implementing some of the more aggressive leakage mitigation techniques described above. Specifically we chose to implement Coarse Grain Power Gating together with Dual $V_T$ and VTCMOS as these techniques are the most effective at combating standby leakage power dissipation in the 90nm node.

2.1 SALT Design

The design of the SALT technology demonstrator was based on an established ARM926EJS reference system[3] with the addition of a prototype next generation Intelligent Energy Controller (“IEC”) for leakage control and an Synopsys DesignWare OTG PHY (Figure 5). The ARM926EJS was partitioned into two voltage domains to allow the RAMs to remain powered whilst the core logic was switched off. The design also implemented in-rush current management with a “soft-start” to avoid any adverse IR drop in the power supply during start up.

The SALT design has support for four levels of standby leakage power management:

1. Halt – simple stopping of the clocks.
Appendix B: External non-confidential publications

2. **Light Sleep** – the CPU is power gated and the state retained in retention registers.

3. **Deep Sleep** – the CPU is switched off and the state retained in RAM

4. **Shutdown** – both CPU and RAM are switched off so the state is not retained.

The sequencing of the various control signals for entering and leaving these sleep modes is managed by the Intelligent Energy Controller ("IEC").

The implementation of Deep Sleep uses a novel scan based technique together with a dedicated AMBA bus master to store the state in any AHB connected memory. This will be described in more detail later.

![Diagram of SALT Architecture](attachment:image.png)

**Figure 5 - SALT Architecture**

### 2.2 SALT Library

The SALT technology demonstrator targeted an experimental "R&D" library based on Artisan’s SAGE-X standard cell library in TSMC90G process. In order to support VTCMOS it was necessary to target a triple well process and add deep well to each cell. Also it was decided to add an extra 10th track supplying true V_DD to the top of each cell in the library in order to simplify the distribution of the un-switched power to the "always on" buffers and retention registers. In addition to these modifications, a power management kit consisting of the following cells was also created, drawn to the same standard cell rules:
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- **Power gates** to disconnect the power from the logic.
- **Isolation Clamps** to preserve CMOS logic levels on the power gated outputs
- **Always On Buffers** to drive power management signals, clocks and reset.
- **Retention Registers** to retain the state whilst power gated.
- **Schmitt Trigger** for in-rush current management.
- **Well Ties and Deep nwell End Caps** for VTCMOS support

The power gates were implemented as PMOS “headers” in order to have a common ground plane and also so active high power gated outputs get clamped inactive when isolated.

To use the deep nwell layer, it was necessary to also create a set of physical only deep nwell capping cells. These must be placed around the standard cell region to ensure that there is sufficient nwell overlap of deep nwell at the ends of each standard cell row to meet the design rules.

Finally this new “R&D” experimental library was recharacterised at lower voltage to account for the estimated IR drop across the PMOS “header” switches.

This collection of additional cells became known as a “Power Management Kit” and formed the basis of a prototype library which has now been productized (without the 10th track!) as ARM’s PMK.

### 2.3 SALT Implementation

The implementation employed the 2005.09 XG Galaxy design platform and the flow was largely based on the ARM Synopsys IEM Reference Methodology which extends the standard ARM Synopsys Galaxy Reference methodology to have support for multiple voltage domains and dual $V_T$. The only additional functionality that was required over and above this flow was the ability to perform state retention synthesis, size and place the power gates, implement the in-rush current management circuitry and add deep nwell capping cells.

Although there was full support for state retention synthesis in the tools, the placement of the power gates, implementation of the in-rush current management and support for deep nwell were all somewhat manual steps.

In order to minimize the impact on the tools and flow it was decided to implement these power management cells as “physical only” cells which could be placed in Jupiter during the floor planning stage. This will be described in more detail later.

### 3 Key Implementation Challenges

#### 3.1 Power Gating

In coarse grain power gating there is a clear trade off between the size, number and spacing of the switches, simplistically the fewer there are the bigger they need to be. However, it is not quite as simple as that as some subtle short channel effects come into play. For example, increasing the gate length by a small percentage can significantly reduce the leakage current and the leakage per unit width generally goes down as the transistor width is reduced (Figure 6).
Appendix B: External non-confidential publications

After much simulation it was decided that a switch transistor of width 0.55\textmu m and length 0.13\textmu m (TSMC90G) provided a good trade-off between area and the $I_{ON}$ to $I_{OFF}$ ratio and so the power gates were built using multiple transistors of this size in parallel.

![Normalized leakage Vs W (PMOS, TT, 85C, L=0.1\textmu m)](image)

**Figure 6 – Leakage Current vs. Gate Width and Length (TSMC90G)**

For several reasons, not least layout convenience, the number of transistors in a power gate was chosen to be 30, so now the resistance ($R_{ON}$) was fixed the spacing could be determined. This was again done by running many HSPICE simulations on a representative test circuit varying the number of headers and the load that they were supplying. The effects on signal delay, IR drop and leakage were then measured. It was found that a power gate was required approximately every 50\textmu m in order to have less than a 5\% IR drop in the switched power supply at 250MHz.

The power gates were laid out as double height cells in such a way that they would easily stack in columns with all the vertical connectivity done by abutment. This meant there was enough room to integrate all the necessary re-buffering of the control signals. A script was then written to place these power gates in columns every 50\textmu m throughout the VCPU placement region (The 40 or so columns of header cells can be clearly seen in Figure 7).
Figure 7 - SALT926 CPU Floor Plan Showing Power Gates in Columns

Once the power gate network was sized and placed, extensive PrimeRail analysis was performed to verify the IR drop from the pads through the VDD mesh, and across the power gates. It was found to be 18mV, well within the 50mV budget (assuming a 20% switching activity).

3.2 In-Rush Current Management

The “soft start” was implemented by building two networks of power gates, a daisy chain of weak “starter” power gates and a network of full power gates. These were then linked by a Schmitt trigger which senses the level of the switched “virtual” $V_{DD}$ and, when the level reaches approximately 90% of the un-switched “true” $V_{DD}$, it engages the main power gate network and asserts a “ready” signal (Figure 8). The Schmitt trigger cell in the R&D experimental library also had an integrated AND function to gate in the SLEEP signal to ensure that the READY signal is de-asserted as soon as SLEEP is asserted with out having to wait for the virtual $V_{DD}$ network to discharge.
Figure 8 - Conceptual Representation Of In-Rush Current Management Circuit

The whole circuit was simulated using NanoSim to verify the in-rush current and switch on times. It was found that the maximum in-rush current was no more than 80mA and it took just under 100nS from de-asserting SLEEP to bring the switched "virtual" V_DD up to operating voltage and for the Schmitt trigger to fire and assert READY(Figure 9).
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Figure 9 - Soft Start

3.3 State Retention

The design of SALT employed aggressive coarse grain power gating to disconnect the power from both the ARM926EJS processor and the OTG USB core when in standby mode. However, to ensure a quick return from standby back into active mode, it is necessary to preserve the state whilst the power is gated. Two state retention techniques were implemented in SALT: one for “light” sleep, where the state was stored locally in retention registers, and the other for “deep” sleep, where the state was scanned out and stored in memory.

3.3.1 Retention Registers

For most designs it is not strictly necessary to preserve the contents of every storage element whilst in standby as only the salient “architectural” state needs to be preserved. In the case of the ARM926EJS, this essential state is in effect the state relating to the programmer’s model. However, unless this essential state is explicitly marked in the source RTL, it is very difficult to infer during implementation. In the SALT implementation it was decided to simply convert every register in the ARM926EJS into a retention register to ease the verification process.

This was done using Power Compiler in the following manner:

```bash
set power_enable_power_gating true
set_power_gating_style -type DRFF
set_power_gating_signal -type DRFF nrestore
compile_operation -scan
hookup_power_gating_ports -type DRFF -port_naming_style nrestore
```

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Appendix B: External non-confidential publications

As previously mentioned there are a number of styles of retention register design which trade off speed, power and area. The simplest design uses the existing slave latch as the storage node which must be kept powered during power gating and should be implemented using high threshold, low leakage transistors. However, although this design has a minimal area overhead and only requires one additional control signal, it does unfortunately suffer from a loss in performance due to the high threshold transistors of the storage node being on the data path. This performance impact can be avoided by keeping the high threshold, low leakage transistors off the data path by adding a “balloon” latch storage node off to one side. Although this design results in minimal impact on performance, there is an area overhead and unfortunately it requires two additional control signals.

The retention register used in SALT was a prototype of the one that is now available in ARM’s Power Management Kit. The design of this “PMK” retention register manages to retain the performance of the “balloon” style whilst having the same simple control as the “live slave” (Figure 10).

![Figure 10 - PMK Retention Register](image)

3.3.2 Scan Hibernate

In order to reduce the leakage still further the power to the ARM926EJS can be shut off completely. In this case, the state can not be stored locally in retention registers and must be stored elsewhere before the power is disconnected.

A novel bus transaction based technique was developed to save and restore state to any AHB connected memory. This technique (called “Scan Hibernate”) involved padding out the number of retention registers to ensure that the number was a multiple of 32 so that the state could be scanned out and presented in a series of 32 bit words to a dedicated AMBA bus master to be saved to memory (Figure 11). The design of this dedicated bus master included an implementation of the “CRC-32” algorithm to check the integrity of the restored data.
An interesting use of this “Scan Hibernate” system is to verify the integrity of the state restored from the retention registers. This can be done by storing the state to memory as well as the retention registers before entering light-sleep mode and then storing the restored state to memory immediately after return to active mode. By comparing the two images of the state from before and after power gating it is possible to verify whether any state got corrupted. This is a very useful diagnostic technique which can be used to explore the low voltage operation of the retention registers as well as the effects of in-rush current induced IR drop.

3.4 Variable Threshold CMOS (VTCMOS)

The implementation of VTCMOS requires a triple well process so that (assuming a p-type substrate) “deep” nwells can be placed under the pwells in order to isolate them from each other so that they can be held at different potentials. In addition to this extra process step, VTCMOS also requires a “tapless” library with floating wells so that special cells which have independent contact with the wells can be placed at regular intervals to set the body bias. These special well bias cells then need to be all connected together with two extra power meshes, V_{DDH} for the nwell and V_{SSB} for the pwell.

As all the power gates in SALT were arranged in columns placed at regular intervals, it was convenient to make the well bias connections by incorporating them into the layout of each power gate cell. This meant that the implementation of VTCMOS almost came for free as all the vertical connectivity of these extra power nets was done by abutment between each power gate cells just like the SLEEP signal in the in-rush current management.

To complete the VTCMOS implementation, it was necessary to place a ring of special deep nwell “capping” cells around the standard cell region in order to meet the minimum nwell overlap of deep nwell as prescribed by the TSMC90G rules.

4 Conclusions and Future Work

As we move down the process generations leakage currents are fast becoming a significant source of power dissipation in both active and standby modes. Various techniques for mitigating leakage power were investigated and Power Gating, Dual V_T and VTCMOS were found to be the most effective. These techniques were then explored in further in practical detail through an

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ongoing collaborative R&D program with Synopsys to investigate aggressive leakage mitigation techniques on ARM based systems. The first phase of this program was focused on understanding the technology and yielded the design described in this paper (which at the time of writing was still in fab). Being an R&D project, the demands of this design were a little ahead of the capabilities in both the tools and the library and so certain back roads had to be taken in order to complete the tape out. However many valuable lessons have been learned, some of which have already been factored into the latest releases of ARM’s Power Management Kit and Synopsys tools.

When the silicon comes back, we plan to investigate the real time impact and entry/exit energy costs of the various sleep modes in order to further develop the next generation “Intelligent Leakage Controller”. Also, we plan to verify the effectiveness of the in-rush current management by using the diagnostic features of the “scan hibernate” system as well as benefits of VTCMOS in both forward and back bias modes.

The second phase of this collaborative program is focused on defining a set of best practices for the rapid deployment of ARM IP with Synopsys tools to provide a complete low power design solution based on open industry standards for our mutual customers.

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6 References


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