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DSP-based servo drive
control for a limited-angle
torque motor

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HIGH PERFORMANCE DSP-BASED SERVO DRIVE CONTROL FOR A LIMITED-ANGLE TORQUE MOTOR

by

Yi ZHANG, B.Eng

A Doctoral Thesis Submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy of the Loughborough University

December 1997

Department of Electronics and Electrical Engineering LOUGHBOROUGH UNIVERSITY

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This thesis describes the analysis, design and implementation of a high performance DSP-based servo drive for a limited-angle torque motor used in thermal imaging applications.

A limited-angle torque motor is an electromagnetic actuator based on the Laws’ relay principle, and in the present application the rotation required was from $-10^\circ$ to $+10^\circ$ in 16 ms, with a flyback period of 4 ms. To ensure good quality picture reproduction, an exceptionally high linearity of $\pm 0.02^\circ$ was necessary throughout the forward sweep. In addition, the drive voltage to the exciting winding of the motor should be less than the $\pm 35$ V ceiling of the drive amplifier. A research survey shows that little literature was available, probably due to the commercial sensitivity of many of the applications for torque motors.

A detailed mathematical model of the motor drive, including high-order linear dynamics and the significant nonlinear characteristics, was developed to provide an insight into the overall system behaviour. The proposed control scheme uses a multi-compensator, multi-loop linear controller, to reshape substantially the motor response characteristic, with a non-linear adaptive gain-scheduled controller to compensate effectively for the nonlinear variations of the motor parameters. The scheme demonstrates that a demanding nonlinear control system may be conveniently analyzed and synthesized using frequency-domain methods, and that the design techniques may be reliably applied to similar electro-mechanical systems required to track a repetitive waveform.

A prototype drive system was designed, constructed and tested during the course of the research. The drive system comprises a DSP-based digital controller, a linear power amplifier and the feedback signal conditioning circuit necessary for the closed-loop control. A switch-mode amplifier was also built, evaluated and compared with the linear amplifier. It was shown that the overall performance of the linear amplifier was superior to that of the switch-mode amplifier for the present application. The
control software was developed using the structured programming method, with the continuous controller converted to digital form using the bilinear transform. The $\delta$-operator was used rather than the $z$-operator, since it is more advantageous for high speed sampling systems. The gain-scheduled control was implemented by developing a schedule table, which is controlled by the DSP program to update continuously the controller parameters in synchronism with the periodic scanning of the motor.

The experimental results show excellent agreement with the simulated results, with linearity of $\pm 0.05^\circ$ achieved throughout the forward sweep. Although this did not quite meet the very demanding specifications due to the limitations of the experimental drive system, it clearly demonstrates the effectiveness of the proposed control scheme.

The discrepancies between simulated and experimental results are analyzed and discussed, the control design method is reviewed, and detailed suggestions are presented for further work which may improve the drive performance.

**Keywords:** Limited-angle torque motor, servo drive, gain-scheduled control, DSP, digital controller, linear power amplifier, switched-mode amplifier
I would like to thank my Supervisor, Mr. Gordon Kettleborough, for his expert guidance, invaluable advice and great encouragement during the years of my research and the writing of this thesis. It is owing to his emphasis on the pragmatic approach by which the research should be carried out that satisfactory results have been achieved in both theoretical and experimental work. My sincere thanks for his strong recommendation for the scholarship awarded for this research. I will always be grateful to him for his profound understanding, long time support and friendship which not only enabled me to complete this work, but also helped me to overcome the enormous personal difficulties which I have encountered.

My deep gratitude must go to my Director of Research, Professor Ivor Smith, for his constructive comments and for the detailed discussions on many drafts he carefully read during the process of preparing the thesis. His enthusiasm and dedication greatly encouraged me to conclude the research with an improved overall presentation. My sincere thanks for his solid support for the scholarship awarded for the research. His kind assistance to me throughout these years will be gratefully remembered.

I would express my sincere thanks to the Department of Electronic and Electrical Engineering for the financial support for this research. I am also very grateful to Mr. S. K Jim and Coercive System Ltd., Rochester, Kent, UK, for the funding and the torque motor contributed for the research.

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Last but not least, my sincere immeasurable indebtedness goes to my wife Hui, our parents, my son Chen, my sister Jing and brother-in-law Feng, whose love, caring, endurance, understanding, and encouragement are unparalleled in the past decade, during which I was away from them for more than three years. It is this traditional family value and spirits that gave me the great strength and motivation to strive to complete my research.

We hold these truths to be self-evident, -- that all men are created equal; that they endowed by their Creator with certain unalienable rights; that among these are life, liberty, and the pursuit of happiness

- Thomas Jefferson
To my wife Hui,

our parents, my son Chen,

my sister Jing and brother-in-law Feng.
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<td>$A_o$</td>
<td>Open-loop voltage gain of the operational amplifiers</td>
</tr>
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<td>$A_{cl}$</td>
<td>Closed-loop gain</td>
</tr>
<tr>
<td>$D_{i, i=1 \text{ or } 2}$</td>
<td>Switch Duty ratio</td>
</tr>
<tr>
<td>$e_b$</td>
<td>Coil induced back e.m.f</td>
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<tr>
<td>$f_1$</td>
<td>Fundamental frequency</td>
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<tr>
<td>$f_{BO}$</td>
<td>Unity-gain frequency</td>
</tr>
<tr>
<td>$f_p$</td>
<td>Power bandwidth of the operational amplifier</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
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<tr>
<td>$GM$</td>
<td>Gain margin</td>
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<td>$G_{O}(s)$</td>
<td>Position lag compensator transfer function</td>
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<tr>
<td>$G_{I}(s)$</td>
<td>Current lead compensator transfer function</td>
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<td>$G_{L1}(s)$</td>
<td>First position lead compensator transfer function</td>
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<td>$G_{L2}(s)$</td>
<td>Second position lead compensator transfer function</td>
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<td>$G_{N}(s)$</td>
<td>Position notch compensator transfer function</td>
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<tr>
<td>$G_{I}(\delta)$</td>
<td>First-order gain scheduled controller transfer function</td>
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<td>$G_{O}(\delta)$</td>
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<td>$G_{I}(\delta)$</td>
<td>First-order gain scheduled $\delta$-controller transfer function</td>
</tr>
<tr>
<td>$i_o$</td>
<td>Converter/amplifier instantaneous output current</td>
</tr>
<tr>
<td>I</td>
<td>DC input current</td>
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<tr>
<td>$I_o$</td>
<td>Converter average output voltage</td>
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<tr>
<td>J</td>
<td>Rotor inertia</td>
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<tr>
<td>$K_b$</td>
<td>Back e.m.f coefficient</td>
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<tr>
<td>$K_f$</td>
<td>Frictional coefficient</td>
</tr>
<tr>
<td>$K_s$</td>
<td>Stiffness coefficient</td>
</tr>
<tr>
<td>$K_t$</td>
<td>Torque coefficient</td>
</tr>
<tr>
<td>$K_{el}$</td>
<td>Linear static current/displacement constant</td>
</tr>
<tr>
<td>$K_{ev}$</td>
<td>Linear static voltage/displacement constant</td>
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list of principal symbols

$K_v$  Adjustable gain amplification coefficient
$k(\theta)$  Varying parameter of the gain scheduled controller
$L$  Motor inductance
$n$  Rotor speed
$n_0, n_2, m_1, m_2$  Coefficients of the second-order continuous controller
$PM$  Phase margin
$p, q, r, d_1, d_2$  Coefficients of the second-order digitized controller
$R$  Motor resistance
$R_1$  Current sensing resistance
$SR$  Slew rate of the operational amplifier
$T$  Sample time
$T_f$  Frictional torque
$T_m$  Electro-magnetic motor torque
$t_{on}$  Switch turn on duration
$t_{off}$  Switch turn off duration
$T_s$  Stiffness torque
$T_{sw}$  Switching period
$\hat{V}_{tri}$  Peak value of the triangular carrier wave
$V_i$  Input voltage to the linear amplifier
$V_A$  Output of non-inverting power operational amplifier
$V_B$  Output of inverting power operational amplifier
$V_{AB}$  Voltage applied to the motor terminals
$V_{tri}$  Carrier wave
$V_c$  Converter DC control voltage
$\pm V_{cc}$  DC power supply to operational amplifier
$v_i$  Converter/amplifier instantaneous input voltage
$V_o$  Converter average output voltage
$v_o$  Converter/amplifier instantaneous output voltage
$\pm V_s$  DC voltage source supply to linear amplifier/switch-mode converter
$\omega$  Shift operator
$\Delta \omega$  Bandwidth near the gain crossover point
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<td>$\Delta t$</td>
<td>Blanking time of the bridge circuit</td>
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<tr>
<td>$\tau_m$</td>
<td>Motor mechanical time constant</td>
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<tr>
<td>$\tau_e$</td>
<td>Motor coil electrical time constant</td>
</tr>
<tr>
<td>$\tau_\theta$</td>
<td>Motor system time constant</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Delta operator</td>
</tr>
<tr>
<td>$\theta$</td>
<td>Rotor position displacement</td>
</tr>
<tr>
<td>$\xi$</td>
<td>Damping ratio</td>
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<tr>
<td>$\Delta T_m$</td>
<td>Net torque</td>
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<tr>
<td>$\omega_n$</td>
<td>Natural frequency</td>
</tr>
<tr>
<td>$\omega_{gc}$</td>
<td>Gain crossover frequency</td>
</tr>
<tr>
<td>$\omega_{pc}$</td>
<td>Phase crossover frequency</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular frequency</td>
</tr>
<tr>
<td>$\omega_{BW}$</td>
<td>Closed-loop bandwidth</td>
</tr>
<tr>
<td>$\omega_p$</td>
<td>Closed-loop resonant frequency</td>
</tr>
<tr>
<td>$\omega_o$</td>
<td>Corner frequency of the gain scheduled controller</td>
</tr>
</tbody>
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Chapter 1

Introduction

1.1 RESEARCH BACKGROUND

In servo systems, electrical rotary actuators play important roles in control, measurement and energy conversion. A great number of actuator designs exist, owing to the very wide range of applications and the fact that complete changes in the actuator structure are needed to achieve both economic and performance-optimum solutions in the different requirements. Actuators familiar to industrial engineers, apart from conventional DC and AC motors, include stepping motors, brushless DC motors, linear motors, etc., whose designs are based on well established electromagnetic theory and techniques [1,2,3], while their industrial applications are well documented [4,5]. A less familiar device, although widely used in aerospace and military equipment is the limited-angle torque motor, which converts small electrical signals into limited mechanical motion, which in turn operates a servo load such as a valve in a hydraulic system, or a mirror in an optical scanning system. In the absence of any nonlinearities, the magnitude and direction of the rotor deflection are directly proportional to the stator winding current and, due to the inherently high magnetic stiffness, the rotor returns to its equilibrium position when the current is removed. The torque motor described in this thesis is for use in thermal imaging applications, where the rotor must follow extremely accurately a fast-changing periodic reference.

There is a notable lack of published literature relating to the control of a limited-angle torque motor, although many publications consider electric drives required to tracking either a step or a ramp input [6,7,8,9,10,11]. In 1988, a control scheme, known as repetitive control [12], was proposed specifically for systems subject to a periodic reference. The idea was based on the internal model principle [13], which states that the output should follow the reference without a steady-state error when the controller incorporates a model of the reference. For example, no steady-state error follows a step change in the reference of a type 1 stable feedback system, as a result of the use
of an integrator 1/s, which is the transfer function model of the step function. However, when applied to repetitive control, the internal model principle does not guarantee control system stability. In fact, the inclusion of a delay element to represent the periodic function in the form of a transfer function has a detrimental effect on the stability. It was necessary to sacrifice ideal tracking, when the control system was modified, to ensure stability. The latest investigations using repetitive control [14,15] show that the addition of compensation networks and a periodic corrective filter can force accurate tracking, but only when the motor model has relatively slow and linear dynamics. No existing practical applications of repetitive control schemes were found in the publication survey conducted for this research.

An entirely different approach to controlling the motor used a conventional three-loop control scheme [16], but in practice this was only effective when a linear model was used for the motor, and the controller was designed essentially on a trial-and-error basis. To overcome the nonlinear variations that exist in the motor parameters, the earlier stage of the research introduced a deliberately-distorted waveform into a feedback loop, but even this failed to achieve the necessary control accuracy, due to insufficient dynamic compensation [17].

1.2 RESEARCH OBJECTIVE

The objective of this research is to develop a systematic engineering methodology, based on which a servo control system subject to a periodic reference can be synthesised conveniently and effectively, to design, construct and test a microprocessor-controlled prototype drive and to obtain experimental results, which are comparable to the simulated results and demonstrate a satisfactory performance. A pragmatically approach was strongly recommended and encouraged, such that the research should lead to visible results, which may be suited directly to engineering applications.
1.3 THESIS ORGANISATION

Chapter 2 introduces three main types of limited-motion actuator: the double-wound, the toroidal and the Laws' relay actuator. A detailed description is given of the Laws's relay principle, based on which the limited-angle torque motor is designed and constructed. The motor control specification for a typical application in thermal imaging is presented.

Chapter 3 describes the development of a detailed mathematical model for the actuator, which incorporates both the high-order linear dynamics and the significant nonlinear characteristics. Various experiments were conducted to obtain information on the various inter-relationships, and the block diagram representation is used to effectively model the motor. The accuracy of the model was validated by static and time response tests on the experimental motor.

Chapter 4 is devoted to the analysis, design and simulation of the drive control system. The control specification is analyzed in a manner by which the application requirements are linked to the control performance and design problems. The frequency response method and performance are outlined, with the system compensation schemes briefly reviewed. The proposed control scheme comprises two key elements: a multi-compensator and a multi-loop linear controller, to reshape substantially the motor response characteristic, and a nonlinear gain-scheduled controller, to compensate effectively for the nonlinear variations of the motor parameters which considerably degrade the control accuracy. The design is confirmed by both frequency-domain performance and time-domain simulations, using the control software Matlab/Simulink.

Chapter 5 analyzes the motor drive behaviour and establishes that, due to its four-quadrant capability and wide-bandwidth, a linear amplifier is suitable to drive the motor. The two main four-quadrant linear amplifiers, linear bipolar and bridge amplifiers, are described and compared. The amplifier performance characteristics are reviewed, with the emphasis on AC characteristics, since to a great extent these
determine the drive performance. A detailed description is given of the experimental amplifier developed for the prototype drive system using a pair of SGS power operational amplifiers L465.

Chapter 6 investigates the use of an H-bridge PWM switched-mode power amplifier as an alternative to the linear amplifier. The detailed analysis, based on an experimental amplifier designed and constructed during the course of the research, indicates that both the limitations of the system bandwidth due to the switching operation and the nonlinearity introduced by the dead time inherently associated with the bridge circuit, have a considerable effect on the drive performance. The comparisons between the linear and switch-mode power amplifier, lead to the conclusion that the linear power amplifier should be used because of its superior overall performance. A switched-mode amplifier may also be used, but only when the above shortcomings are overcome.

Chapter 7 describes in detail the controller hardware and software developed for implementing the proposed drive control system, with the TMS320E14 DSP being chosen as the core of the hardware. The circuits for analog-to-digital and digital-to-analog converters, the address decoder, multiplexer, feedback signal conditioning and various DSP on-chip peripherals are discussed. The continuous controller was converted into digital form using the bilinear transform with the $\delta$-operator, which has the overall advantage over the conventional $z$-operator when a fast sampling rate is used. The discrete gain-scheduled control is realized by developing a schedule table, which is stored in the DSP, and accessed by the control program to update continuously the controller parameters. The control software is designed using the structure programming methodology, with the source code written in the DSP assembly language. The assembled object code may be either programmed into the DSP on-chip EPROM, or downloaded from a PC under the TI DSP Development System for debugging and testing. The choice of the sample rate and its effect on the system performance are discussed.

Chapter 8 describes experimental studies on the motor drive control system, detailing
both the procedures used for tuning the multi-loop multi-compensator controller and the practical results obtained, and these are compared with the predicted results achieved in simulations. An additional current lead compensator is used to compensate for the lagging effect of the A/D converter (Zero-Order-Hold) ignored in the earlier theoretical investigation. Other practical aspects, such as the limited word-length representations for the continuous controller coefficients, and the computing time allocated for the individual digital compensators, are also discussed.

Conclusions, discussions and suggestions for further work appear in Chapter 9.
Chapter 2

Limited-Angle Torque Motor

This chapter briefly introduces the three main types of limited-motion actuators widely used in servo control systems. It discusses in detail the construction and operation of one of these types, the limited-angle torque motor, and describes the control specification required for the present application of thermal imaging.

2.1 INTRODUCTION TO LIMITED-MOTION ACTUATORS

Limited-motion actuators have been used widely in positional control servo systems [18,19,20,21]. While most of the applications are simple point-to-point tasks, there is an increasing need for actuators capable of positioning loads in 'an analogue way', in contrast to 'a binary way'. This is particularly true with rotary actuators, which are often required to move and position a load at any point of a pre-defined trajectory, or to operate a control valve in a linear manner. In high or medium torque applications, hydraulic or pneumatic actuators are more suitable than electric actuators [22], but in low torque applications (less than 1 kNm), electric actuators are usually preferred. Despite their lower torque and force per-unit size and weight, compared with their hydraulic and pneumatic counterparts, electromechanical actuators have obvious advantages, such as being both more economic and easily interfaced with control systems. In addition, bulky and costly pipework and other auxiliary equipment are not necessary.

Electric rotary actuators may be divided into two main categories:

1. those requiring a step-down gearbox transmission;
2. direct-drive devices.

Whereas type (1) actuators provide a higher output torque and power, type (2) actuators are quieter and are not subject to nonlinear effects such as backlash, gearbox friction, etc. Prominent among the various direct drive devices is the limited-motion
rotary actuator, which has been applied in various servo control systems [23,24,25].

The limited-motion rotary actuator is a device that can drive a load through a limited angle of deflection, usually less than $\pm 180^\circ$. Due to this property, it is also known as a limited angle torque motor, limited angle torquer, or even torque motor [26,27].

The three main types of limited-motion actuators rely on the polarized reluctance principle [28] and are shown in Fig. 2.1.

(a) the double-wound type [23,24] is used for large angular travel and has concentrated windings on both the stator and the rotor;
(b) the toroidal type [25] has a distributed winding on the stator and a permanent magnet rotor
(c) the Laws’ relay type [29] is used for small angular travel and has a coil and permanent magnet excitation on the stator, and a salient soft-iron rotor.

The device in this thesis is based on the Laws’ relay principle.

2.2 LAWS’ RELAY PRINCIPLE

2.2.1 Principle of Operation

The flux patterns for a Laws’ relay actuator are shown in Fig. 2.2, with two magnetic circuits carrying the flux produced by the pair of permanent magnets and another two carrying the flux produced by the control windings. In the equilibrium position, the rotor bridges the stator poles, thereby maintaining a state of magnetic balance in the four air gaps. When a current is applied to the control winding, the balance of the magnetic bridge is disturbed and the rotor moves to a new equilibrium position.

The control winding may be supplied from either a single-ended or a bipolar source. With a single-ended input, two control windings are series connected and the direction of the armature rotation is determined by the direction of the current flow. On no-
load the angle of rotation is proportional to the amplitude of the input current, while on load the armature rotates to a position at which the torque produced by the control current is equal and opposite to the applied load torque. With a bipolar supply, both the torque produced and the deflection are related to the difference between the currents flowing in each of two symmetric control windings. Since the torque output is proportional to the net current, it is possible to position accurately a load within the angular deflection range of the torque motor by controlling this current.

Full details of Laws' relay type actuators are described in the technical note 'An Electro-Mechanical Transducer with Permanent Magnet Polarisation' [29].

### 2.2.2 Description of Limited-angle Torque Motor

The design and construction of the limited-angle torque motor is based on the Laws’ relay principle. The motor, shown in Fig. 2.2, has a moving-iron rotor with a relatively low inertia, that rotates up to a maximum ±15° within a magnetic bridge formed by an exciting winding and rare-earth permanent magnets on the stator. Excitation of the stator winding causes an unbalance of the magnetic bridge, producing a resultant torque, with a magnitude and direction which are dependent upon the current and the angular position of the shaft.

In the experimental unit, a high accuracy brushless capacitive transducer with an extremely low inertia rotor was fitted to the shaft to sense the rotor position. The change in capacitance with position is converted into an electrical signal through a built-in electronic circuit, forming a signal conditioning module with a bandwidth of 5 kHz.

Fig. 2.3 is an engineering drawing of an experimental motor provided by Coercive System Ltd.. The specifications of the FSM-S526 Frame Scan Motor System consisting of the motor/transducer unit and the signal conditioning module, are given in Appendix A.
2.2.3 Stiffness

One of the principal features that distinguishes a limited-angle torque motor from a conventional electric motor is its inherent stiffness, which makes it particularly suitable for high performance servo control systems, such as aerospace servo-valve control, where fail safe operation is vital.

If the rotor of Fig. 2.2 is moved from the centre position, by means of an external force applied to the shaft, the unbalanced static fluxes that result produce a force opposing the external load in an attempt to restore the initial state of magnetic balance. The rotor will move to a new balance position dependent upon the magnetic restoring force and the applied external force. This magnetic restoring force is known as the stiffness and is measured in terms of torque per deflection angle.

Since the torque of a limited angle torque motor is a direct function of the control current, it can be measured at any point of the rotor deflection. This information is usually presented in terms of the torque/deflection characteristics of Fig. 2.4. It is evident from these that the slope of the characteristics at different levels of excitation is the same as that at zero-current, which represents the stiffness of the motor. It follows that any modification to the stiffness will result in a corresponding modification to the slope of the torque/deflection characteristic when energized. This modification may be made by adjusting the strength of the static magnetic field produced by the permanent magnets.

From the viewpoint of design, a primary factor to be considered when determining the motor stiffness is the nature and magnitude of the driven load. In most cases, the stiffness of the motor has to be such that the centralizing force is sufficient to overcome the combined effects of the stiffness of the controlled plant at any position in the range of deflection.
2.2.4 Dynamic Characteristics

As with other electric motors, the dynamic characteristics of a limited-angle torque motor may be described by the frequency response. The typical characteristic for a Laws’ relay actuator [29], shown in Fig. 2.5, has a flat low-pass property in the frequency range 0 - 10 Hz. This then falls at a slope of about 6 dB/octave in the mid-range from 10 to 150 Hz and exhibits a much higher resonant frequency of 100 - 300 Hz than usually occurs in a conventional motor. This implies that the actuator is ideal for high speed servo control systems.

Further investigations into various actuator parameters show that the frequency response changes with different operating conditions, such as the setting of the maximum deflection angle. This reflects the fact that the nonlinear parameter characteristics may significantly affect the dynamic characteristics and thereby influence the overall design of the control system. For the limited-angle torque motor provided by Coercive System Ltd., the performance characteristics, such as deflection/current, deflection/torque and hence torque/current can all be conveniently measured or inferred. Although these are static considerations, they provide direct information on the motor parameters.

Further detailed dynamic characteristics of the motor are investigated in the next chapter using more rigorous mathematical methods.

2.3 CONTROL SPECIFICATION

The control specification for the limited angle torque motor used in the present work relates to the specific application of thermal imaging, where a mirror is mounted on the rotor shaft and a light beam is projected onto the mirror. The rotor shaft is required to sweep through an angle from -10° to +10° in 16 ms, then fly back during the following 4 ms. The deflection cycle is then repeated, as shown in Fig. 2.6. This operation makes the light beam sweep over a screen in a similar way to the time base used in an oscilloscope. An exceptionally high linearity, ±0.2% of the
full scale deflection of $\pm 10^\circ$, is required for the linear sweep to ensure quality pictures. The scan efficiency is defined as the ratio of the time taken for the linear sweep and the cycle period, and for this application it should not be less than 80\%. i.e., 16 ms for the linear scanning and 4 ms for the flyback. This is extremely difficult to achieve, and imposes very stringent requirements on the drive control system. A thorough literature survey found little material published on this specific control subject, and the limited number of publications relating to the design and construction of the limited-angle torque motor were quoted previously.

In view of the specialized nature of the design methods and production techniques associated with torque motors, there has been a tendency for manufactures to guard against the publication of information which may be of use to competitors, and this tendency has led to a general lack of technical information that would aid research.
Chapter 2

Limited-Angle Torque Motor

Fig. 2.1 Three main types of direct drive limited-motion actuators

(a) Doubly-wound with concentrated windings

(b) Toroidal-state, PM rotor

(c) Laws relay
Fig. 2.2 Basic operational principle of Laws’ relay

Fig. 2.3 Full size illustration of a limited-angle torque motor
Fig. 2.4 Torque/deflection characteristics at various levels of excitation

Fig. 2.5 Typical frequency response characteristics of the Laws' relay
Fig. 2.6 The ideal rotor position waveform
Chapter 3

Motor System Modelling and Dynamic Analysis

A detailed mathematical model was developed to predict the dynamic behaviour of the torque motor. It is important that the model should be accurate, as it provides the basis for the design of the control system that must achieve precise control during the linear scanning period. This chapter describes both linear and a nonlinear models for the motor, with the transfer function based linear model being analyzed in both the time- and frequency-domains and providing a basic understanding of the dynamic characteristics. A block diagram representation was used to model the nonlinear system, which effectively combines both the linear high-order dynamics and nonlinear characteristics. Validation of this model was provided by careful experimental tests on the motor.

3.1 LINEAR MODELS

The equivalent circuit shown in Fig. 3.1 may be used to represent the limited-angle torque motor. The exciting coil is modelled as a series L/R circuit, with a voltage source $e_b$ representing the e.m.f generated in the coil due to rotor movement in the magnetic field.

Reference to Fig. 3.1 shows that the rotor position is controlled by the voltage $v_i$ applied to the exciting coil. Kirchhoff’s voltage law then gives

$$v_i = Ri + L \frac{di}{dt} + e_b$$  \hspace{1cm} (3.1)

or

$$\frac{di}{dt} = L^{-1}(v_i - e_b - Ri)$$  \hspace{1cm} (3.2)

The electromagnetic torque of the motor is
Chapter 3  

Motor System Modelling and Dynamic Analysis

\[ T_m = K_i \]  

(3.3)

and the generated e.m.f is

\[ e_b = K_b \frac{d\theta}{dt} = K_b n \]  

(3.4)

The mechanical equation is

\[ T_m = K_s \theta + K_f \frac{d\theta}{dt} + J \frac{d^2\theta}{dt^2} \]  

(3.5)

or

\[ \frac{d^2\theta}{dt^2} = J^{-1}(T_m - K_s \theta - K_f \frac{d\theta}{dt}) \]  

(3.6)

where

\[ \frac{d\theta}{dt} = n \]  

(3.7)

Eqns. (3.1) to (3.7) together form a model for the motor. If the state variables of the system are defined as \( i, n \) and \( \theta \), the above equations may be rewritten in the matrix form of Eqn. (3.8), which is the state equation model and comprises a set of first-order differential equations.

\[
\begin{bmatrix}
\frac{di}{dt} \\
\frac{dn}{dt} \\
\frac{d\theta}{dt}
\end{bmatrix} =
\begin{bmatrix}
\frac{R}{L} & -\frac{K_b}{L} & 0 \\
-K_s & -K_f & 0 \\
J & J & J
\end{bmatrix}
\begin{bmatrix}
i \\
n \\
\theta
\end{bmatrix}
+ \begin{bmatrix}
1 \\
0 \\
0
\end{bmatrix}
\]

(3.8)
Chapter 3  

Motor System Modelling and Dynamic Analysis

The corresponding state diagram of the motor is shown in Fig. 3.2. Using Mason’s formula [31], and with the initial states all set to zero, the overall transfer function between the motor position \( \theta(s) \) and the input voltage \( V(s) \) is obtained as

\[
\frac{\theta(s)}{V(s)} = \frac{K_t}{JLs^3 + (RJ + Kl)s^2 + (K_tK_b + K_JR + LK)s + K_JR} \quad (3.9)
\]

Alternatively, the block diagram representation shown in Fig. 3.3 may be deduced by taking Laplace Transforms of Eqns. (3.1) to (3.7). The advantage of using a block diagram is that it gives a clear insight into the interrelationships existing between each component of the motor system, and Fig. (3.3) has been used throughout the analysis and design of the control system.

The full mathematical model of the torque motor may be obtained by substituting the nominal parameters, given in Appendix A, into Eqns. (3.8) and (3.9) and Fig. 3.3, giving the state equation model of Eqn. (3.10), the overall transfer function model of Eqn. (3.11) and the block diagram transfer function model of Fig. 3.4 respectively.

\[
\begin{bmatrix}
\frac{di}{dt} \\
\frac{d\omega}{dt} \\
\frac{d\theta}{dt}
\end{bmatrix} =
\begin{bmatrix}
-3.5 \times 10^2 & -2.8 & 0 \\
4.2 \times 10^5 & -3.3 \times 10^5 & -8.3 \times 10^5 \\
0 & 1 & 0 
\end{bmatrix}
\begin{bmatrix}
i \\
\omega \\
\theta
\end{bmatrix} + 
\begin{bmatrix}
22.2 \\
0 \\
0
\end{bmatrix} v \quad (3.10)
\]

\[
G(s) = \frac{\theta(s)}{V(s)} = \frac{9259259.3}{s^3 + 688.9s^2 + 2109207.3s + 296296304.1} \quad (3.11)
\]
3.2 OVERALL TRANSFER FUNCTION MODEL ANALYSIS

The high-order transfer function for the linear model of the torque motor normally results in a complex analysis, due to difficulties in establishing analytical relationships relating the process performance with the system parameters. On the other hand, analytical expressions for first- and second-order systems are well defined [32]. An investigation was therefore made to determine if the high-order system could be approximated to by a low-order one. One possible method, termed the dominant pole approach [33], uses either one pole or a pair of poles that have dominant roles in the transient response performance, but these do not exist in the transfer function being investigated. Another reduced-order method [34] uses an equivalent low-order transfer function as an approximation, with the two systems having similar responses according to certain prescribed criteria. Unfortunately, it is not possible to achieve this with the motor transfer function. It was concluded therefore that a low-order approximation to the motor system was inappropriate, and that the original high-order model needed to be used in the control analysis and design.

The alternative to a reduced-order method is to consider the overall system to comprise a second-order system in cascade with a first-order system. The dynamic analysis is then based on the two individual low-order subsystems, in a process that is termed cascade decomposition. Eqn. (3.11) rewritten in the factorized form:

$$G(s) = \frac{9259259.3}{(s + 146)(s^2 + 542.9s + 2029982.9)}$$  \hspace{1cm} (3.12)

gives a transfer function of the motor system comprising a negative real pole, \( s = -146 \) and a pair of conjugate complex poles, \( s = -245 \pm 1299j \). Eqn. (3.12) may be divided into the two subsystems

$$G(s) = K_p G_1(s) G_2(s)$$  \hspace{1cm} (3.13)
where

\[ G_1(s) = \frac{4.6}{s + 146} \]  

and

\[ G_2(s) = \frac{2029982.9}{s^2 + 542.9s + 2029982.9} \]

Comparing the transfer functions of the prototype first-order and second-order subsystems, with the standard forms of Eqns. (3.16) and (3.17), shows that the system parameters are obtained as a natural oscillatory frequency \( \omega_n = 1424.8 \) rad/sec. and damping ratio \( \xi = 0.19 \), with a corner frequency \( \omega_c = 146 \) rad/s and a loop gain \( K_1 = 4.6 \), thus

\[ G_1(s) = \frac{K_1}{s + \omega_c} \]  

\[ G_2(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n + \omega_n^2} \]

Fig. 3.5 shows a block diagram comprising these two low-order subsystems, forming the equivalent overall transfer function.

The magnitude/frequency-response characteristics of the two low-order subsystems and the cascaded system representing the motor are given in Fig. 3.6. It is evident that the 3rd-order system is dominated mainly by the first-order subsystem, as both the DC gains and the corner frequencies are close, and comparison of Figs 3.6(a) and (c) shows that the resonant property of the second-order subsystem is retained, with a slightly decreased resonant frequency but a considerably attenuated resonant peak.
3.3 LINEAR MODEL TIME RESPONSE ANALYSIS

The dynamic characteristics of a torque motor may also be conveniently investigated via a time response simulation, for which the use of a block diagram model is most appropriate. Three standard test signals, i.e., step, ramp and sinusoidal were used to determine the system performance. A step response test reveals a great deal about the speed of response to an abrupt change in input and represents typical conditions in an actual control system, i.e., a sudden change in the speed demand or a load disturbance. A ramp response test shows how the system follows linear changes in input with time, while a sinusoidal test examines the response to a periodic input. The reference input to the motor in the present application is a combination of these three basic responses.

A block diagram representation of the torque motor incorporating three built-in internal feedback loops is shown in Fig. 3.8. The additional 'frictional torque loop' is derived from the block diagram of Fig. 3.4, to illustrate the detailed internal states of the motor. Due to the existence of the back e.m.f loop, it is impossible to separate the R-L electrical network from the mechanical network, preventing analysis of the individual blocks of the diagram.

When step, ramp and sinusoidal inputs are applied to the system of Fig. 3.7, the time response waveforms at various points are as shown in Figs. 3.8 to 3.10 respectively, based on which the dynamic characteristics of the linear model may be outlined as:

1. The torque motor is extremely fast-acting and capable of generating high instantaneous acceleration due to the large torque-to-inertia ratio $\Delta T_m/J$, where $\Delta T_m = T_m - T_s - T_f$. This may also be seen from the very small mechanical time constant $\tau_m = J/K_f = 3$ ms, which is comparable to the electrical time constant $\tau_e = L/R = 2.8$ ms. The inherently high mechanical resonant frequency and stiffness are valuable when the motor is used in high-speed and precise positional control.
(2) The torque motor possesses a low-pass electro-mechanical property that may be described by a first-order time-lag system. The step response of Fig. 3.8 shows a system time constant $\tau_e = 7.6$ ms, which is close to the 6.9 ms of the first-order system discussed in Section 3.2.1. The high-frequency response is observed by the oscillations superimposed on the exponentially rising waveform, and this may be accounted for by including a cascaded 2nd-order oscillatory component, which cannot be neglected in the present application.

(3) The response of the rotor is limited not only by the back e.m.f, but also by the L/R ratio of the control winding which prevents the current from reacting quickly to the input demand. This suggests that the current control mode should be introduced, so as to improve substantially the 'current following' capability.

(4) The torque response is dominated by the internal stiffness torque, and the frictional torque is relatively small. This indicates that the overall performance of the motor will be significantly affected by the stiffness characteristics.

(5) Both the current and position responses lag well behind the input voltage, suggesting strongly that the motor characteristics will need considerable compensation if it is to track accurately the sawtooth input waveform.

3.4 NONLINEAR STATIC CHARACTERISTICS

In the previous sections, various linear models for the torque motor were developed. Based on the transfer function model, the dynamic characteristics of the motor system were analyzed, using both frequency response and time response methods. However, to implement accurate control, the nonlinear characteristics that exist in the prototype motor must be taken into account. Both experimental measurements and further system simulations were therefore performed, to establish a nonlinear model for use in the control system design.
3.4.1 Ideal Static Characteristics

The ideal static characteristics of the motor may be obtained by setting the derivative terms of Eqns. (3.1), (3.3) and (3.5) to zero, giving

$$K_I = K_s \theta$$

(3.18)

and

$$I = \frac{V}{R}$$

(3.19)

where $V$ is the DC input voltage, $I$ is the steady state current, $\theta$ is the shaft position, and $R$, $K_s$ and $K_I$ are the winding resistance ($\Omega$), torque constant (Nm/A) and stiffness constant (Nm/rad), respectively.

Eqns. (3.18) and (3.19) show that the static characteristics depend on the motor parameters. With the nominal values given in Appendix A, the following linear relations exist

$$\theta = K_{\theta I} I$$

(3.20)

where $K_{\theta I} = 0.5 \text{ rad/A}$, and

$$\theta = K_{\theta V} V$$

(3.21)

where $K_{\theta V} = 0.033 \text{ rad/V}$

3.4.2 Nonlinear Static Characteristics

The nonlinear static characteristics may be determined experimentally by measuring the relationships between the input voltage, motor current, static stiffness torque and
output shaft position. The experimental procedure is described below.

(1) Relationships between input voltage, motor current and shaft position

With a variable DC voltage applied to the motor, readings of the input voltage, motor current, and shaft position are obtained as shown in Fig. 3.11. Fig. 3.12 illustrates the nonlinear relationship between the applied current and shaft position. An almost linear displacement with current is limited to about ±6°, after which the current required to produce a given increase in displacement increases rapidly.

The winding resistance $R$ can be determined from the slope of the V/I curve of Fig. 3.13, giving an experimental figure of 16.5Ω that is close to the design value of 16Ω presented in Appendix A.

(2) Relationship between magnetic stiffness and shaft position

The magnetic stiffness was measured using a spring balance attached to a shaft mounted pulley, as shown in Fig. 3.14. The variation of stiffness (i.e. torque/shaft angle) shown in Fig. 3.15 is clearly a nonlinear relationship above a displacement of ±6°. The stiffness coefficient is then no longer constant, and is considerably larger than the nominal value of 0.25 Nm/rad, given in Appendix A.

(3) Relationship between torque and current

Although the torque constant $K_t$ of the motor cannot be determined directly, combining Figs. 3.12 and 3.15 gives Fig. 3.16, which demonstrates an almost linear relation between the motor current and electro-magnetic torque.

3.4.3 Mathematical Description of Nonlinear Static Characteristics

An approximate mathematical expression was sought to include the nonlinearity in the dynamic model. The best fit to the experimental curve was found to have the form:
The coefficients of Eqn. (3.22) were determined using a computer program known as Easyplot, to give the relationship between magnetic stiffness and shaft position as

\[ T_s = \left( \frac{0.034 + 7.4 \theta^2}{1 - 5.7 \theta^2} \theta \right) \]  

(3.23)

where \( T_s \) Nm is the stiffness torque, due to the shaft angular displacement \( \theta \) rad. Fig. 3.17 shows an experimental curve, together with the relationship defined by Eqn. (3.23).

3.5 NONLINEAR MODEL

Based on the nonlinear static characteristics of the motor, which were experimentally measured and mathematically analyzed in the last section, further investigations were conducted to establish a nonlinear model capable of describing and predicting the dynamic behaviour of the motor.

3.5.1 Frequency Response Measurement

The nonlinear static characteristics discussed previously suggest that the dynamic characteristics of the motor model will also exhibit a nonlinear behaviour when subjected to a time-varying input signal. This is confirmed by a frequency response test, with a band of frequencies between 0 to 1000 Hz supplied to the motor, and the gain and phase difference between the input and the transducer output measured using a Frequency Spectrum Analyzer. Fig. 3.18(a) shows three such magnitude-frequency characteristics, and in Fig. 3.18(b) these are re-scaled to illustrate the noticeable differences in the low frequency range. The fact that the magnitude response curve drops with an increase in the amplitude of the input is typical nonlinear saturation behaviour; the response of a linear system will remain the same despite changes in
the input amplitude.

### 3.5.2 Nonlinear Dynamic Modelling [35,36]

The measured nonlinear static characteristics must be included in a nonlinear system model. An immediate difficulty that arises is how to deal with the linear dynamics of the remaining system, since, strictly speaking, the transfer function approach only applies to linear systems. If even one element in the system is nonlinear, the system may not be expressed by a transfer function. This difficulty is overcome by the use of the block diagram technique, which explicitly expresses various static and dynamic relationships in the form of individual blocks, connected through the system variables by the transfer functions, differential or state equations or mathematical functions. It may be derived directly from either the state diagram or signal flow graphs [8]. With the nonlinearities and dynamic effects separated, the nonlinear effects are lumped into one nonlinear block with no dynamics, i.e. the input to output relationship is the static characteristic of the nonlinearity. Equally, the dynamics of the system may be lumped into another block, which represents the linear differential or difference equations governing the dynamic behaviour.

The above idea was used to model the nonlinear motor. The constant stiffness $K_s$ was replaced by the nonlinear static function of Eqn. (3.23), and the experimentally obtained value was used for the torque constant, while the other dynamic blocks remain unchanged. This results in the block diagram model of Fig. 3.19, which is diagrammatically similar to, but conceptually different from, the linear block diagram model of Fig. 3.7. Retaining the form of the block diagram modelling the nonlinear dynamics makes it possible to design and simulate a multi-loop control system for the nonlinear motor, in the same manner as with a linear system, as described in the next chapter.

### 3.5.3 Verification of Nonlinear Dynamic Model

The nonlinear dynamic model was validated by comparing the experimental shaft
position response with that obtained from the dynamic model. The most important finding was that the static relation between the stiffness torque and shaft position is the major cause of the nonlinear dynamic behaviour. Fig. 3.20 shows the time response of the shaft position for both the simulated and experimental motor, which becomes increasingly distorted as the amplitude of the sinusoidal input increases. It is evident that the nonlinear model can describe the actual motor nonlinear behaviour with good accuracy.

It was found necessary to modify some of the motor parameters provided by the manufacturer (see Appendix A) to ensure that the results obtained were of acceptable accuracy. In particular, the estimated motor damping constant provided by the manufacturer was increased from $1 \times 10^{-4}$ Nm/rad/s to $2.5 \times 10^{-4}$ Nm/rad/s. In addition, the measured value of 0.1125 was used rather than the design value of 0.125 for both the torque and back emf constants $K_t$ and $K_b$. The close agreement between the static and predicted characteristics seen in Fig. 3.21 confirms the accuracy of the modelling.

3.6 PIECE-WISE LINEAR MODEL

The nonlinear model containing a single nonlinear element gave good agreement with the experimental results. For this type of nonlinearity, with a precisely defined mathematical description, it is possible to develop a set of piece-wise linear models in which the coefficients are determined by the various slopes at discrete points along the nonlinear curve. The full scale of the dynamic characteristics can then be described by different differential equations or transfer functions, according to the different operating conditions, for example in terms of the shaft displacement. The great advantage of this approach is that it enables the use of standard linear control methods, thus significantly simplifying the design process.

Fig. 3.22 gives a family of frequency response characteristics for the piece-wise linear models, obtained by approximating the continuous nonlinear function of Eqn. (3.23) by a sequence of piece-wise segments, with each slope representing the
estimated stiffness constant at the different shaft position. It shows clearly that the motor DC and low-frequency characteristics change considerably compared to the nominal model, due to the variations of the stiffness coefficients that are dependent on the shaft position. Therefore both the complex linear and nonlinear characteristics must be effectively compensated for and well controlled, in order to accurately track the 50 Hz sawtooth reference input, as described throughout the following chapters of this thesis.
Chapter 3  
Motor System Modelling and Dynamic Analysis

Fig. 3.1 Equivalent circuit for limited angle torque motor

Fig. 3.2 State diagram of limited angle torque motor
Fig. 3.3 Block diagram model of limited angle torque motor

Fig. 3.4 Block diagram model for limited angle torque motor with nominal parameter values
Fig. 3.5 Decomposition of overall transfer function into two low-order cascade subsystems
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Fig. 3.8 Time response to a step input
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Fig. 3.9 Time response to a ramp input
Fig. 3.9 Time response to a ramp input (continued)
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Fig. 3.10 Time response to a sine input
Fig. 3.10 Time response to a sine input (continued)
Fig. 3.11 Measurement of static characteristics
Fig. 3.12 Measured static I-θ characteristics

Fig. 3.13 Measured static V-I characteristics
Fig. 3.14 Experimental arrangement for static $T_o$ characteristics
Fig. 3.15 Measured static $T_s\theta$ characteristics

Fig. 3.16 Derived static $T_s$-I characteristics
Fig. 3.17 Best fit curve to the measured $T_r-\theta$ Characteristics
(a) Three measured magnitude characteristics

(b) Re-scaled plot showing variations of magnitude characteristics

Fig. 3.18 Motor frequency response measurement
(i) input peak = 12.6V
(ii) input peak = 16V
(iii) input peak = 20V
Nonlinear motor model incorporating nonlinear stiffness characteristics into linear model of Fig. 3.7

\[ T_s = \frac{0.034 + 7.4 \theta^2}{1 + 5.7 \theta^2} \]
Simulation of  motor

horizontal axis: 5ms/div
vertical axis: 3.5°/div

Experimental motor

(a) Input amplitude = 7V

Fig. 3.20 Verification of nonlinear model - comparisons of time response of the shaft position for both simulated and experimental motor with a 50Hz sine wave input
Simulated motor

Experimental motor

(b) Input amplitude = 12V

Fig. 3.20 Verification of nonlinear model - comparisons of time response of the shaft position for both simulated and experimental motor with a 50Hz sine wave input (continued)
Simulated motor

Experimental motor

(c) Input amplitude = 17V

Fig. 3.20 Verification of nonlinear model - comparisons of time response of the shaft position for both simulated and experimental motor with a 50Hz sine wave input (continued)
Fig. 3.21 Verification of nonlinear model - comparison of predicted and measured static V-θ characteristics

Fig. 3.22 Family of frequency response characteristics for the piece-wise linear models corresponding to

(i) $k_s = 0.05 \text{Nm/rad}$, (ii) $k_s = 0.1 \text{Nm/rad}$, (iii) $k_s = 0.2 \text{Nm/rad}$
(iv) $k_s = 0.25 \text{Nm/rad}$, (v) $k_s = 0.4 \text{Nm/rad}$, (vi) $k_s = 0.5 \text{Nm/rad}$
(vii) $k_s = 0.6 \text{Nm/rad}$, (viii) $k_s = 0.75 \text{Nm/rad}$, (ix) $k_s = 0.9 \text{Nm/rad}$
Chapter 4

Control Analysis, Design and Simulation

This chapter presents a detailed description of the drive control analysis and design. The proposed control scheme uses a multi-compensator, multi-loop linear controller to reshape substantially the motor response characteristics, which have both an inherent time-lag and oscillatory dynamics. An additional nonlinear gain-scheduled controller effectively compensates for the nonlinear variations of the motor parameters, and stability is ensured by the linear controller. The control system is designed using the frequency-domain method, and the effectiveness of the design is verified by extensive time-domain simulations using the control software Matlab/Simulink.

4.1 ANALYSIS OF THE CONTROL SPECIFICATIONS

The specification given in Chapter 2 requires the control system to be designed with an exceptionally high tracking capability. In each sweep cycle, the torque motor should follow the linear input reference from $-10^\circ$ to $+10^\circ$ for 16 ms, and then fly back from $+10^\circ$ to $-10^\circ$, with the time allowed for the flyback being 4 ms, as shown in Fig. 2.1. In the control system design, accurate tracking will inevitably require a high loop gain, and the fast flyback is achieved only with a satisfactory transient dynamic response. The flyback is the most critical part of the control, since not only must the motor shaft be driven from $+10^\circ$ to $-10^\circ$, but the other internal state variables, such as current and speed, must be controlled in an appropriate way. The current has to reverse sufficiently quickly to produce the electro-magnetic torque required for the reverse acceleration. Meanwhile, the speed has to reverse in direction and increase to a maximum, to ensure a fast flyback, and then reverse in direction again and reach a steady-state value before the shaft starts the linear sweep of the following cycle. As the control accuracy during the flyback is not required to be as high as that during the linear portion, the transient response may be such that, within the flyback interval of 4 ms, a position overshoot may be allowed, but the current and speed must fully recover to the states that ensure a linear sweep with the
defined accuracy for the following forward motion. Both the steady-state and the transient response, which usually conflict in the design problem [37], must be met at the same time and with little compromise. Furthermore, the control system should be sufficiently 'robust' to overcome the nonlinear motor parameter variations, and to withstand other possible un-modelled motor dynamics.

In the motor system modelling study of Chapter 3, it was shown that the open-loop motor is slow and sluggish in response to a basic 50 Hz sinusoidal input, and that the time response waveform is far from ideal. It was realized therefore that heavy dynamic compensation will be necessary to 'reshape' the motor characteristics, so that tight control is implemented throughout both forward and flyback motions and the specified waveform is obtained. There are three control requirements that should be emphasized at the design stage: (1) the linearity over the linear sweep between ±10° must be within the required accuracy of 0.02°; (2) the linear sweep must occupy 80% of the 20 ms cycle time, i.e. 16 ms; (3) the drive voltage should not exceed ±35 V.

Another important issue that needs to be understood is the system stability. The nature of the control requires the system to have a very large loop gain over a wide frequency range and, since this usually has a de-stabilizing effect, stability should be examined throughout the design process to ensure sufficient margin. Satisfactory relative stability also indicates the robustness of the control system.

In summary, the control specification imposes very demanding requirements on the control system in terms of high performance with respect to multi-constraints. The extensive design and simulation described below was therefore undertaken.

4.2 DESIGN METHODOLOGY

The experimental study of Chapter 3 established that the torque motor is a high-order dynamic nonlinear system, and the design in such cases largely depends on an understanding of the dynamics of the controlled process [35,36]. Initial experience had shown that it was even difficult to design a controller to achieve the required
tracking performance for the linear model, due to the nature of the motor dynamics and the demanding specification. It would therefore be very difficult to design a controller to cope with this highly nonlinear system, without appropriate dynamic compensation. However, the nonlinearity existing in the motor is mainly related to the varying stiffness with the position of the motor shaft, and a family of piecewise linear models was derived on an experimentally obtained nonlinear stiffness-position curve (see Chapter 3). By this means, the nonlinear system control may be converted into a linear system control, for which there are many well developed methods and techniques available for both analysis and synthesis [30,37,38].

The design problem was considered in two steps: (1) design a linear controller based on the nominal linear model and (2) introduce nonlinear control to improve and enhance the performance of the linear controller. In step (1) the linear controller compensates for the motor high-order dynamics, while in step (2) the required tracking performance is achieved with the added nonlinear controller. The main advantage of this two-step approach is that the stability of the overall system may conveniently be examined by using the piecewise linear model, and thus guaranteed when the nonlinear model is used in the time-domain analysis and simulation.

The frequency response method [30,38] was used for the linear controller design, since full information on the system stability, transient and steady-state response was available from the open-loop and closed-loop frequency responses. In particular, by manipulating the magnitude and phase response plot with respect to the same frequency variable, the Bode plot method provides the most effective and convenient way to synthesise a multi-loop, multi-compensator high-order system. Analytical relationships in complex cascade and/or feedback compensations effectively become simple arithmetic additions and subtractions on the logarithmic graphs [39,40.41].

For nonlinear control, a gain-scheduling adaptive control technique [42,43] is most suitable, as the quick reaction it provides for known nonlinearities is an important practical advantage. Other adaptive approaches, such as reference model adaptive control and self-tuning adaptive control [43.44] require on-line estimates of the motor
parameters, which unnecessarily complicate the control. Furthermore, based on a family of piece-wise linear motor models, the frequency response approach is equally applicable to the design of the nonlinear gain-scheduled controller.

The control system was analyzed, designed and simulated using the Matlab/Simulink software [45,46], which supports linear and nonlinear systems and models in continuous time, sampled time, or a hybrid of the two. It provides a graphical user interface for building models as block diagrams, and avoids the laborious work previously required to formulate both differential and difference equations in a programming language. The package includes a comprehensive block library of sinks, sources, linear and nonlinear components, and connectors, and it is also possible to create customized blocks for the user's special requirements. Time simulation is performed either from the Simulink menus or by entering commands in the command window of Matlab. The powerful model analysis tool enables design and simulation to be carried out simultaneously. The use of the linmod functions extracts the linearized model from the modelled system, which may then be analyzed and evaluated in either the time or the frequency-domain, resulting in an efficient design and simulation process.

4.3 PERFORMANCE SPECIFICATION

When designed in the frequency domain, the general performance specifications for a motor servo drive control systems, such as satisfactory transient and steady-state time responses, require the linear model described in Chapter 3 to be compensated to have the desirable frequency response discussed below.

4.3.1 Open-loop Frequency Response

The open-loop frequency response of the drive control system shown in Fig. 4.1 should satisfy the following requirements [32,47]:

(1) The magnitude response should cross the 0 dB axis with a slope of \(-20\) dB/
dec. The frequency band near the gain cross-over point, \((\Delta \omega = \omega_2 - \omega_1)\) should be sufficiently large to maintain system stability.

(2) The gain-crossover frequency \(\omega_{gc}\), at which the magnitude is equal to 0 dB, should be sufficiently high to ensure a fast response speed.

(3) The magnitude response in the DC and low frequency range should be sufficiently high to ensure a steady-state accuracy.

(4) The slope of the magnitude response in the high frequency range should ideally be at least \(-60 \text{ dB/dec.}\), to provide adequate attenuation of high frequency noise or disturbances.

(5) The phase margin \(PM\) (the phase corresponding to the gain-crossover point), and gain margin \(GM\) (the gain corresponding to the phase-crossover point, where the phase shift is \(-180^\circ\)), are generally independent, and should be adequately large (\(PM \geq 45^\circ\), and \(GM \geq 10\text{dB}\)) to guarantee the relative stability of the system.

4.3.2 Closed-loop Frequency Response

When the open-loop frequency response meets the required specification, the closed-loop frequency response shown in Fig. 4.2 should also satisfy the corresponding specification as follows:

(1) The closed-loop bandwidth \(\omega_{BW}\) (the frequency at which the frequency response has declined 3 dB from its DC or low frequency value), and the resonant frequency \(\omega_r\) (the frequency at which the maximum magnitude of the frequency response is attained), are sufficiently large to ensure a fast time response.

(2) The resonant peak value is within the value specified to ensure the relative
Chapter 4  

Control Analysis, Design and Simulation

stability.

(3) A fast cut-off rate ($\geq -60$ dB) provides good noises-filtering capability.

However, from the high-frequency noise considerations, the closed-loop bandwidth should not be excessively large, and the fast cut-off rate must be guaranteed for practical implementation.

4.3.4 Time Response

The control system is finally evaluated by the time-domain simulation against the control specification given in Section 4.1. The key time-domain variables, which are monitored in the simulation are position, current, drive voltage and position error, with position and current being the system feedback variables introduced to compensate for the motor dynamic characteristics. The drive voltage waveform indicates not only the effectiveness of the control efforts resulted from the compensation, but also the relative stability, with its magnitude in the critical flyback period limited to a maximum value of $\pm 35$ V. The position error, which is the difference between the reference position input and the actual position output, measures the closeness of the actual position tracking the reference input. If it is assumed that the reference position is an ideal linear ramp in the active scanning period (ie: a span of $\pm 10^\circ$ over 16 ms), the linearity of the actual position output may be conveniently measured by the position error, or alternatively the degree of the parallel of the actual position to the reference. In the following sections, the time-domain response waveforms of the above variables are simulated to evaluate the design performance.

4.3.5 Relationships Between the Frequency and Time Response

It is difficult to establish analytical relationships between the frequency-domain specification and the time specification for high-order systems, and the design is not straightforward as with low-order systems [30,37]. An iterative step-by-step approach
was therefore used, with the design carried out in the frequency-domain, then examined with respect to various frequency specifications, and finally tested and verified in the time-domain. The time-domain response performance is directly related to, though being analytically implicitly determined by, the frequency-domain response performance needed for control design.

The steady-state response of a DC servo drive is largely determined by the DC and low-frequency gains, whereas the control accuracy for the limited angle torque motor depends to a great degree on the gains of the open-loop frequency response over a wide frequency range. The requirements on the loop gains responsible for the steady-state accuracy should therefore be extended to medium range frequencies, for which a technical term 'low-medium frequency range' has been used when defining the frequency-domain performance. In order to follow an input reference signal effectively composed of many high-order harmonic components, the gain-crossover frequency will inevitably be high, to ensure both the response speed and stability of the system.

4.4 SYSTEM COMPENSATION

Compensation for the motor dynamics aims to achieve a satisfactory steady-state and transient response, and a satisfactory relative (or robust) stability for the nominal linear motor model, based on which adaptive nonlinear controllers may be 'safely' added to improve the system performance.

4.4.1 General Considerations

System compensation involves establishing a suitable feedback system configuration and using a number of compensators to reshape the motor dynamics to have a specified frequency response. When using the frequency-domain method, design considerations are given to [30,38,47]:

(1) The use of a cascaded multi-loop structure. This is often used in high
performance servo drive systems, since it improves the system stability and overall response performance by introducing linear gain state feedback, and/or dynamic state feedback.

(2) The use of feedback compensation. This is more effective than forward compensation for systems where the tracking performance is critical, and/or stability problems would arise from the use of the high gain usually associated with multi-compensators and required for high-accuracy servo control.

(3) A combination of forward and feedback compensation based on a cascaded multi-loop structure. This is capable of simultaneously improving both the steady-state accuracy and transient response, while retaining the overall system relative stability, and it is thus particularly suitable for systems that are subject to multi-restraints.

(4) A maximum robustness, which is very desirable because of the presence of the nonlinear stiffness. Robustness is measured by either the phase margin and gain margin, or the system sensitivity, to which particular attention should be paid.

4.4.2 Multi-loop Structures

Fig 4.3 shows a typical cascaded three-loop structure for the servo position drive control, which incorporates position, speed and current feedback. It is obviously advantageous that all the system variables are controlled through feedback, and therefore that a satisfactory performance may be achieved. On the other hand, the system cost increases as extra hardware and software are required for implementation. This problem may be overcome by using the alternative two-loop system shown in Fig. 4.4, which is simpler since only position and current are used as feedback variables. If both systems are able to meet the specification, the two-loop system will be preferable, as it requires less time for the control algorithm computation, and therefore the shorter sample period vital for digital control.
**4.4.3 Types of Compensator**

Table 4.1 summarises the transfer functions of the first- and second-order compensators that are commonly used in control systems.

**4.5 LINEAR CONTROLLER DESIGN**

The linear controller consists of a cascaded two-loop feedback system, a current loop and a position loop, with a number of compensators employed in the different loops.

**4.5.1 Current Loop Design**

The current loop is introduced to compensate for the motor characteristics, such that, in its open-loop frequency response, the gain crossover frequency is significantly raised, the gain and phase margins are sufficiently large, and the steady-state DC and low-medium frequency gains are adequately high. Ideally, the overall current loop should be compensated for effectively as a unity- or constant-gain device from the viewpoint of its equivalent closed-loop transfer function. Any simple gain adjustment will cause a decrease in the phase margin, and lead to a reduction in the stability, or even to instability.

To provide effective compensation, a lead compensator is placed in cascade with the motor, with the motor current used as the feedback to implement the internal current loop control, as shown in Fig. 4.5. The zero of the compensator is used to cancel the pole of the motor R-L circuit, and the pole and gain of the compensator are set to achieve the required stead-state and transient response. The transfer function of the lead compensator is

\[
G_{le}(s) = K_l \left( \frac{s + \omega_{il}}{s + \omega_{il_2}} \right)
\]  
(4.1)
Table 4.1 Type of Compensators and Main Functional Features

<table>
<thead>
<tr>
<th>Type</th>
<th>Transfer Function</th>
<th>Functional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>lead compensator</td>
<td>$G_l(s) = \frac{s+\omega_1}{s+\omega_2}$ if $\omega_1 &lt; \omega_2$ or $K_l \frac{\alpha T_l}{T_l} s + 1$ if $\alpha &gt; 1$</td>
<td>- increase gain crossover frequency</td>
</tr>
<tr>
<td>lag compensator</td>
<td>$G_g(s) = \frac{s+\omega_1}{s+\omega_2}$ if $\omega_1 &gt; \omega_2$ or $K_g \frac{\alpha T_g}{T_g} s + 1$ if $\alpha &lt; 1$</td>
<td>- increase loop gain</td>
</tr>
<tr>
<td>lead-lag compensator</td>
<td>$G_k(s) = K_l K_g \left( \frac{\alpha T_l}{T_l} s + 1 \right) \left( \frac{\beta T_g}{T_g} s + 1 \right)$ if $\alpha &gt; 1$ and $\beta &lt; 1$</td>
<td>- improve phase margin</td>
</tr>
<tr>
<td>notch compensator</td>
<td>$G_n(s) = \frac{s^2 + 2\xi\omega + \omega^2}{s^2 + 2\xi_p\omega + \omega^2}$ if $\xi &gt; 1$ or $(s+z_1)(s+z_2)$ if $(s+p_1)(s-p_2)$</td>
<td>- cancel undesirable structural resonance</td>
</tr>
</tbody>
</table>

- improve phase margin
- decrease, or increase gain-crossover frequency
- increase, or increase loop gain for a specified frequency range
- improve phase margin

60
and when $\omega_{i1}$ is chosen to equal $R/L$, $K_i$ is set as 6000, and $\omega_{i2}$ as $10\omega_1$. the open-loop and closed-loop frequency response characteristics are as in Figs. 4.6 and 4.7. for the compensated and uncompensated current loops. The gain-crossover frequency is increased by compensation from 186 rad/s to 125000 rad/s, and the new phase margin, although reduced to 94° from the previous 129°, is still sufficient to retain the required relative stability. The closed-loop bandwidth is increased from 165 rad/s to 75000 rad/s, indicating that the inner loop has been compensated as a constant system element. It is seen, however, that both the open-loop magnitude and phase response characteristics are considerably affected in the frequency range where an inherent electro-mechanical resonance exists in the motor. The resonant property of the motor is confirmed in the current loop time simulation, as shown in Fig. 4.8. This implies that, in order to control accurately the torque motor, further compensation is needed for the position loop system.

4.5.2 Position Loop Design

The position loop design involves using a number of different compensators, with the aim of simultaneously achieving satisfactory steady-state and transient performance.

Fig. 4.9 shows the frequency response characteristics for the open-loop position system, when only the inner current loop, together with a simple position loop gain, are incorporated. The gain-crossover frequency of 1541 rad/s is insufficient to ensure a fast transient response, the slope at the crossover point is $-40$ dB, and the phase margin is only $9^\circ$. An excessively large resonant peak exists in the closed-loop frequency response of Fig. 4.10, showing instability of the system.

4.5.2.1 Forward compensation

Fig. 4.11 shows the block diagram of the motor control system, which consists of an inner current loop and a position loop with a notch compensator, a first-stage lead compensator, a second-stage lead compensator and a lag compensator employed the forward path.
Notch and the first-stage lead compensator

A notch compensator is used in cascade with the first-stage lead compensator to compensate for the electro-mechanical resonance of the motor, and to increase the gain-crossover frequency and the phase margin. The zeros of the notch compensator, which are usually used to cancel the resonant poles of the plant, are designed here to provide an appropriate level of attenuation in the resonant frequency range (see Fig. 4.10). The poles are chosen to improve the phase margin at the gain-crossover frequency. Based on the notch compensation, the lead compensator is determined by realizing the maximum lead phase at the gain-crossover point, and achieving the specified DC and low-medium frequency response [30,45].

Second-stage lead compensator

A second-stage lead compensator is necessary to increase further the gain crossover frequency and the DC and low-medium frequency gains, and to improve the phase margin. It was achieved in a similar fashion to the first-stage lead compensator.

Lag compensation

One problem that arises from multi-stage lead compensation is that the increase in the loop gain is limited, due to the nature of the lead compensation [32]. A lag compensator is therefore used in cascade with the above compensators, to further raise the loop gain to achieve the high steady-state accuracy.

Fig. 4.12 gives a family of open-loop frequency response characteristics corresponding to the various different stages of the linear compensation as described above. These demonstrate clearly that the motor dynamic characteristics has been substantially reshaped in order to meet the demanding required frequency response requirements.

Figs. 4.13 to 4.15 show the time-domain simulations for the various linear
compensation schemes when the linear motor model is used. It is seen that the control performance in terms of the tracking error has been improved by adding more compensators to the position loop, and that the control system, employing a notch, two lead and one lag compensators, and characterized by Fig. 4.12 (curve v) gives a low position tracking error of 0.05°.

4.5.2.2 Feedback lead compensation

The frequency response characteristics of Fig. 4.12 indicates clearly that to control accurately the torque motor inevitably requires both a high gain-crossover frequency and a DC low-medium frequency loop gain in the open-loop magnitude response, and this normally results in a correspondingly high closed-loop bandwidth when only forward compensation is used. However, this closed-loop bandwidth cannot be too high, or any undesirable high-frequency noise will considerably affect the control performance when digital implementation is subject to a practically limited sample frequency. To overcome this, the second lead compensator is moved from the forward path to the feedback path, as shown in Fig. 4.16. The closed-loop magnitude response characteristics for the control systems of Figs. 4.11 and 4.16 are given in Fig. 4.17. Notably, while maintaining the open-loop frequency response shown in Fig. 4.12 (curve v), the closed-loop system bandwidth has been considerably reduced. It is also observed, from the time simulation of Fig. 4.18, that the drive voltage in the flyback is reduced, but that the position tracking error remains essentially unchanged.

4.5.3 Evaluation of Two-loop Control System Performance

To assist in evaluating the performance of the two-loop system using linear dynamic compensators, Table 4.2 summarizes the design procedure, with the constituents of the main performance specification achieved at the various stages.

Careful examination of the open-loop and closed-loop frequency response characteristics of Figs. 4.12 and 4.17 gives the following quantitative measures of the
control system.

In the open-loop frequency response,

- the open-loop magnitude frequency response intersects the 0 dB axis with a slope of $-20$ dB/decade;
- the gain crossover frequency $\omega_{gc}$ is 14240 rad/s;
- the frequency bandwidth about the gain cross-over point from $\omega_1$ (= 5050 rad/s) to $\omega_2$ (= 36060 rad/s) is 31010 rad/s;
- the DC gain is 95.86 dB, and the gain over the low-medium frequency range from 314 rad/s to 3140 rad/s is between 39.4 dB to 16.1 dB;
- the slope of the magnitude response in the high frequency range is $-60$ dB/decade;
- the phase margin $55^\circ$ and gain margin 15 dB;

In the closed-loop frequency response

- the bandwidth BW is 6300 rad/s;
- the resonance disappears, and the system is well damped;
- the cut-off rate is $-60$ dB/dec.

4.5.4 System Robustness Analysis Under the Nonlinear Motor Model

The robustness of the control system may be investigated by taking into account the severe case of a nonlinear variation in the motor stiffness coefficient $K_s$, identified in the earlier experimental study (see Chapter 3). A family of frequency responses was therefore obtained for the control system, with each response corresponding to one of the piecewise linear motor models developed in Chapter 3. The analysis tool *linmod* in Matlab/Simulink is capable of extracting a set of multiple linear models, and the resulting open-loop and closed-loop Bode plots are given in Fig. 4.19 and 4.20. The immediate observations are that the open-loop gain-crossover frequency, phase margin and gain margin all remain unchanged, despite variations in $K_s$ from
Table 4.2 Summary of Two-loop Control System Design and Performance

<table>
<thead>
<tr>
<th>Compensation</th>
<th>Performance Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>gain crossover frequency $\omega_{gc}$</td>
</tr>
<tr>
<td>1. a simple gain</td>
<td>1541 rad/s</td>
</tr>
<tr>
<td>2. notch + 1st lead in the forward path</td>
<td>4279 rad/s</td>
</tr>
<tr>
<td>3. notch + 1st lead + 2nd lead in forward path</td>
<td>9996 rad/s</td>
</tr>
<tr>
<td>4. notch + 1st lead + 2nd lead + lag in forward path</td>
<td>14240 rad/s</td>
</tr>
<tr>
<td>5. notch + 1st lead + lag in forward path, and 2nd lead in feedback path</td>
<td>14240 rad/s</td>
</tr>
</tbody>
</table>
0.05 Nm/rad to 0.9 Nm/rad (nominal value is 0.25 Nm/rad), and that the closed-loop frequency magnitude response also retains almost the same shape and magnitude as that of the nominal motor control system. This suggests that the system is insensitive to the nonlinear variations of the motor parameter stiffness $K_s$, and therefore that the response speed and relative stability of the control system are unaffected by the use of the nonlinear motor model. However, both the DC and low-medium frequency gain drop considerably with an increase in the stiffness, which indicates that the position tracking error is affected by the stiffness variations.

Verification of the above analysis was provided by the time simulations carried out with the nonlinear motor model, as shown in Fig. 4.21. It is seen that, in comparison with Fig. 4.18, the position error waveform reveals characteristics typical of nonlinear stiffness, with the tracking error increasing as the rotor moves towards the extreme positions of $\pm 10^\circ$, but becoming smaller near the equilibrium position. The maximum position error obtained is $0.09^\circ$, and the maximum drive voltage lies within the specified limit of $\pm 35$ V.

4.6 ADAPTIVE CONTROLLER DESIGN

4.6.1 Limitation of the Linear Controller

To obtain the required tracking performance, compensation is needed for the decrease in the loop gain over the DC and low-medium frequency range due to the increase in the stiffness, which is evident in Fig. 4.19. One method is to establish a lower bound gain for the control system, by considering the largest possible variation in the stiffness. However, when using a fixed controller it is very difficult to ensure stability. The system gain, which is set to meet the tracking accuracy for the linear model using the largest stiffness constant (of the order of 1 Nm), would become excessively large, with the phase margin considerably reduced, when the rotor moves near the equilibrium position corresponding to a small stiffness (of the order of 0.05 Nm). This suggests strongly that the controller should be adaptive, capable of changing itself to cope with the nonlinear stiffness variations, and maintaining both
high control accuracy and stability.

6.6.2 Gain-scheduled Control

An adaptive controller is inherently nonlinear, and an effective control approach is through gain-scheduling, which originated in connection with flight control [48,49]. Fig. 4.22 illustrates the basic concept of the typical gain-scheduled control system involved. The controller parameters are varied to retain the required performance, with the change of parameters being related to some specified operating conditions or state variables, termed the scheduling variables. The design process is to find suitable scheduling variables and schemes, and these are normally based on an understanding of the controlled process. The scheme may be either pre-programmed into the software, as a look-up table, or implemented on-line as an additional closed-loop if the scheduling variables are chosen as state variables, or output variables, as shown in Fig. 4.23. Gain-scheduled controllers provide a quick response of the controller parameters to changes in the controlled systems, compared with other adaptive controllers, such as self-tuning and reference-model controllers, which require both on-line process parameter estimation and control design [43,44]. Furthermore, the adaptation mechanism of scheduling control does not cause instability problem as a result of off-line design. A gain-scheduled controller is particularly suitable for a controlled process subject to large-scale nonlinear variations which may be identified in advance [42,50,51].

The gain-scheduled control approach involves designing a non-linear controller, comprising a family of linear controllers, each of which is designed on the basis of a specified linear operating point of the non-linear plant. When applied to the torque motor, the controller will compensate for the nonlinearly varying motor stiffness, such that the controller gain is constantly changing according to the rotor position. This establishes a lower band of loop gain that maintains the tracking error within the error band, despite the motor nonlinearity. At the same time, the system stability indicated by the phase and gain margins, and obtained from the linear compensation, is unaffected by the fast and continuous changes to the system gain. This implies that
the gain scheduled controller should be a dynamic compensator, and not merely a variable gain compensator. A first-order gain-scheduled controller was therefore used as discussed below.

### 4.6.3 Gain-scheduled Controller Design

Consideration was given to three possible locations for the gain scheduled controller, in the current loop, in series with the position loop compensators and in parallel with the position loop compensators. In all cases the scheduled variable used was the position output, and the controller has the first-order transfer function

$$G_p(s) = \frac{s + k(\theta)\omega_o}{s + \omega_o}$$  \hspace{1cm} (4.2)

where $k(\theta)$ is the gain parameter varying with the rotor position $\theta$ and $\omega_o$ is the corner frequency.

It is recognized that locating any controller in the current loop will normally only improve the current response, or any controlled dynamics included inside this feedback loop. Further, the inclusion of an adaptive controller may have a detrimental effect on the overall system stability, due to the large and rapid nonlinear dynamic changes that occur in the inner loop. Therefore, the investigation has been focused on schemes which locate the controller in the position loop, with the aim of achieving the required position tracking performance.

#### 4.6.3.1 Gain-scheduled control in series with forward position compensators

Fig. 4.24 shows the block diagram of the control scheme, with the additional controller in series with the forward position compensation and adding a third feedback loop to the previous two-loop system. The position output is chosen as the scheduling variable.
Fig. 4.25 shows a family of frequency response characteristics of the gain-scheduled controller in terms of the parameters \( k(\theta) \), with \( \omega_o \) set to 426 rad/s. The design principle is as follows. When \( k(\theta) > 1 \), the controller acts as a lag compensator, whose gain rises with any increase in \( k(\theta) \) and is greater than 0 dB for \( \omega > \omega_o \). It is used to compensate for the decrease in the system gain due to any increase in the stiffness. When \( k(\theta) < 1 \), the controller acts as a lead compensator, whose gain reduces with any decrease in \( k(\theta) \) and is less than 0 dB for \( \omega < \omega_o \). It is used to compensate for the increase in the system gain due to any reduction in the stiffness. The positive/negative phase shift provided by the lead/lag compensator depends on the value of \( k(\theta) \), but the total contribution to the overall phase margin at the gain cross-over point is additionally determined by the corner frequency \( \omega_o \). If \( \omega_o \) is far from the gain-crossover frequency, the negative phase shift may be made a minimum, ensuring satisfactory transient and steady-state response and overall stability. Once \( \omega_o \) has been chosen, \( k(\theta) \) is the only parameter in the controller that needs to be changed.

The parameter \( k(\theta) \) is made to vary in synchronism with the motor position, in such a way that it has its smallest value when the motor at the equilibrium position corresponding to the smallest stiffness constant. It increases to a larger value with an increase of the stiffness constant, and finally reaches a maximum when the rotor moves to the extreme position of \( \pm 10^\circ \). This can be expressed mathematically as

\[
k(\theta) = K_c \frac{d}{d\theta} \left[ T_s(\theta) \right]
\]

(4.3)

and

\[
T_s(\theta) = \left( \frac{a+b\theta^2}{1+c\theta^2} \right) \theta
\]

(4.4)

where \( K_c \) is a constant determined by the system performance, and \( a, b \) and \( c \) are constant coefficients determined by the nonlinear stiffness characteristics. The nonlinear function \( T_s(\theta) \) was found as the best fit to the experimental curve described in Chapter 3.
Fig 4.26 shows the frequency response characteristics of the overall open-loop control system, when the scheduled controller is incorporated into the previous two-loop system. It is in contrast to the frequency response of the linear two-loop system (see Fig. 4.19), in that the DC and low-medium frequency loop gains now remain essentially at a constant level that will ensure the position error is within the error band, despite significant, nonlinear variations in the stiffness. The reduction in relative stability is insignificant, and a phase margin exceeding 45° is achieved at all the operating points. The noise filtering ability is retained as −60 dB/dec., the same as that of the linear two-loop system (see curve v of Fig. 4.12).

Fig. 4.27 presents the time simulation results. The position tracking error (linearity) of ±0.02° clearly exists throughout the full 20° forward sweep of the motor, and only when the direction is reversed for the flyback does the drive voltage approach −35 V.

4.6.3.2 Gain-scheduled controller in parallel with forward position compensators.

Fig. 4.28 shows the diagram of another scheme, which places the gain-scheduled controller in parallel with the position compensators in the forward path. The compensation principle is such that when the stiffness increases as the rotor moves towards its extreme positions of ±10°, the gain-scheduled controller, functioning as a lag compensator with k(θ) > 1, compensates for any decrease in the loop gain via the parallel path. It can be seen however that, when the rotor moves towards the equilibrium position, the correspondingly excessively large loop gain cannot be effectively compensated for by the controller, due to its parallel connection with the linear position compensators. With the first-order controller characterised in Eqn. 4.2 and Fig. 4.25, the family of frequency response characteristics for the overall control system shown in Fig. 4.29 are very similar to Fig. 4.19, indicating that incomplete compensation will affect the improvement in the tracking performance. The time simulation given in Fig. 4.30 proves again that the system performance can be predicted by the frequency-domain design, with the position tracking error achieved being 0.07°.
4.6.4 Evaluation of the Final Control Design

Careful examination of both the frequency response and time response characteristics for the above two schemes, leads to the following comments with regard to the addition of the gain-scheduled controller.

(1) The use of the gain-scheduled controller in the position loop considerably improves the tracking performance, without affecting the overall system stability achieved by the linear compensation schemes.

(2) Locating the gain-scheduled controller in series with the forward position compensators gives a satisfactory control performance. The required position tracking error of ±0.02° has been achieved, with the drive voltage limited to ±35 V. A phase margin exceeding 45° at all the operating points is achieved, and guarantees the system stability.

(3) Locating the controller in parallel with the position compensator gives a better overall stability performance, with the phase margin exceeding 50° for all the operating points. However, the maximum position tracking error of 0.07° fails to meet the tracking performance requirement.

Therefore, the control scheme with the gain-scheduled controller located in series with the forward position compensation should be used for practical implementation.

The continuous transfer functions of the various compensators/controllers are given in Appendix B.
Chapter 4  
Control Analysis, Design and Simulation

Fig. 4.1 Open-loop frequency response characteristics for servo drive control system

Fig. 4.2 Closed-loop frequency response characteristics for servo drive control system
Fig. 4.3 Three-loop structure for a position drive control system

Fig. 4.4 Two-loop structure for a position drive control system
Fig. 4.5 Current loop system
Fig. 4.6 Open-loop frequency response characteristics of compensated and uncompensated current loop
Fig. 4.7 Close-loop frequency response characteristics of compensated and uncompensated current loop
Fig. 4.8 Time simulation for the current loop system
Fig. 4.9 Open-loop frequency response characteristics of position control with the compensated current loop and a simple gain in forward position loop
Fig. 4.10 Close-loop frequency response characteristics of position control with the compensated current loop and a simple gain in forward position loop
Fig. 4.11 Motor control system employing the position forward compensations.
Fig. 4.12 Open-loop frequency response characteristics of control system employing various linear compensation schemes 
(i) linear model, (ii) current loop added, (iii) notch and first lead compensator added, (iv) second lead compensator added, (v) lag compensator added
Fig. 4.13 Time simulation for motor control system with the current loop, and a notch and a first lead compensation in the forward path of the position loop
Fig. 4.14 Time simulation for motor control system with the current loop, and a notch and two lead compensation in the forward path of the position loop.
Fig. 4.15 Time simulation for motor control system with a current loop, and a notch, two lead and a lag compensation in the forward path of position loop
Fig. 4.16 Diagram of motor control system employing both forward and feedback position compensations.
Fig. 4.17 Closed-loop frequency response characteristics of feedback compensation showing the effectiveness in reducing an excessively large system bandwidth

(i) with a notch, first and a lag compensators placed in forward path, and a second lead compensator in feedback path

(ii) with a notch, a first and second lead, and a lag compensators placed in forward path
Fig. 4.18 Time simulation for motor control system of Fig. 4.16, with the linear motor model
Fig. 4.19 Open-loop frequency response characteristics for control system with piece-wise linear motor model
(i) \( K_s = 0.05 \, \text{Nm/rad} \), (ii) \( K_s = 0.1 \, \text{Nm/rad} \), (iii) \( K_s = 0.25 \, \text{Nm/rad} \)
(iv) \( K_s = 0.5 \, \text{Nm/rad} \), (v) \( K_s = 0.75 \, \text{Nm/rad} \), (vi) \( K_s = 0.9 \, \text{Nm/rad} \)
Fig. 4.20 Closed-loop frequency response characteristics for control system with piece-wise linear motor model

(i) $K_s = 0.05 \text{ Nm/rad}$, (ii) $K_s = 0.1 \text{ Nm/rad}$, (iii) $K_s = 0.25 \text{ Nm/rad}$
(iv) $K_s = 0.5 \text{ Nm/rad}$, (v) $K_s = 0.75 \text{ Nm/rad}$, (vi) $K_s = 0.9 \text{ Nm/rad}$
Fig. 4.21 Time simulation for motor control system of Fig. 4.16, with the nonlinear motor model
Chapter 4

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Fig. 4.22 Typical gain-scheduled control system

Fig. 4.23 Gain-scheduled control system with the output as scheduling variables
Fig. 4.24 Diagram of control system employing the gain-scheduled controller in series with the position loop compensators.
Fig. 4.25 Family of frequency response characteristics for the gain-scheduled controller

(i) $k = 0.1$,  
(ii) $k = 0.2$,  
(iii) $k = 0.5$,  
(iv) $k = 0.8$

(v) $k = 1$,  
(vi) $k = 2$,  
(vii) $k = 5$,  
(viii) $k = 8$

(ix) $k = 10$
Fig. 4.26 Family of frequency response characteristics for control system employing the gain-scheduled controller in series with the forward position loop compensators

(i) $K_s = 0.05 \text{ Nm/rad}$, (ii) $K_s = 0.1 \text{ Nm/rad}$, (iii) $K_s = 0.25 \text{ Nm/rad}$
(iv) $K_s = 0.5 \text{ Nm/rad}$, (v) $K_s = 0.75 \text{ Nm/rad}$, (vi) $K_s = 0.9 \text{ Nm/rad}$
Fig. 4.27 Time simulation for motor control system employing the gain-scheduled controller in series with the forward position loop compensators
Fig. 4.28 Diagram of control system employing the gain-scheduled controller in parallel with the position loop compensators.
Fig. 4.29 Frequency response characteristics for control system employing the gain-scheduled controller in parallel with the forward position loop compensations

(i) $K_s = 0.05 \, \text{Nm/rad}$, (ii) $K_s = 0.1 \, \text{Nm/rad}$, (iii) $K_s = 0.25 \, \text{Nm/rad}$

(iv) $K_s = 0.5 \, \text{Nm/rad}$, (v) $K_s = 0.75 \, \text{Nm/rad}$, (vi) $K_s = 0.9 \, \text{Nm/rad}$
Fig. 4.30 Time simulation for motor control system employing the gain-scheduled controller in parallel with the forward position loop compensators.
Chapter 5

Drive Strategy One: Linear Power Amplifier

The power amplifier converts the normally small control signals to the level of the power signals needed to drive the motor. Chapters 5 and 6 analyze and discuss the options for the power amplifier, with design considerations given to the experimental prototypes developed to drive the motor.

5.1 INTRODUCTION TO THE POWER AMPLIFIERS

The power amplifier can be either linear or switched-mode, depending on the drive requirements [52] and, ideally, it should have the following capabilities.

1. Both the output voltage and current can reverse, in order to provide four-quadrant operation.
2. Operation in a current-controlled mode should be possible. This is usually best implemented by a current feedback loop that introduces both dynamic compensation and an inherent current limiting of the converter output.
3. The average output voltage should vary linearly with the control input, and should be independent of the load on the motor.
4. The armature current should produce minimal fluctuations in the torque, speed and/or rotor position.
5. The converter output should respond as quickly as possible to the control input, allowing the converter to be represented by a constant gain without a dead time in the overall transfer function model.

A linear power amplifier can satisfy all these requirements, and is preferred in wide-bandwidth low-power systems below several hundred watts. Its advantages include the absence of electromagnetic interference (EMI) and the ease of interfacing with the microcontroller. Its main shortcomings are a low energy efficiency, due to the significant amount of power dissipated in the output transistors, the bulky size of the heat sinks for high power drives, and a high component cost.
In conventional drive systems, linear amplifiers are normally constructed using a linear gain element, such as an operational amplifier, to feed a power stage which in turn drives the motor. However, the rapid development of LSI and VLSI technology has made it possible to integrate the power stage into the operational amplifier, producing the true monolithic linear IC power devices that are now commercially available.

On the other hand, switched-mode amplifiers control the output voltage by variation of the duty ratio of the power switches, which operate in either a saturated or an off mode, and dissipate little power. Switched-mode amplifiers have found widespread use in medium and high power converter systems, where the performance in terms of energy efficiency, power rating and physical size is important. There are however inherent limitations, due to the reduced system bandwidth, the EMI problems, and the complex hardware and software required for the switching operations.

The following sections examine the drive behaviour of the limited angle torque motor, and analyze and compare the two main linear amplifier topologies. A detailed description is given of the development of the experimental amplifier, which was constructed using two power operational amplifiers L465 operating in complementary modes. It is shown that, with a voltage supply of ±20 V, the amplifier was able to provide a maximum voltage of ±40 V, with a current output up to ±4 A.

5.2 DRIVE BEHAVIOUR ANALYSIS

Fig. 5.1 shows a block diagram for the linear power amplifier supplied from a dc source, and used to drive the torque motor modelled as a voltage source connected in series with an R-L circuit. The drive requirement for the motor may be examined by observing the relationship between the current $i_o$ and the voltage $v_o$ appearing at the output terminals of the amplifier.

When a 50 Hz 24 V(peak to peak) sinusoidal voltage produced by the amplifier was applied to the motor, the voltage and current waveforms were as shown in Fig. 5.2.
During interval $t_1$, the amplifier supplies a positive voltage $v_o$ to the motor and the current $i_o$ flows inwards. During $t_2$, the voltage is negative and the current is reducing, but still positive. During $t_3$, the current and the voltage are both negative. The amplifier has therefore to sink current, and continues to do so during the interval $t_4$ when the voltage becomes positive. The process is repeated in subsequent supply cycles, and the relation between $v_o$ and $i_o$ may be summarised as:

- Interval $t_1$: $v_o > 0$, $i_o > 0$
- Interval $t_2$: $v_o < 0$, $i_o > 0$
- Interval $t_3$: $v_o < 0$, $i_o < 0$
- Interval $t_4$: $v_o > 0$, $i_o < 0$

showing that the power amplifier operates in all four-quadrants of the $v$-$i$ plane during each 20 ms cycle of operation.

The above analysis, and that carried out in Chapter 3, indicates clearly that a power amplifier must satisfy the requirements (1) to (5) of Section 5.1, in order to drive the torque motor effectively and efficiently.

### 5.3 Four-Quadrant Linear Amplifiers

Both linear bipolar and linear bridge four-quadrant amplifiers are commonly used in linear servo drive, and they may be characterized by their output stage configurations.

#### 5.3.1 Linear Bipolar Amplifiers [53]

The linear bipolar circuit of Fig. 5.3 uses a PNP and an NPN transistor in a complementary emitter-follower scheme. If base-emitter forward voltage drops are ignored, the emitter voltage of each transistor follows the input voltage and is applied to the motor. The current flows through either transistor $T_1$ or transistor $T_2$, and these operate in the linear region. For example, when $v_i$ is positive $T_1$ carries a motor current provided from the power supply $+V_s$. Since the PN junction in this
transistor is forward-biased, a voltage of approximately 0.6 V appears across the base-emitter junction. The base-emitter junction of $T_2$ is however reverse-biased and the transistor does not conduct. Conversely, when $v_i$ is negative $T_2$ conducts and carries the motor current, which is supplied by the power supply $-V_s$.

One problem arises with this circuit when the base-emitter forward voltage drop of each transistor is considered. The relationship between $v_i$ and $v_o$ is then as shown in Fig. 5.4(a), with a dead zone of about $-0.6$ V to $+0.6$ V existing about the two voltage cross-overs. Thus, when $v_i$ varies sinusoidally, the output voltage $v_o$ is distorted, as shown in Fig. 5.4(b). The problem is eliminated by adding two further diodes to the circuit, as shown in Fig. 5.5. When the compensation is incomplete, due to discrepancies between the characteristics of these diodes and those of the base-emitter junctions in the transistors, there is a possibility of simultaneous current flow in both transistors. A remedy for this is to insert two small-value resistors between the emitters, as shown in Fig. 5.6.

Fig. 5.7 illustrates four-quadrant operation of the linear bipolar amplifier. Note that, when the polarity of the terminal voltage opposes the current flow, either transistor $T_1$ or $T_2$ will continue to conduct, depending on the direction of current flow.

5.3.2 Linear Bridge Amplifier [2,53]

Fig. 5.8 shows the circuit diagram for the linear bridge amplifier. One operating mode occurs when the transistor pair $T_1$, $T_4$ conducts, and positive voltage and current are applied to the motor, corresponding to first quadrant operation in the $v$-$i$ plane. When the transistor pair $T_2$, $T_3$ conduct, voltage and current of opposite polarities are applied to the motor, which corresponds to third-quadrant operation. While one transistor pair conducts, the other pair must both be in the cut-off region. Both the magnitude and polarity of the output voltage are controlled by the input voltage applied to the bases of the operating transistor pair, whereas the magnitude and polarity of the current depend on the characteristics of the load.
For second- and fourth-quadrant operation, extra control is required to enable the current to reverse against the opposite polarity voltage, and the control circuit for the bridge amplifier may therefore be more complicated than that for the bipolar amplifier. One effective way of overcoming this difficulty is to use two identical bipolar amplifiers (see Fig. 5.7) to form the bridge circuit shown in Fig. 5.9. When appropriately controlled, the amplifier is capable of the four-quadrant operation illustrated by Fig. 5.10.

5.3.3 Comparison Between the Linear Bipolar and Linear Bridge Amplifiers

A linear bridge circuit, using two linear bipolar circuits, has certain obvious advantages. It requires only one power supply for full four-quadrant operation, although a dual power supply works equally well. The transistor \( V_{CEO} \) rating (i.e., the maximum collector to emitter voltage) is reduced to the magnitude of the single power supply, compared with the single bipolar amplifier requiring the \( V_{CEO} \) rating to be the sum of the dual power supplies. Furthermore, if the bridge is properly designed, the difference between the power supply and the motor voltages is equally divided between the two transistors. This greatly increases their output current capability before a forward-bias second-breakdown failure is encountered. One shortcoming is that more components are needed, and the cost of the system is accordingly greater. However, this is usually compensated for by a considerable improvement in the drive performance.

5.3.4 Current-Controlled Linear Servo Amplifier [2,52]

A current-controlled linear servo amplifier is a linear amplifier incorporating a mechanism capable of implementing current control. In the basic scheme illustrated in Fig. 5.11, the power transistor is used to control a dc motor, and the emitter current \( i_e \) is determined directly by \( v_i \). By neglecting the base-emitter voltage \( v_{BE} \), we obtain \( i_o \approx i_e = v_i/R_e \), showing that the output current \( i_o \) is directly controlled by the input voltage \( v_i \).
The current-control required by high performance servo systems is usually implemented using an inner current loop with outer speed and/or position loops. In the current-controlled bipolar amplifier of Fig. 5.12(a), a small-value resistor is used to sense the current, while an operational amplifier used as an error amplifier controls the power stage circuit. Kirchhoff's current law applied to the inverting input terminal (the virtual ground) of the amplifier gives

\[ i_{ref} - i_f = i_c \]  

(5.1)

where \( i_{ref} \), \( i_f \) and \( i_c \) are the reference, feedback and error current signals, respectively.

Substituting \( v_i = i_{ref}R_2 \), \( v_c = i_cR_f = v_o \), \( v_s = i_fR_f = i_oRS \) gives

\[ \frac{v_i}{R_2} - \frac{R_s}{R_1}i_o = \frac{v_c}{R_f} \]  

(5.2)

which is shown diagrammatically in Fig. 5.12(b).

In another common current-control strategy, the current feedback loop operates only when the circuit reaches a certain threshold, thereby imposing a maximum current limit on the power amplifier. This is usually known as a current interventionist system.

### 5.4 POWER OPERATIONAL AMPLIFIERS

A power operational amplifier has the same circuit configuration as a conventional operational amplifier, with the output stage being greatly enhanced in terms of its capability to handle a large drive voltage and current. Such a power amplifier can be regarded as a device which combines, on a single chip, input, pre-amplifier and compensation circuits, with the bipolar power stage output discussed in the previous section. Therefore, the power operational amplifier can be analyzed in the way
addressed extensively elsewhere [54,55,56,57].

5.4.1 Equivalent Circuit

The output voltage of the equivalent circuit of Fig. 5.13(a) is

\[ v_o = A_o v_{id} = A_o (v_1 - v_2) \]  

where \( A_o \) = open-loop voltage gain  
\( v_{id} \) = differential input voltage  
\( v_1 \) = voltage at the nonlinear inverting input terminal with respect to ground  
\( v_2 \) = voltage at the inverting terminal with respect to ground  
\(+ V_{cc}\) = positive power supply  
\(- V_{cc}\) = negative power supply

Eqn. (5.3) shows that the output \( v_o \) is directly proportional to the arithmetic difference between the two input voltages (referred to as the differential input), and not to the inputs themselves (referred to as common mode input). The polarity of the output voltage therefore depends on the polarity of the difference voltage. Fig. 5.13(b) shows the ideal voltage transfer curve, which is the graphical representation of Eqn. (5.3).

5.4.2 Closed-loop Configurations

In practice, power operational amplifiers are seldom used in the open-loop configuration, but are configured as either closed-loop inverting or non-inverting amplifiers as shown in Fig. 5.14(a) and (b). Like conventional operational amplifiers, the overall gain of each circuit is precisely determined by the values of external feedback components, almost irrespective of the individual characteristics. The amplifier is powered by two voltage supplies \( \pm V_s \), but could alternatively be powered from a single-ended supply.
5.4.3 Performance of Power Operational Amplifier

Ideal power operational amplifiers have infinite values of input impedance, open-loop gain and bandwidth, zero output impedance, and give perfect tracking between input and output. Since, however, practical amplifiers fall short of these ideals, it is important to fully understand the performance as specified in the data sheet and discussed below.

5.4.3.1 DC electrical characteristics

The DC characteristics are defined by the following quantities:

*Open-loop Voltage Gain* ($A_o$)

This is the dc or low-frequency voltage gain, occurring between the input and output terminals of the operational amplifier. It may be expressed in direct terms or in terms of dB. Typical figures are within the range of 80 - 100 dB.

*Input Resistance* ($R_i$)

This is the resistive part of the impedance looking directly into the input terminals of the amplifier when used in an open-loop mode. Typical values are above 1 MΩ for bipolar transistor amplifiers, and $10^6$ MΩ for FET-input amplifiers.

*Output Resistor* ($R_o$)

This is the resistive part of the output impedance of the amplifier when used in the open-loop mode. Values of a few hundred ohms or less are typical of most operational amplifiers.

*Input Bias Current* ($I_i$)

This is the sink or source current of the input terminals of the operational amplifiers, when biased for linear operation. It is typically a fraction of a micro-amp in bipolar amplifiers, and a few pico-amps in FET devices.
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Supply Voltage Range (±Vcc)
Operational amplifiers are usually operated with split (positive and negative) supply rails, which are typically at potentials between ±3 V and ±15 V.

Input Voltage Range (Vi)
Most operational amplifiers only operate correctly if their input terminal voltage is less than the supply value.

Differential Input Offset Voltage (Vdi)
This is the output voltage that exists in a practical operational amplifier when both input terminals are grounded. Although it is normally only a few millivolts, the output voltage of the final stage may depart considerably from the zero value when the overall system gain is large. Because of this, most amplifiers have facilities, either external or internal, that compensate for the offset voltage.

Common Mode Rejection Ratio (CMRR)
An operational amplifier has an output that is proportional to the difference between the signal on its two input terminals. Ideally, it should give zero output if identical signals are applied simultaneously to both inputs, ie: in common mode. In practice, such signals do not entirely cancel within the amplifier, but produce a small net output signal. The ability to reject common mode signals is usually expressed in terms of the 'common mode rejection ratio' (the ratio of the differential signal gain versus the common mode signal gain), and a value of 90 dB is typical of most practical amplifiers.

5.4.3.2 AC electrical characteristics

The AC characteristics are defined by the following quantities:

Unity Gain Frequency fBo
This is the frequency at which the gain of the open-loop gain frequency response falls to unity (0 dB). It is also defined as the gain-bandwidth product, since for a given
amplifier this is equal to $f_{B0}$. Fig. 5.15 shows the gain-frequency response of a typical power operational amplifier and, for a given open-loop gain, the corresponding frequency bandwidth may be determined from

$$f = \frac{f_{B0}}{A_o(f)}$$

or

$$f_{B0} = f \times A_o(f)$$

where $A_o(f)$ is the open-loop gain at the frequency $f$.

**Closed-loop Gain ($A_{cl}$)**

The ideal closed-loop gain of the power operational amplifier depends only on the external components which complete the closed-loop. However, the actual closed-loop gain is determined by the open-loop gain of the amplifier, which is frequency-dependent, as shown by Fig. 5.15 and Eqn 5.4. Consequently, the closed-loop gain $A_{cl}$ is also determined by the signal frequency applied to the amplifier. The relationship between the open-loop gain, and the ideal and actual closed-loop gains for the inverting and non-inverting amplifiers shown in Fig. 5.14 may be expressed as [4]

$$actual\ A_{cl} = \frac{-\frac{R_f}{R_1}}{1 + \frac{1}{A_o(f)}\left(\frac{R_f + R_1}{R_1}\right)}$$

(5.4)

where $-\frac{R_f}{R_1}$ = ideal $A_{cl}$ for inverting amplifiers, and
actual $A_{cl} = \frac{(R_f + R_1)}{R_1} \frac{1}{1 + \frac{1}{A_o(f)} \left( \frac{R_f + R_1}{R_1} \right)}$ (5.5)

where $(R_f + R_1)/R_1 = \text{ideal } A_{cl}$ for non-inverting amplifiers.

It is seen from Eqns. (5.4) and (5.5) that, when the open-loop gain is much larger than the closed-loop gain, the actual closed-loop gain is close to the corresponding ideal closed-loop gain at the given frequency. The closed-loop amplifier bandwidth is therefore determined solely by the open-loop gain vs frequency characteristics and closed loop gain.

**Slew Rate (SR)**

In addition to the normal closed-loop bandwidth limitations, the amplifiers are also subject to a phenomenon termed output slew rate limiting, which is defined as the maximum rate of change of output voltage produced in response to a large input step. Slew rate usually expressed in volts per microsecond. Fig. 5.16 illustrates the effects of slew rate limiting in the output of the operational amplifier fed with a square waveform input.

**Power Bandwidth $f_p$**

This is defined as the maximum frequency, measured at either unity or any other given closed loop gain, for which full output can be obtained at rated load without distortion. The inability of an amplifier output voltage to slew faster than a limiting rate can introduce distortion in otherwise sinusoidal output signals. Some amplifier data sheets give graphs relating the maximum sinusoidal output voltage obtainable without distortion to the corresponding frequency. For this reason, it is also termed **Full Power Response**.
5.4.4 AC Performance of Power Operational Amplifier

To drive the torque motor requires the amplifier to be used as an ac amplifier, with its closed-loop bandwidth exceeding the overall control system bandwidth of 1 kHz. The key indicators that must be considered in this application are the corresponding performance characteristics of the amplifier, in terms of the open-loop gain frequency response, slew rate and power bandwidth.

The open-loop gain frequency response provides an effective way of analyzing the amplifier dynamic behaviour when small signals of less than 1 V peak are present, and it is because of this that the open-loop frequency response is also referred to as the small-signal response characteristic. The main frequency response parameters, such as the unity gain frequency $f_{Bo}$, open-loop gain and bandwidth $f_o$ and $A_o(f)$, respectively, and the closed-loop gain and bandwidth $A_c(f)$ and $f_{cl}$, were discussed in the last section. However, when the signals are large, the performance of the amplifier is mainly influenced by the slew rate and power bandwidth, which impose limitations on both the maximum amplitude and the rate of change of the signals applied to the amplifier, to ensure linear signal amplification. These are further considered below.

In the voltage follower of Fig. 5.17(a), $v_i$ is the sine wave with a peak amplitude $V_p$ shown in Fig. 5.17(b). The maximum rate of change of $v_i$ depends on both the frequency $f$ and the peak amplitude $V_p$, and it must not exceed the slew rate permitted by the amplifier, or

$$\left(\frac{dv_i}{dt}\right)_{\text{max}} = 2\pi f V_p \leq SR$$

If this figure exceeds the slew rate of the amplifier, the output $v_o$ will be distorted (i.e., the output $v_o$ cannot follow $v_i$ because of slew rate limiting), as shown by the triangular shape of $v_o$ in Fig. 5.17(c). The maximum frequency $f_{\text{max}}$ at which an
undistorted output voltage with a peak value of $V_p$ is obtained, is determined by the slew rate, in accordance with

$$f_{\text{max}} = \frac{SR}{2\pi V_p} \quad (5.7)$$

which establishes the Power Bandwidth, or Full Power Response (previously defined), when the amplifier is used at the rated load. If both $f_{\text{max}}$ and SR are given, the peak sinusoidal output $V_p$ that can be produced without distortion is

$$V_p = \frac{SR}{2\pi f_{\text{max}}} \quad (5.8)$$

For a design problem in which the control specification is given in terms of $f_{\text{max}}$ and $V_p$, the lower limit of the slew rate required for the power operational amplifier can be calculated using Eqn. 5.7 (or Eqn. 5.8). Therefore, to drive the torque motor, the slew rate of the amplifier must be at least 8 V/µs to obtain an undistorted 1 kHz sine wave output with peak value of 20 V. It is evident that achieving any increase in $f_{\text{max}}$ will correspond to a reduction in the maximum output voltage.

5.5 DESIGN OF LINEAR POWER AMPLIFIER

5.5.1 Design Specifications

The main design specifications for the power amplifier used to drive the torque motor are:

- Output voltage exceeding $\pm 35$ V;
- Output current exceeding 0.5 A;
- Power bandwidth at least 1 kHz;
- Slew rate greater than 8 V/µs;
5.5.2 Power Operational Amplifier L465

The power operational amplifier L465 is a monolithic linear device with main features being:

- Output current 4 A
- Supply voltage ±20 V
- Typical slew rate of 14 V/µs
- Large power bandwidth
- Low saturation
- Safe operation area (SOA) protection
- Short circuit protection
- Thermal protection

The data sheet for the L465 is given in Appendix C, and indicates a bandwidth of 100 kHz when \( V_o = 1 \) V and \( R_L = 4 \) Ω. The output voltage swing \( V_{pp} \) is 27 V at a bandwidth of 10 kHz and an output current of 0.5 A. In addition, the open-loop voltage gain is 80 dB at 1 kHz, and from Eqn. 5.3 this gives a unity-gain bandwidth of 10 MHz. Various protection facilities available on the chip further enhance the safety of operation. The disadvantage of the L465 is that the output voltage is limited to the maximum of ±20 V, which does not meet the drive requirement of ±35 V. However, this has been effectively overcome by use of the circuit configuration described below, which involves the use of the two L465 devices.

5.5.3 Configuration and Operating Principle

The circuit configuration of the linear power amplifier is shown in Fig. 5.18(a), with a pair of L465s forming the bridge circuit discussed in Section 5.2. A more detailed circuit, including the power stages of the L465 is given in Fig. 5.18(b). In addition to the capability for four-quadrant operation, the effective voltage across the motor is increased by a factor of at least two, due to the complimentary operation of the operational amplifiers. Using a split power supply of ±20 V results in a maximum
drive voltage of $\pm 40$ V.

The input is applied to operational amplifier 1, connected as a non-inverting amplifier, with the output connected both to one terminal of the motor and to the inverting input of operational amplifier 2 connected as an inverting amplifier. When the output voltage $v_A$ of operational amplifier 1 appears at terminal A of the motor, the output voltage $v_B$ of operational amplifier 2, which is proportional to $-v_A$, appears at terminal B. The drive voltage is

$$v_{AB} = v_A - v_B = v_A - K_v v_A = (1 + K_v) v_A$$  \hspace{1cm} (5.9)

with $v_A = v_i$ for the non-inverting amplifier 1

$$v_{AB} = (1 + K_v) v_i$$  \hspace{1cm} (5.10)

where $K_v = R_0/R_x$ determines the voltage gain of the amplifier. It is clear that the voltage across the motor terminals is directly proportional to the input control voltage, and that only one input is required to control the bridge circuit that drives the motor. The high input impedance associated with an operational amplifier makes it easy to interface with the other operational amplifiers or a digital-to-analogue converter, without causing excessive loading. The low output impedance in both the inverting and non-inverting amplifiers results in a highly efficient drive.

The circuit incorporates a small resistor $R_i$ used to sense the motor current when implementing the current-controlled scheme considered in Section 5.3.4.

5.5.4 Practical Considerations

5.5.4.1 Choice of voltage gain $K_v$

Eqn. 5.10 defines the linear relation between the control input and drive output, and
the required voltage is achieved by an appropriate choice of the voltage gain $K_v$. Since the control signal may contain frequencies above 20 times the basic reference frequency of 50 Hz, the amplifier gain $K_v$ should be chosen such that it remains essentially constant over this frequency range, and it is also independent of the output current. From previous discussions, it is evident that the lower the closed-loop gain the wider is the power bandwidth. On the other hand, the amplifier gain cannot be too small or the required output voltage cannot be achieved. Furthermore, since one L465 operates as a follower, and the other as a complementary inverter, it is better not to make the inverter gain too large and to have an overall balanced gain-frequency response determined by that of the individual devices. $K_v$ is therefore set between 2 and 3, while the maximum input level to the power amplifier is assumed to be $\pm 10$ V, which is conveniently achieved from any operational amplifiers. Eqn. (5.10) shows that this gives a maximum output voltage between $\pm 30$ V and $\pm 40$ V in the power amplifier.

5.5.3.2 Safe operation and current limiting

The L465 offers various internal protection features for safe operation, including SOA, short circuit and thermal protection. However, to provide extra protection, a 2 A quick-blow fuse was inserted in series with the power supply and a heat-sink with a thermal resistance of 4°C/W (L100, W65, H15) was used for each L465, to limit the case temperature to around 45°C during normal operation.

Four anti-parallel freewheeling diodes ($D_1$ to $D_4$ in Fig. 5.18) were employed to limit the reverse voltage across the transistors to the forward diode drop, thus protecting them from damage by any excessive voltage induced in the motor winding by sudden changes in the current. They also complete a return path for regenerated current [53].
Fig. 5.1 Diagram of linear power amplifier

Sinusoidal input voltage
\[ v_o = 24V_{p-p} \]

Drive current
\[ i_o = 0.5A_{p-p} \]

20 ms

Fig. 5.2 Simulated response waveforms showing the relation of the drive voltage and current
**Chapter 5**

**Drive Strategy One: Linear Power Amplifier**

**Fig. 5.3** Linear bipolar amplifier: output stage

![Linear bipolar amplifier circuit diagram](image)

**Fig. 5.4** Characteristics of the linear amplifier of Fig. 5.3

(a) Transfer function showing crossover distortion

(b) Output distortion for a sinusoidal input

Approx. 0.6V
**Fig. 5.5** Elimination of the dead zone using diodes

**Fig. 5.6** A circuit using low resistors between both emitters
Chapter 5  Drive Strategy One: Linear Power Amplifier

(a) First-quadrant operation
\( v_o > 0, \ i_o > 0 \)

(b) Second-quadrant operation
\( v_o < 0, \ i_o > 0 \)

(c) Third-quadrant operation
\( v_o < 0, \ i_o < 0 \)

(d) Fourth-quadrant operation
\( v_o > 0, \ i_o < 0 \)

Fig. 5.7 Four-quadrant operation of the linear bipolar amplifier
Fig. 5.8 Linear bridge amplifier: output stage

Fig. 5.9 Linear bridge amplifier employing two identical bipolar amplifiers in the output stage
(a) First-quadrant operation
\[ v_o > 0, \ i_o > 0, \ v_{iB} = -v_{iA} \]

(b) Second-quadrant operation
\[ v_o < 0, \ i_o > 0, \ v_{iB} = -v_{iA} \]

(c) Third-quadrant operation
\[ v_o < 0, \ i_o < 0, \ v_{iB} = -v_{iA} \]

(d) Fourth-quadrant operation
\[ v_o > 0, \ i_o < 0, \ v_{iB} = -v_{iA} \]

Fig. 5.10 Four-quadrant operation of the linear bridge amplifier using the circuit of Fig. 5.9

120
**Fig. 5.11** Basic current-controlled linear amplifier

(a) Linear bipolar amplifier with current sensor and error amplifier

\[ i_{\text{ref}} = \frac{v_i}{R_2} \quad i_f = \frac{v_c}{R_f} \quad i_e = \frac{(R_s / R_i) i_o}{R_3} \]

(b) Equivalent relation between reference, feedback and error current signals

**Fig. 5.12** A current-controlled bipolar linear amplifier
(a) Equivalent circuit

(b) Ideal voltage transfer curve

Fig. 5.13 Representation of a power operational amplifier
Fig. 5.14 Circuit configurations of power operational Amplifier
Chapter 5  Drive Strategy One: Linear Power Amplifier

Fig. 5.15 Typical frequency response of power operational amplifier

Fig. 5.16 Effect of the slew rate limiting on the output of the amplifier with a square wave input
Chapter 5  Drive Strategy One: Linear Power Amplifier

(a) Voltage follower circuit

(b) Sinusoidal input with the maximum frequency $f_{\text{max}}$

(c) Voltage output showing distortion due to slew rate limiting

Fig. 5.17 Effect of the slew rate limiting on the output of the voltage follower with a sinusoidal input
Chapter 5

Drive Strategy One: Linear Power Amplifier

(a) Circuit schematic

(b) A close look at the circuit showing the bridge configuration at the power stage when using a pair of L465s

Fig. 5.18 Linear amplifier employing power operational amplifiers
Chapter 6

Drive Strategy Two: Switch-Mode Power Amplifier

A PWM switch-mode power amplifier was investigated as an alternative to the linear amplifier, with a view to improving the overall performance by increasing the bandwidth of the power amplifier. In addition, reducing the component count by employing software controlled digital PWM, and eliminating the heat sink required by the linear amplifier, would reduce the initial cost.

The H-bridge switch-mode converter is suitable for driving the motor, since under idealized conditions it possesses a performance superior to that of a linear amplifier, in terms of a linear voltage gain with theoretically infinite bandwidth, and a smaller physical size due to the high switching frequency. Investigations of its suitability for the present application are discussed and a comparison is made with corresponding results for a linear power amplifier.

6.1 SYSTEM DESCRIPTION [58, 59]

6.1.1 Circuit Topology

The H-bridge converter shown in Fig. 6.1 consists of two legs, A and B, each of which has two switches, $S_{A+}$ and $S_{A-}$, and $S_{B+}$ and $S_{B-}$. The diode connected in anti-parallel with each of the switches provides a path for any reverse current, and is essential for four-quadrant operation when the drive load is non-passive. The constant voltage source $V_s$ has a very large capacitor connected across it, to reduce the voltage ripple in the supply to the converter. All the switches and diodes are assumed to be ideal devices, which can be turned on or off instantly. The two switches in each leg are controlled in such a way that, when one of them is on, the other is off, but both of them are never off simultaneously. The converter output voltage $v_o (=v_{AN} - v_{BN})$ therefore depends only on the switch states and is independent of the direction of $i_o$. The above assumptions are used in the following analysis of the idealize H-bridge converter, with the load being a dc-motor modelled as a voltage.
source $E_a$ in series with an R-L circuit.

6.1.2 PWM Modulation

To control the converter switches, a symmetrical carrier waveform is compared with a control voltage using a comparator and logic circuitry. In the PWM switching scheme the carrier frequency, which is also the switching frequency, is fixed, and the switch duty ratio (ratio of the on-time to the switching period) is varied. Two switching strategies are commonly used; bipolar switching, in which complementary switch pairs $(S_{A+}, S_{B-})$ and $(S_{A-}, S_{B+})$ are alternately switched-on and off, and unipolar switching, in which the switches in one leg are controlled independently of those in the other leg.

Fig. 6.2 shows circuit diagrams of the modulators for the two switching strategies. It is evident that the two strategies require different modulating circuits, and it is impossible for a given analogue modulator to change from one strategy to the other. However, with the advent of the microprocessor and VLSI circuitry, the function of the modulator hardware may be realized by software programmed into the controller, greatly increasing the flexibility for change between the switching strategies and reducing the component count required for the implementation of analog PWM. This technique is referred to as digital PWM [60].

6.2 PWM SWITCHING STRATEGIES [52,58]

The principles of bipolar and unipolar strategies are examined and compared with respect to the H-bridge DC-DC converter.

6.2.1 Bipolar Switching Strategy

Fig. 6.3 shows various idealized waveforms for the bipolar switching strategy. Switching signals generated by comparing a triangular waveform $V_{tri}$ with a dc control voltage $V_c$ are shown in Fig. 6.3(a). When $V_c > V_{tri}$, $S_{A+}$ and $S_{B-}$ are both turned
on, otherwise, $S_{B+}$ and $S_{A-}$ are turned on. Figs. 6.3(b) to (d) show the output voltages $v_{AN}$, $v_{BN}$ and $v_o (= v_{AN} - v_{BN})$. It is seen that $v_o$ jumps between $+V_s$ and $-V_s$ and, for this reason, the switching strategy is referred to as bipolar switching PWM.

By inspecting Fig. 6.3, the duration $t_{on}$ of switch pair A ($S_{A+}$, $S_{B-}$) is

$$t_{on} = 2t_1 + \frac{T_{sw}}{2} \quad (6.1)$$

and the duty ratio of the switch pair A is then

$$D_1 = \frac{t_{on}}{T_{sw}} = \frac{1}{2} (1 + \frac{V_c}{\hat{V}_{tri}}) \quad (6.2)$$

where $\hat{V}_{tri}$ is the peak amplitude of the triangular carrier wave. The duty ratio of the switch pair B ($S_{B+}$, $S_{A-}$) is

$$D_2 = 1 - D_1 \quad (6.3)$$

From Eqns. (6.2) and (6.3), the voltages at the output terminals A and B are

$$V_{AN} = D_1 V_s \quad (6.4)$$

and

$$V_{BN} = D_2 V_s \quad (6.5)$$

so that.
Chapter 6  Drive Strategy Two: Switch-Mode Power Amplifier

\[
V_o = V_{AN} - V_{BN} = D_1 V_s + D_2 V_s = (2D_1 - 1) V_s \tag{6.6}
\]

giving

\[
M = \frac{V_o}{V_s} = 2D_1 - 1 \tag{6.7}
\]

where \(M\) is the voltage gain. Substituting for \(D_1\) from Eqn. (6.2) into Eqn. (6.6) gives

\[
V_o = \left( \frac{V_s}{V_{tri}} \right) V_c = kV_c \tag{6.8}
\]

where \(k = V_s/\hat{V}_{tri}\) is a constant for a given \(V_s\) and the carrier wave.

It is obvious from Eqn. (6.2) that the duty ratio \(D_1\) varies between 0 and 1, depending on the polarity and magnitude of the control input \(V_c\), and therefore that the average output \(V_o\) may be varied continuously from \(-V_s\) to \(+V_s\). The average output current \(I_o\), can be either positive or negative. For a small \(I_o\), as shown in Fig. 6.3(e), the instantaneous current \(i_o\) varies between positive and negative over a switching cycle, regardless of the polarity of the output voltage, and the converter operates in all four quadrants in the \(v_o\)-\(i_o\) plane, as shown in Fig. 6.4.

6.2.2 Unipolar Switching Strategy

In the unipolar switching strategy shown in Fig. 6.5, a triangular waveform is compared with the control voltage \(+V_c\), as well as with \(-V_c\), to determine the switching signals controlling legs A and B in the following manner:

- \(S_{A+}\) is on, but \(S_{A-}\) is off, if \(V_c > V_{tri}\)
- \(S_{A+}\) is off, but \(S_{A-}\) is on, if \(V_c < V_{tri}\)

and

- \(S_{B+}\) is on, but \(S_{B-}\) is off, if \(-V_c > V_{tri}\)
S_{B+} is off, but S_{B-} is on, if \(-V_c < V_{tri}\)

Fig. 6.5 shows that the states of the switches in each leg are complementary, i.e., when one is on, the other is off. The duty ratio \(D_1\) for switch \(S_{A+}\) is the same as that in Eqn. (6.2) and can be re-written

\[
D_1 = \frac{t_{on}}{T_{sw}} = \frac{1}{2} \left(1 + \frac{V_c}{\dot{V}_{tri}}\right)
\]  \hspace{1cm} (6.9)

and the duty ratio \(D_2\) for switch \(S_{B+}\) is

\[
D_2 = 1 - D_1
\]  \hspace{1cm} (6.10)

Eqn. (6.6) gives

\[
V_o = V_{AN} - V_{BN} = D_1 V_s + D_2 V_s = (2D_1 - 1)V_s
\]  \hspace{1cm} (6.11)

and substituting Eqn. (6.2) in (6.11)

\[
V_o = \left(\frac{V_s}{\dot{V}_{tri}}\right) V_c = kV_c
\]  \hspace{1cm} (6.12)

It is seen from Fig. 6.5(d) that the output voltage \(v_o\) jumps between \(V_s\) to 0, and for this reason, the switching strategy is called unipolar switching. In a manner similar to bipolar switching, when the average current \(I_o\) is small, the instantaneous current \(i_o\) during one switching period can be either positive and negative, as shown in Fig. 6.5(e), and the converter operates in all four quadrants of the \(v_o-i_o\) plane, as shown in Fig. 6.6.
6.2.3 Comparison of the Two Switching Strategies

In both switching strategies, the output voltage $v_o$ depends on the states of the switches or freewheeling diodes, and the average output voltage $V_o$ may be varied linearly with the input control voltage. With the same switching frequency, unipolar switching results in a better output voltage waveform than does bipolar switching, since the switching frequency in the output voltage is effectively doubled and any ripple is considerably reduced.

6.3 CONVERTER HARMONICS

To drive the torque motor requires the converter to be controlled by a 50 Hz non-sinusoidal input signal computed from the digital controller, as described in Chapter 4. Any complex periodic waveform may be expressed mathematically as a dc mean value, plus a fundamental frequency sinusoid [61] and its harmonics, and therefore the converter harmonics may be analyzed in a same way as that for the converter controlled by a sinusoidal waveform.

Figs. 6.7 and 6.8 show the PWM modulation waveforms, the switching signals and the harmonic spectrum of the output voltages, for both bipolar and unipolar switching strategies. Detailed investigations elsewhere [52,62] have shown that the harmonic distribution in the H-bridge converter has the following important features:

1. The peak of the fundamental frequency component is proportional to the input voltage, for the given dc supply voltage and carrier triangular waveform.

2. In the linear modulation range (where the peak amplitude of the input control signal is not larger than that of the carrier signal) harmonics in the output voltage exist as sidebands, centred around the switching frequency and its multiples.

3. When the carrier frequency, which is also the switching frequency, is much greater than the fundamental frequency, the harmonics in both synchronous and asynchronous PWM become small.
(4) In the unipolar switching strategy, the switching frequency is effectively doubled, compared with bipolar switching. As a result all the harmonics are raised to a higher frequency range, further from the fundamental signal frequency.

The above analysis suggests that the switching frequency has to be much above than the maximum frequency of the control signal, and that, under this condition, the linear relationship between the converter control and average output voltage may be retained.

### 6.4 CHOICE OF SWITCHING FREQUENCY

Harmonic analysis indicates that the switching frequency of the H-bridge converter should be as high as possible to give the best drive performance. By taking other system considerations into account, the lower limit of the switching frequency can be established:

1. It should be as high as possible, in order to make use of the inherent low-pass filtering characteristics of the torque motor.
2. It should be much higher than the maximum frequency of the effective signals appearing in the converter or, equivalently, the bandwidth of control system. This implies that the switching operation will have little effect on the overall closed loop system. From Chapter 4, the bandwidth of the close loop control system was seen to be around 1 kHz, and the switching frequency should be at least 20 kHz to avoid audible noise.
3. It should be much higher than the sample frequency, when digital control is employed. Considerations of the system bandwidth indicates a sample frequency of about 10 kHz, and the switching frequency should be at least an order of magnitude larger, i.e., 100 kHz. A switching frequency much higher than the sample frequency ensures the control operations are effectively carried out after each sampling.
However, the converter is subjected to a number of practical limitations, which may be used to establish the upper limit to the switching frequency:

1. Nonlinear effects on the voltage gain caused by the dead time are proportional to the switching frequency [52].
2. Digital PWM schemes impose an inherent limit on the maximum switching frequency, due to the limited speed and finite word length of the microprocessor [60]. For instance, a switching frequency of 100 kHz would require the microprocessor to operate at a clock frequency of 25 MHz (a period of 40 ns) to achieve a 8-bit resolution.
3. The switching loss is proportional to the switching frequency and this will result in a reduced converter efficiency at high frequency switching.

The above considerations indicates that a high switching frequency satisfies some of these considerations while contradicting others and, as a compromise choice, a switching frequency of 100 kHz was chosen. A frequency significantly higher or lower than this, will either affect the converter performance, or have serious practical difficulties in implementation, as shown below.

6.5 THE EXPERIMENTAL H-BRIDGE CONVERTER [63,64,65]

In developing the experimental H-bridge converter, it was necessary to determine the switching devices and other components that were to be used, together with the converter circuit configuration, gate drive circuits, etc. These all directly determine the drive performance of the converter, and are discussed below.

6.5.1 Switch Devices: Power MOSFETs

At a switching frequency of 100 kHz, power MOSFETs are the obvious choice for the converter switches. A power MOSFET has a very fast switching time (less than 100 ns), allowing very high switching operation. It is a voltage-controlled device that requires a simple gate drive circuit with relatively small current. It has also a wide
Safety Operating Area (SOA) and the complete absence of the second breakdown suffered by BJTs, thus gaining great ruggedness of operation. Its excellent thermal stability, due to a positive resistance temperature coefficient, leads to a switching time that does not display any temperature dependency. Fig. 6.9 shows typical current-voltage characteristics.

6.5.2 Power Circuit

Each leg of the converter shown in Fig. 6.10 is formed by two switches, with a P-channel MOSFET in the top limb and an N-channel MOSFET in the bottom limb. This arrangement simplifies the gate drive circuit and eliminates the need for isolated gate drive circuits, which are necessary if the same bridge converter is formed using only N-channel MOSFETs. The input to each drive circuit has a delay circuit, which generates a short dead time, to eliminate current shoot-through during normal operation.

A rectifier diode is connected in series with each switching device, and a fast recovery diodes is connected in anti-parallel with the combination. The series rectifier blocks the flow of current in the body drain diode of the MOSFET, so that the freewheeling current is forced to flow through the external fast recovery diode, and the reverse recovery characteristics of the MOSFET, which has inherently slow dynamics, is therefore that of the fast recovery diode.

6.5.3 Choice of the Power MOSFETs

The choice of MOSFETs is primarily concerned with their power rating and switching characteristics. The motor drive requires a maximum ±40 V dc voltage supply with a maximum ±0.5 A output current, and the power consumption is therefore relatively small. The important parameter is the static drain-source on-state resistance $R_{DS}$, with a low value, indicating not only a high current handling capability, but also a low voltage drop across the switch. In addition, a small $R_{DS}$ results in a low conduction loss and consequently, a heat sink may not be necessary.
A more demanding requirement is that the electrical characteristics of the N-channel and P-channel MOSFETs must match closely, although a perfect match is practically impossible.

Table 6.1 shows the main electrical characteristics of the N-channel Power MOSFET IRF520 and its P-Channel counterparts IRF9520, which were considered for use in the motor drive. It is seen that the pair have closely matched switching characteristics, e.g., turn-on and turn-off times, and total gate charge, which are of considerable importance in high frequency switching circuits. The effects of different values of $R_{ds}$ can be ignored due to the small motor drive current.

### 6.5.4 External Freewheeling Diodes and Series Rectifiers

The reverse recovery times of the IRF520 and IRF9520 shown in Table 6.1 are 280 and 230 ns, which apparently cannot satisfy the present application. The BYW80-150 fast recovery diodes, with a reverse time of 35 ns, a reverse breakdown of 150 V and forward current of 8 A, were therefore used for both the freewheeling diodes and series rectifiers.

### 6.5.5 Gate Drive Circuits

Fig. 6.11 shows the gate drive circuits for the MOSFETs in one leg of the inverter. For the N-channel MOSFET driver, powered by a 15 V DC supply, two transistors form a complementary emitter follower stage (i.e. a totem pole circuit), with the output connected through a low value resistor to the gate of the MOSFET. The P-channel MOSFET drive includes a level shift to reference the drive signal to the positive rail of the main power supply. In order to gain the switching speed, another complementary emitter follower stage is arranged to ensure sufficient base current for the transistor being used as a level shift. Two potentiometers are included to ensure the best switching turn-on and turn-off performance to be achieved. Only a single +15 V DC supply is needed for the drive circuits, whereas a +5 V DC is normally available for the TTL control logic circuits.
The choice of transistors for the gate drive circuit depends on the total gate charge for the IRF520 and IRF9520 devices, and Table 6.1 shows that in both cases $Q_g = 10 \text{nC}$. Assuming the switching time $t_s = 100 \text{ ns}$, the charging current for the devices is then
\[ I_G = \frac{Q_c}{t_c} = \frac{10 \times 10^{-9}}{100 \times 10^{-9}} = 0.1A \] (6.13)

and it is clear that it is possible to drive the MOSFET even faster if the drive current is increased.

The npn-transistor ZXT451 and its complementary pnp-ZXT551 specified below were chosen for use in the gate drive circuits.

ZXT451: \( I_{c(\text{max})} = 1.5 \text{ A}, \ V_{ce(\text{max})} = 60 \text{ V}, f_c = 5.5 \text{ MHz} \)

ZXT551: \( I_{c(\text{max})} = -1.5 \text{ A}, \ V_{ce(\text{max})} = -60 \text{ V}, f_c = 5.5 \text{ MHz} \)

### 6.5.6 Time Delay Circuits

Fig. 6.12 presents a diagram of the time delay circuit, together with its operating waveforms. The rising edge of the PWM signal input is used to trigger the monostable circuit. The negative output of the monostable with a time delay \( \Delta t \) at its rising edge is obtained. The same principle is applied to generate a delay time \( \Delta t' \) for the complementary PWM signal, but using another monostable. In this way, the 'off' periods of the corresponding two complementary PWM signals are effectively extended for an extra interval of time \( \Delta t \) and \( \Delta t' \), required for converter operation, and \( \Delta t \) is normally made equal to \( \Delta t' \).

As the converter operates at high frequency, it is vital to make the dead time as short as possible to minimize any nonlinear effects, and use of the monostable 74LS123 chip enables a dead time of a few nanoseconds to be achieved by adjusting the external RC network. Polystyrene capacitors and the multi-turn carbon potentiometers are used such that the generated time delay \( \Delta t \) has an excellent thermal stability.
6.6 PRACTICAL LIMITATIONS ON THE DRIVE PERFORMANCE OF THE H-BRIDGE CONVERTER

Although possessing a superior performance under idealized conditions, the practical limitations on the performance of the H-bridge converter may not be trivial, as analyzed below.

6.6.1 Linear Voltage Gain

The idealized linear voltage gain is significantly affected by the dead time, particularly when the switch frequency is high. Detailed investigations [52,66] indicate that the nonlinear effects brought about by the dead time are proportional to the switching frequency. The higher the switching frequency, the more severe is the nonlinearity in the output voltage, as shown in Fig. 6.13 and the following equations apply

\[ \Delta V_o = \frac{2\Delta t}{T_{sw}} V_s \quad i_o > 0 \quad (6.13) \]

and

\[ \Delta V_o = -\frac{2\Delta t}{T_s} V_{sw} \quad i_o < 0 \quad (6.14) \]

For the experimental system described in Section 6.5, and assuming \( V_s = 40 \) V, \( T_{sw} = 10 \mu s \) and \( \Delta t = 100 \) ns, the change in the average output voltage \( \Delta V_o \) is therefore \( \pm 0.8 \) V.

For a dc-to-ac converter, the instantaneous-average output voltage \( v_o(t) \) is shown in Fig. 6.14, where \( i_o \) is assumed to be sinusoidal and lagging behind \( v_o(t) \). The distortion in \( v_o(t) \) at the current zero-crossing is caused by the existence of the low-
order harmonics of the fundamental frequency signal due to the dead time introduced.

6.6.2 The Bandwidth

The bandwidth of the switch-mode H-bridge converter is influenced by several interrelated factors. The dependence on the switching frequency may be explained by examining the harmonic spectra shown in Figs. 6.7(c) and 6.8(c). The further away the harmonics are from the fundamental frequency component, the larger is the bandwidth of the converter, and a high switching frequency is generally beneficial to the system from the bandwidth point of view, since the harmonics are effectively raised to the high frequency range where they may more easily be eliminated by an external filter. However, the switching frequency cannot be too high due to the existence of a dead time, and the bandwidth is thereby limited. Again, the requirement of retaining a linear voltage gain is in conflict with that of achieving a large bandwidth.

Additionally, the bandwidth will be considerably influenced by the limited resolution that the micro-controller can provide when a software controlled PWM scheme is employed. Even with a high performance DSP (as is shown in Chapter 7), a switching frequency of 100 kHz will restrict the resolution to only 8-bits for the H-bridge converter.

6.7 SUMMARY AND COMPARISON OF THE LINEAR AND SWITCH-MODE POWER AMPLIFIERS

In Chapter 5 and 6, the analysis and design details of both a linear and switch-mode power amplifiers were presented. The main requirement of the power amplifier, from the point of view of the overall performance of the control system, is a linear voltage gain over a wide frequency range, whereas the drive current and as well as power consumption are insignificant factors. The linear amplifier provides a drive
option with the excellent performance. It requires only a simple interface with the micro-controller and generally has a wide frequency bandwidth for linear voltage amplification. The shortcomings are that a heat sink is required and the cost may be high.

The switch-mode amplifier was investigated as an alternative to the linear amplifier, with the aim of improving the overall system performance/cost, e.g., eliminating the heat sink, and increasing the bandwidth. The H-bridge converter was suitable for the drive because of its inherent linear voltage gain, which may not be available in other types of four-quadrant switch-mode converters [67,68]. The critical condition for the ideal drive performance is that the switching frequency must be considerably higher than the maximum system frequency. In practice however, this is limited by the presence of the dead time required for the H-bridge converter. The compromise choice of the switch frequency used in the experimental design was 100 kHz, although the nonlinear effects on the voltage gain and subsequently bandwidth reduction were evident. A further limitation came from the limited resolution in the microprocessor when the digital PWM scheme was considered.

In conclusion, because of its considerable overall advantages the linear amplifier was used in the closed-loop experimental study, described in the following chapters.
Chapter 6

Drive Strategy Two: Switch-Mode Power Amplifier

Fig. 6.1 H-bridge dc-dc converter

(a) bipolar switching

(b) unipolar switching

Fig. 6.2 Diagram of the PWM modulator
Chapter 6  Drive Strategy Two: Switch-Mode Power Amplifier

Fig. 6.3 Various idealized waveforms of bipolar strategy
Chapter 6  Drive Strategy Two: Switch-Mode Power Amplifier

(a) First-quadrant operation  
\[ v_o > 0 \quad i_o > 0 \]

(b) Second-quadrant operation  
\[ v_o < 0 \quad i_o > 0 \]

(c) Third-quadrant operation  
\[ v_o < 0 \quad i_o < 0 \]

(d) Fourth-quadrant operation  
\[ v_o > 0 \quad i_o < 0 \]

Fig. 6.4 Four-quadrant operation of bipolar switching
Fig. 6.5 Various idealized waveforms of unipolar strategy
Chapter 6  

Drive Strategy Two: Switch-Mode Power Amplifier

Fig. 6.6 Four-quadrant operation of unipolar switching

(a) First-quadrant operation

\[ v_o > 0, \quad i_o > 0 \]

(b) Second-quadrant operation

\[ v_o < 0, \quad i_o > 0 \]

(c) Third-quadrant operation

\[ v_o < 0, \quad i_o < 0 \]

(d) Forth-quadrant operation

\[ v_o > 0, \quad i_o < 0 \]
Chapter 6 Drive Strategy Two: Switch-Mode Power Amplifier

(a) the PWM modulation

(b) output voltage

(c) harmonic spectrum

Fig. 6.7 Converter harmonics for bipolar switching
Chapter 6

Drive Strategy Two: Switch-Mode Power Amplifier

(a) the PWM modulation

(b) output voltage

(c) harmonic spectrum

Fig. 6.8 Converter harmonics for unipolar switching
Chapter 6

Drive Strategy Two: Switch-Mode Power Amplifier

(a) output characteristics

(b) transfer curve

Fig. 6.9 The MOSFET current-voltage characteristics
Fig. 6.10 Converter circuit with the complementary P- and N-channel MOSFET pair and direct gate drive

Fig. 6.11 Gate drive circuits for one leg of the converter
Fig. 6.12 Time Delay Circuits
Fig. 6.13 Effect of the dead time \( \Delta t \) on the linear voltage gain

Fig. 6.14 Effect of the dead time \( \Delta t \) on the sinusoidal output
Chapter 7

The DSP-Based Drive Control System

To implement the control scheme proposed in Chapter 4 necessitates a high performance drive control system, which will comprise a microprocessor-based hardware and optimized software. A complete experimental system centred around a Digital Signal Processor (DSP) was developed, with the TMS320E14 chosen as the core of the controller hardware, due to its advantageous architecture, excellent performance and various on-chip control peripherals. The controller, designed in the continuous-time domain, was converted into digital form using the bilinear transform with the δ-operator, which is most suitable for a fast sampling system. The discrete implementation of gain-scheduled control was achieved by developing a schedule table, which is used to update continuously the controller parameters. Control software was designed using the structure programming methodology. The program code, written in the efficient assembly language, was debugged, tested, and then programmed into the DSP on-chip EPROM using the TI TMS3201x Development System. A high sample frequency of 10 kHz was used in the analog-to-digital conversion, to ensure that the control operations were carried out in an accurate, effective and efficient way.

7.1 THE TMS320C14/E14 DSP

The TMS320C14 and TMS320E14 are both members of Texas Instruments (TI) first-generation TMS320 DSP family [69]. They are the first devices that combine the high performance of a DSP with the on-chip peripherals of a microcontroller [70,71], and are therefore particularly suitable for control applications.

Fig. 7.1 shows the functional block diagram outlining the principle hardware structure of the TMS320C14/E14 devices, and the main features are summarized below.

- 160 ns instruction under the full clock frequency 25.6 MHz;
- 256 16-bit word on-chip data RAM;
• 4K 16-bit on-chip program ROM (C14), or EPROM (E14);
• EPROM code protection for copyright security;
• 4K 16-bit word total external memory at full speed (micro-processor mode):
• 16-bit x 16-bit multiplier with a 32-bit product;
• 32-bit Arithmetic Logic Unit (ALU);
• 32-bit Accumulator with the overflow mode, to emulate the effect of saturation in the analog system;
• 0 - 16-bit barrel shifter;
• 16-bit bi-directional data bus with 50-Mbps transfer function;
• 16-bit selectable I/O port;
• Serial port with programmable protocols;
• Event manager with capture inputs and compare outputs, used for PWM outputs;
• Four independent programmable timers (1 watchdog, 2 general purpose timer and 1 serial port timer);
• 15 external/internal interrupts.

It is seen that the TMS320C14/E14 has integrated into a single chip almost all the peripherals necessary for digital control, except for the A/D and D/A converters. However, this does not impose any difficulties, as they can be added externally to the DSP devices, and in the case of the PWM drive output the D/A converter may not be required. Furthermore, the TMS320E14 is the EPROM version of the TMS320C14, which has 4K on-chip EPROM, thus eliminating any need for external memory devices and their associated control circuits. Detailed descriptions of the TMS320C14/E14 are given in [72].

7.2 HARDWARE DEVELOPMENT

7.2.1 Hardware Configuration

Fig. 7.2 presents the hardware configuration of the control system based on the TMS320E14 DSP.
The control system may be configured to drive either a linear or switch-mode power amplifier. When the linear amplifier is needed, the digital control signal is output via a D/A converter and, when a switch-mode amplifier is used, the PWM signals generated by the DSP Compare Subsystem are sent to the drive circuits of the H-bridge converter formed by power MOSFETs as described in Chapter 6.

A 50 Hz sawtooth position reference generated from a programmable signal generator is supplied to the system via the Feedback and Signal Conditioning Circuits, which also receive and condition both the motor position and current feedback signals. The current, position, and position error (which is the difference between the reference and position feedback) are then sampled and converted into discrete signals by an A/D converter for processing in the DSP.

The TI TMS3201x Development System [73] was used to write, debug and test the control software. The drive control system may operate at full speed under the TMS320E14 based 'Emulation' mode, with the object code downloaded to the Emulator using the window-driven menu in the PC monitor. Alternatively, the DSP system may be linked to the PC through an RS 232 serial interface, which enables the PC to be used as a host machine to assist the tuning of the controller.

### 7.2.2 System Clock, Reset and Power Supply

Fig. 7.3 shows the quartz crystal oscillator circuit, which provides an external 25 MHz clock signal with 50% duty cycle via the CLKIN pin. The effective clock frequency used by the DSP is one fourth of the CLKIN frequency, and is available at the CLKOUT pin for external use.

As shown in Fig. 7.4, an RS flip-flop, controlled by a miniature toggle switch connected to its input, is used to activate the RESET function. The DSP is powered by an on-board 5 V DC supply, derived from an integrated DC supply chip LM7805.

The DIP Array uses a set of switches connected to the I/O port, which were intended
Chapter 7

The DSP-Based Drive Control System

to aid the development of the control program using the Capture Subsystem available in the DSP.

7.2.3 Analog-to-Digital Conversion

Analog-to-digital conversion is of vital importance to the digital signal processing and digital control system performance. Two high performance A/D converters AD7870 are used to convert the analog feedback signals into digital ones. This device combines a 12-bit ADC with an internal clock, a built-in sample-and-hold amplifier and reference on a single chip, and can operate at a maximum throughput frequency of 100 kHz, or 10\(\mu\)s conversion time (2\(\mu\)s for sample-and-hold, and 8\(\mu\)s for successive approximation). Its data access time of only 57 ns enables it to interface directly with the high speed DSP, minimising the delay time in the A/D circuit path. Fig. 7.5 shows a functional diagram of the AD7870 together with the timing diagram for one of its interface modes with the 12-bit parallel data output. In this mode, the conversion is initiated by a low going pulse on the \(\overline{{\text{CONV}}}\) input, and the rising edge of this pulse starts the conversion by driving the track/hold amplifier into its hold mode. The \(\overline{{\text{INT}}}\) line can be used to interrupt the DSP. The corresponding read operation to the device accesses the data, and the \(\overline{{\text{INT}}}\) line is reset to high on the falling edge of \(\overline{{\text{CS}}}\) and \(\overline{{\text{RD}}}\). Additional I/O ports, IOP\(_0\) and IOP\(_1\) are connected to the \(\overline{{\text{CS}}}\) (chip enable) of the A/D converters, to enable the chip when a conversion is completed.

7.2.4 Digital-to-Analog Conversion

The Digital-to-Analog Converter AD767 is given a complete 12-bit conversion function, by including an on-chip output amplifier to provide a maximum voltage of \(\pm 15\) V. The 40 ns write pulse enables the converter to be compatible with the fastest microprocessors and DSPs. The AD767 is initiated by a low-going signal on its \(\overline{{\text{CS}}}\) pin connected to the \(\overline{{\text{WCONV}}}\) signal of the Address Decode Logic described below.
Chapter 7  The DSP-Based Drive Control System

7.2.5 Address Decode Logic

Conventional address decode devices, such as 74LS138 and 74LS154, are too slow to operate directly within the timing constraints of the DSP address and data bus. High speed TTL logic gates are therefore used to combine the RD (read) and WR (write) signals with the two least significant address lines A₀ and A₁, to provide the logic signals controlling the operations of the A/D and D/A converters. Fig. 7.6 shows the circuit diagram of the address decode logic, and Table 7.1 gives the truth table for the Address Decode Logic. Advanced Schottky (AS) devices, which have a switching time of less than 5 ns, are used for these time critical circuits.

Table 7.1 Truth table for Address Decode Logic

<table>
<thead>
<tr>
<th>Input (from DSP)</th>
<th>Output (to A/D Converter)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₁</td>
<td>A₀</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Note: x can be either logic 0 or 1.

7.2.6 Multiplexer and Control Signals

The system was designed to accommodate more than two channels of the analogue inputs, with an 8-channel analogue multiplexer 74HCT4051 controlled by the DSP at the given instants, switching the A/D converter to the specified loop. Control signals from the I/O port of the DSP (IOP₅, IOP₆, and IOP₇) are used to control the
multiplexer via its address data signals A and B and control $\overline{INH}$. While the analogue signals (the current, position and position error) are connected to the input terminals $Y_0$, $Y_1$, and $Y_2$.

### 7.2.7 PWM Signal Generator and Interface Circuits

Fig. 7.7(a) shows the architecture of the high precision PWM mode in the DSP Compare Subsystem, which is software-controlled by setting the Timer Control (TCON) register. In this mode, each of the six output pins is uniquely associated with one Compare and Action register. The pulse width of each PWM signal is determined by the associated Compare register, while the overall period is determined by the selected timer period register (either Timer 1 or Timer 2). When the value of the 14 Least Significant Bits (LBS) of the selected timer, which is clocked by CLKOUT (with a period of 160 ns), matches the 14 Most Significant Bits (MSBs) of the compare register, the two LSBs of the specified compare register are used to count the number of CLKIN pulses (with a period of 40 ns) before the associated compare (CMP) pin is reset. In this manner, the resolution of the PWM is increased by a factor of four (ie: minimum pulse width is 40 ns), as shown in Fig. 7.7(b). Table 7.2 gives the relationships between the switching frequency and the resolution bits in the high precision PWM mode.

High speed ICs 74HCT04 are used as the buffers to interface the DSP with the gate drive circuits of the MOSFETs.

<table>
<thead>
<tr>
<th>PWM frequency (kHz)</th>
<th>Bits of resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>8</td>
</tr>
<tr>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>6.25</td>
<td>12</td>
</tr>
<tr>
<td>1.5</td>
<td>14</td>
</tr>
</tbody>
</table>

Table 7.2 Relationship between switching frequency and resolution
Table 7.2 indicates clearly that the PWM resolution becomes lower with an increase in switching frequency, and that at a switching frequency of 100 kHz the resolution is only 8 bits, which is significantly lower than that the 12 bits of the D/A converter.

7.2.8 RS232 Serial Port and Interface Circuits

The DSP provides an RS232 communication interface with the pins TXD and RXD. These signals are TTL compatible and are converted via the MAX232C to RS232 logic levels ("1" = -9 V, "0" = +9 V), to connect to the serial port of a PC. Fig. 7.8 shows the connections for a "null-modem" cable to link the computer and the DSP. The asynchronous mode controlled by the on-chip Serial Port Control Register is used for communication between the PC and the DSP. Fig. 7.9 shows the configuration of the serial port for the asynchronous mode.

7.2.9 Feedback and Signal Conditioning Circuits

The JFET-input operational amplifiers TL071 and TL072, which feature low input bias, offset current and fast slew rate, are used to construct both feedback and signal conditioning circuits [55].

Fig. 7.10 shows the circuit employed for position feedback, position error and signal conditioning. The position error signal is obtained by subtracting position feedback signal from the position reference signal, which is produced by an external generator. Voltage followers are used at the input and output of the conditioning circuits, to increase the input impedance and reduce the output impedance.

Fig. 7.11 shows the current feedback and signal conditioning circuits. The differential current signal, which is sensed through a small resistor connected in series with the motor, is amplified and converted via an instrumentation amplifier to a single-ended analogue signal amplifier. The monolithic integrated circuit INA111, replacing the standard three operational instrumentation amplifier, offers excellent performance and eliminates any need to use highly matched precision resistors.
Fig. 7.12 shows the circuit for conditioning the control signal, which is output from the D/A converter and supplied to the power amplifier.

### 7.3 DEVELOPMENT OF THE DIGITAL COMPENSATORS

The controller designed in the continuous-time domain was converted into a set of equivalent discrete equations by the bilinear transform with the \( \delta \)-operator [45,74]. The necessity for using this operator is associated with the high coefficient sensitivity matrix identified as existing in the conventional shift \( z \)-operator [75,76,77]. When the modified canonic \( \delta \)-form structure is used, the main benefits include a simpler algorithm and a shorter coefficient word-length. These lead to the fast execution of arithmetic routines and therefore a higher sample rate, which is essential for improving the overall system performance with a minimum quantisation error [77,78].

#### 7.3.1 The Principle of the \( \delta \)-Operator

The \( \delta \) operator is defined as

\[
z = \delta + 1
\]

or

\[
\delta = z - 1
\]

therefore,

\[
\delta^{-1} = \frac{1}{z - 1} = \frac{z^{-1}}{1 - z^{-1}} = \frac{u_o(z)}{u_i(z)} \quad (7.2)
\]

Eqn. (7.2), illustrated by Fig. 7.13, indicates that \( \delta^{-1} \) is an accumulator: the quantity to be read into RAM at each sampling interval is the sum of the latest sample \( U_i \) and the previous summation \( U_o \) fetched from RAM and stored in the accumulator.
7.3.2 The Structure of the \( \delta \)-Controller

The general form of first- and second-order controllers may be written in the \( s \)-domain as

\[
G_1(s) = \frac{n_0 + n_1s}{1 + m_1s} \quad (7.3)
\]

and

\[
G_2(s) = \frac{n_0 + n_1s + n_2s^2}{1 + m_1s + m_2s^2} \quad (7.4)
\]

On using the bilinear transform expressed in terms of \( \delta \), that is

\[
s = \frac{2\delta}{T(2 + \delta)}
\]

or

\[
\delta = sT \quad (7.5)
\]

From this, the discrete transfer functions in the \( \delta \)-operator form for a first-order controller is

\[
G_1(\delta) = \frac{c_0 + c_1\delta^{-1}}{1 + r_1\delta^{-1}} \quad (7.6)
\]

and for a second-order controller

\[
G_2(\delta) = \frac{c_0 + c_1\delta^{-1} + c_2\delta^{-2}}{1 + r_1\delta^{-1} + r_2\delta^{-2}} \quad (7.7)
\]

Fig. 7.14 show diagrams for the above equations in canonic \( \delta \)-form. A modified
structure may be obtained, if the feedback coefficients of Fig. 7.14 are moved into the forward path of the controller, with appropriate changes to the coefficients which form the output $y$. These are shown in Fig. 7.15, with the resultant equations being given in Eqns. 7.8 and 7.9.

The relationships between the coefficients of Eqns. 7.3 and 7.4 and those of the modified canonic $\delta$-transfer functions are summarized in Tables 7.3 and 7.4 [77].

$$G'_1(\delta) = \frac{p + d_1q\delta^{-1}}{1 + d_1\delta^{-1}}$$ \hspace{1cm} (7.8)

and

$$G'_2(\delta) = \frac{p + d_1q\delta^{-1} + d_1d_2r\delta^{-2}}{1 + d_1\delta^{-1} + d_1d_2\delta^{-2}}$$ \hspace{1cm} (7.9)

Where $G'_1(\delta)$ and $G'_2(\delta)$ are the modified canonic $\delta$-transfer functions of the first- and second-order controller.

**Table 7.3** Emulation table for first-order $\delta$-controller

<table>
<thead>
<tr>
<th>$G_1(s) = \frac{n_0 + n_1s}{1 + m_1s}$</th>
<th>$G'_1(\delta) = \frac{p + d_1q\delta^{-1}}{1 + d_1\delta^{-1}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p = \frac{n_0T + 2n_1}{T + 2m_1}$</td>
<td>$n_0 = q$</td>
</tr>
<tr>
<td>$q = n_0$</td>
<td>$n_1 = T\left(\frac{p}{d_1} - \frac{q}{2}\right)$</td>
</tr>
<tr>
<td>$d_1 = \frac{2T}{T + 2m_1}$</td>
<td>$m_1 = T\left(\frac{1}{d_1} - \frac{1}{2}\right)$</td>
</tr>
</tbody>
</table>
Table 7.4 Emulation table for second-order $\delta$-controller

<table>
<thead>
<tr>
<th>$G_2(s) = \frac{n_0 + n_1s + n_2s^2}{1 + m_1s + m_2s^2}$</th>
<th>$G_2'(\delta) = \frac{p + d_1q\delta^{-1} + d_1d_2r\delta^{-2}}{1 + d_1\delta^{-1} + d_1d_2\delta^{-2}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p = \frac{n_0T^2 + 2n_1T + 4n_2}{T^2 + 2m_1T + 4m_2}$</td>
<td>$n_0 = r$</td>
</tr>
<tr>
<td>$q = \frac{n_0T + n_1}{T + m_1}$</td>
<td>$n_1 = T\left(\frac{q}{d_2} - r\right)$</td>
</tr>
<tr>
<td>$r = n_0$</td>
<td>$n_2 = T^2\left(\frac{p}{d_1d_2} - \frac{q}{2d_2} + \frac{r}{4}\right)$</td>
</tr>
<tr>
<td>$d_1 = \frac{4T^2 + 4m_1T}{T^2 + 2m_1T + 4m_2}$</td>
<td>$m_1 = T\left(\frac{1}{d_2} - 1\right)$</td>
</tr>
<tr>
<td>$d_2 = \frac{T}{T + m_1}$</td>
<td>$m_2 = T^2\left(\frac{1}{d_1d_2} - \frac{1}{d_2} + \frac{1}{4}\right)$</td>
</tr>
</tbody>
</table>

Note: $T$ is the sample time.

7.3.3 Choice of Sample Frequency

The sample frequency must be considered carefully in any digital control system. As the present closed-loop system bandwidth is designed to be around 1 kHz, as analyzed in Chapter 4, the sample frequency should be set above 10 times the bandwidth [79,80], or 10 kHz. However, the upper limit of the sample frequency depends largely on the algorithm computation and on the DSP speed. In the present system, the control algorithms include a number of compensators in both the current and position loops, including an adaptive gain-scheduled controller, and the DSP operates at its full speed of 25 MHz, corresponding to an instruction cycle of 160 ns. The estimated computing time required for the algorithms, indicated that the sample
7.3.4 Emulation of the Controller [77,81]

Based on the emulation tables of the previous section, the continuous s-domain transfer functions of various compensator designs may be transformed to the δ-form, and these are given below. A sample time of 100 µs is used.

(1) notch compensator for position loop:

\[
G_N(\delta) = \frac{p_N + d_{N1}q_N\delta^{-1} + d_{N1}d_{N2}r_N\delta^{-2}}{1 + d_{N1}\delta^{-1} + d_{N1}d_{N2}\delta^{-2}} \tag{7.10a}
\]

(2) lag compensator for position loop:

\[
G_G(\delta) = \frac{p_G + d_Gq_G\delta^{-1}}{1 + d_G\delta^{-1}} \tag{7.10b}
\]

(3) first lead compensator for position loop:

\[
G_{L1}(\delta) = \frac{p_{L1} + d_{L1}q_{L1}\delta^{-1}}{1 + d_{L1}\delta^{-1}} \tag{7.10c}
\]

(4) second lead compensator for position loop:

\[
G_{L2}(\delta) = \frac{p_{L2} + d_{L2}q_{L2}\delta^{-1}}{1 + d_{L2}\delta^{-1}} \tag{7.10d}
\]

(5) lead compensator for current loop:
$$G_f(\delta) = \frac{p_i + d_iq\delta^{-1}}{1 + d_i\delta^{-1}}$$ (7.10e)

### 7.3.5 Digital Algorithms

The digital algorithms for the general first- and second-order $\delta$-controller derived from Eqns. (7.8) and (7.9) are summarized in Tables 7.5 and 7.6. These can be directly applied to the above compensators for programming the control code.

**Table 7.5 Algorithm for first-order $\delta$-controller**

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$v = u_i - w$</td>
</tr>
<tr>
<td>2</td>
<td>$y_o = pv + q_1w$</td>
</tr>
<tr>
<td>3</td>
<td>$w = w + d_1v$</td>
</tr>
</tbody>
</table>

**Table 7.6 Algorithm for second-order $\delta$-controller**

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$v = u_i - w - x$</td>
</tr>
<tr>
<td>2</td>
<td>$y_o = pv + qw + rx$</td>
</tr>
<tr>
<td>3</td>
<td>$x = x + d_2w$</td>
</tr>
<tr>
<td>4</td>
<td>$w = w + d_1v$</td>
</tr>
</tbody>
</table>
7.4 IMPLEMENTATION OF GAIN-SCHEDULED CONTROLLER

A first-order gain-scheduled controller was developed to compensate for the nonlinear variations in the motor stiffness. Implementation of the controller requires the development of a schedule table, by which the nonlinear stiffness variation with the rotor position is related directly to the adaptation of the controller. The data stored in the table is then used to update the controller parameter in synchronism with the periodic scanning of the motor, to achieve accurate control over the rotor position.

7.4.1 Emulation of Gain-scheduled Controller

The principle of the first-order gain-scheduled controller was analyzed in Chapter 4, with its transfer function given in Eqn. 4.7 as

\[
G_s(s) = \frac{s + k(\theta)\omega_0}{s + \omega_0} \quad (7.11)
\]

where \(\omega_0\) is the corner frequency and \(k(\theta)\) the parameter varying with the motor position \(\theta\). Using Emulation Table 3, the discrete form of the controller in the \(\delta\)-operator is obtained as

\[
G_s(\delta) = \frac{p_s + d_sq_s\delta^{-1}}{1 + d_s\delta^{-1}} \quad (7.12)
\]

in which the coefficients are

\[
p_s(k(\theta)) = \frac{k(\theta)\omega_0 + 2}{k(\theta)(\omega_0 + 2)} \quad (7.13a)
\]

\[
q_s = k(\theta) \quad (7.13b)
\]
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and

\[ d_s = \frac{2T\omega_0}{T\omega_0 + 2} \]  

(7.13c)

For a given sample time \( T \) and corner frequency \( \omega_0 \), the term \( d_s \) is a constant, while both \( p_s \) and \( q_s \) vary with \( k(\theta) \), which is the nonlinear function of the rotor position \( \theta \).

7.4.2 Control Algorithm

The algorithm for implementing the gain-schedule control is given in Table 7.7, where \( v_s \) and \( w_s \) are internal variables of the algorithm, \( K_c \) is a constant that is determined by the system performance, and \( a, b \) and \( c \) are constant coefficients determined by the nonlinear stiffness characteristics. The nonlinear function \( k(\theta) \), described in Chapter 3, was found as the best fit to the experimental curve.

<table>
<thead>
<tr>
<th>Table 7.7 Gain-scheduled control algorithm</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v_s = u_i - w_s ) \hspace{1cm} (1)</td>
</tr>
<tr>
<td>( y_o = p_s(k(\theta))v_s + q_s(k(\theta))w_s ) \hspace{1cm} (2)</td>
</tr>
<tr>
<td>( w_s = w_s + d_s v_s ) \hspace{1cm} (3)</td>
</tr>
<tr>
<td>( k(\theta) = K_c \frac{d}{d\theta} (T_s(\theta)) ) \hspace{1cm} (4)</td>
</tr>
<tr>
<td>( T_s(\theta) = \frac{a+b\theta^2}{1+c\theta^2} \theta ) \hspace{1cm} (5)</td>
</tr>
</tbody>
</table>

7.4.3 Schedule Table

It is very difficult in practice to calculate on-line within the sample interval the algorithm of Table 7.7, which is the combination of a standard first-order \( \delta \)-controller
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with a high-order nonlinear function. However, this can be effectively overcome by developing a schedule table, in which each value of the varying parameter \( k(\theta) \) corresponding to a given position, is pre-calculated and stored. At any instant, the correct value of \( k(\theta) \) can be used to update the controller and, in this manner, the controller is able to adapt itself rapidly, without overloading the DSP with extra computation.

The data for the reference position, which is available in the form of a time sequence waveform, is used to carry out the off-line calculation for the schedule time, and this does not cause any problems, as the actual position is very close to the reference position in the steady-state. Fig. 7.16 shows the complete procedure for developing the schedule table. Consideration of both the reference period of 20 ms and the sample time of 100\( \mu \)s indicates that the table will have 200 data point, and this can represent the continuous nonlinear curve with good accuracy and smoothness. The constant coefficient \( K_c \) is set to 10.

7.4.4 Position Synchronous Control

As the position reference is provided externally to the drive control system, it is vital to employ synchronous control to ensure that the application of the gain-scheduled controller will not cause instability. Fig. 7.17 shows that the first element \( k(0) \) in the table, which has the minimum value of the nonlinear function (curve A), should correspond to the zero-crossover point with the positive slope at \( t=t_0 \) in the position response, to achieve a satisfactory performance. With curve B chosen to be out of phase with the sawtooth, the system will be less stable or even unstable, due to the sudden addition of an excessively large gain at the incorrect time instant. Theoretically, the maximum gain provided by the gain-scheduled controller should coincide with both the extreme positions of \( \pm 10^\circ \). A control mechanism is therefore required to detect continuously the position response, in order to establish the precise time instant at which the gain-scheduled controller is applied, and this can be realized by the software controlled logic given in the next section.
7.5 CONTROL SOFTWARE DESIGN AND PROGRAMMING

The control software was designed using the top-down structured programming methodology [82,83], in which each module represents a real-time task at a given level, and may consist of several levels of sub-modules. It is convenient to modify or remove a module or sub-module without affecting the others, and this ensures a reliable, safe and correct software source code. The mixed use of both the flow chart and program structure diagrams gives a clear description of the real-time characteristics and multi-level hierarchical structure of the control software.

7.5.1 Software Structure

Fig. 7.18 shows the overall software structure. The program first initializes various system constants, variables, registers and on-chip peripherals, and after activating the system timer interrupt it moves to a loop, in which the controller equations are repeatedly executed when a timer interrupt is generated. The timer interrupt can be directly routed to the CPU by appropriately initializing the Interrupt Mask (IM) register and Interrupt Mode register INTM. The CPU responds immediately by branching to the Interrupt Routines Service (IRS). There is no need to execute a repeated code, which is conventionally associated with a software-control interrupt and this results in the accurate sample period essential for high speed real-time control.

7.5.2 Interrupt Routines Service (IRS)

Fig. 7.19 shows a diagram for the Interrupt Routines Services (IRS), which at its top level consists of five main module blocks, namely A/D Conversion, Position Loop Algorithm, Scale and Overflow Check, and D/A Conversion. The use of a Program Structure Diagram, instead of a Flow Chart, describes explicitly lower levels of the software. The A/D Converter converts the analog feedback signals into digital ones, which are used to compute both the position and current loops, and Scale and Overflow Checks are performed on computed results before they are converted back
to analog signals via a D/A converter. All the modules are executed 'from top to bottom' and 'from left to right'. A lowest level of module in each branch will correspond to a source code, and it is therefore convenient to verify the design level-by-level and module-by-module.

7.5.2.1 Analog-to-Digital Conversion

Fig. 7.20 shows the flow chart for the A/D Conversion module. After a start command is initiated, the program enters a loop to wait for the completion. This may be either signalled by using the interrupt line INT on the A/D converter to request a CPU interrupt, or controlled by software which sets the sample time in the program. The output of the A/D converter is a 12-bit complement number, and this is converted to a 16-bit complement number by a 4-bit left shift operation.

7.5.2.2 Position loop algorithms

The overall Position Loop Algorithm is shown in Fig. 7.21. The Position Synchronous Control is realized by continuously checking the position feedback, to determine when the gain-scheduled controller should be added. When this condition is met the flag bit 'Schedule' is set, and the subsequent operations are controlled in synchronism with the shaft position.

The flow chart for the gain-scheduled controller is shown in Fig 7.22, and those for the various linear compensators are shown in Figs. 7.23 to 7.26.

7.5.2.3 Current loop algorithm

Fig. 7.27 shows the flow chart for the Current Loop Algorithm, comprising a first-order lead compensator. The current error is the difference between the output from the position loop algorithm and the current feedback signal obtained from the A/D converter.
7.5.2.4 Scale and overflow check

The scaling of the computed result is carried out by combining arithmetic left shift and additions with multiplications, and the overflow check is performed on the calculated result. The number of the shift bit, additions and the multiplying factor are determined by the adjustment of the loop gain due to the A/D and D/A conversions. Fig. 7.29 shows the flow chart for the scale and overflow check.

7.5.2.5 Digital-to-analog conversion

The scaled result in a 16-bit 2's complement code format is converted to an 12-bit offset code format, which is then written to the D/A converter to produce a ±15 V output voltage. Fig. 7.28 shows the flow chart for the conversion.

7.5.4 Numerical Routines

The realizations of the discrete algorithms given in Tables 7.5 to 7.7 are used to compute the compensations defined by Eqns. 7.10(a) to 7.10(e) and 7.12. These are essentially additions, subtractions and shift of the fixed-point variables, and multiplications of a fixed point variable by a coefficient, which is also in fixed-point format. The coefficient word-length is chosen as 16-bit, consistent with the DSP word-length, and the internal variable word-length chosen as 2x16-bit word. These guarantee both a high computational precision and a minimum dynamic algorithm error. Further, both the coefficient and internal variables are scaled down to be fractional numbers, which results in the fractional arithmetic suitable for implementation on the fixed point DSPs, such as the TMS320E14. Saturation arithmetic may be required, to check the overflow for the results of an addition, subtraction, or shift operation.

7.5.4.1 Multi-word multiplication

The multiplication algorithm is implemented as a two-word (32-bit) variable
multiplied by a one-word (16-bit) coefficient, and the resultant product is saved in a
two-word (32-bit) format. As both the variables and coefficients are specified as
fractional numbers, there will be no overflow in the product, thereby eliminating any
need for an overflow check for the multiplication. The MSB of the coefficient word
is always set to zero, which results in fast execution of the multiplication code. Fig.
7.29 shows the number format used and Fig. 7.30 the algorithm adopted.

7.5.4.2 Multi-word additions and subtractions

Two-word additions and subtractions are conveniently implemented in the 32-bit
accumulator. Care should be taken over the arithmetic operation of the least
significant 16-bit of the variables, which is specified as an unsigned number. An
overflow check is necessary for the arithmetic results. Fig. 7.31 shows the
algorithms implemented.

7.5.4.3 Arithmetic shift

Arithmetic shift is frequently required for scaling a variable, an intermediate or a
final result. The arithmetic left shift is used to scale up the intermediate results or
variables. In this case, the scaling factor is greater than 1 and saturation or overflow
is possible; the overflow check or saturation is therefore required for the detection of
such condition.

7.4.4.4 Saturation Arithmetic

Conventionally, saturation arithmetic is required in software to detect the overflow
for the intermediate and final results of the various operations. In the TMS320E14,
this is incorporated into the hardware, which has an Overflow Mode in its 32-bit
accumulator, giving a considerable reduction in the required saturation code. The
Overflow Mode is controlled by the instructions SOVM and ROVM, which set and
reset overflow bit OVM in the Status Register. When the OVM is set, and an
overflow occurs, the accumulator is automatically loaded with either a maximum
positive number (7FFFFFFF) or a maximum negative number (FFFFFFF), depending on the sign of the results. A single instruction BV is used to check the overflow bit (also in the Status Register) and, if the overflow bit is set (indicating the overflow occurs), the program branches to a location specified by the instruction.

7.5.5 Control Software Programming

The control source code was written exclusively in the DSP assembly language [72], and the various arithmetic routines were implemented using macros [84], which are sections of code repeatedly executed wherever referenced within the program. Although more object code is generated in assembling the source code program, overhead of stack operations required for the sub-routine calls is avoided. This is particularly suitable for programming the TMS320E14, which can accommodate easily a large control code, when using macros for the repeated arithmetic code, due to its program memory of 4Kx16-bit, but it would have difficulties in cope with a code requiring the use of sub-routine calls due to its limited four level stack.

The control code was debugged, tested and programmed into the DSP on-chip EPROM using the TI TMS3201x Development System, which provides various useful debugging capabilities, such as single step, trace/breakpoint, on-chip register status, full-speed emulations, disassembler, etc.. A full DSP Assembly source code is given in Appendix D.
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Fig. 7.1 Functional diagram of TMS320C14/E14
Fig. 7.2 Hardware Configuration of the TMS320 E14 DSP Based Control System
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**Fig. 7.3** The clock oscillator

![Clock Oscillator Diagram]

- $R_1 = 330\Omega$
- $R_2 = 330\Omega$
- Crystal: 25 MHz

---

**Fig. 7.4** The reset circuit

![Reset Circuit Diagram]

- Reset Switch
- RS flip-flop
- $+5V$
- $10k\Omega$
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![Functional Diagram of Analog-to-Digital Converter AD7870](image)

**Figure 7.5 Analog-to-Digital converter AD7870**

**a) Functional diagram**

**b) Timing diagram**

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Fig. 7.6 Circuit diagram of Address Decode
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(a) Architecture of high precision PWM mode

(b) PWM waveform on CMP pin showing the high precision resolution

Fig. 7.7 Operation of the DSP PWM generator
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Fig. 7.8 Null-Modem link with MAX232 between the PC and DSP

Fig. 7.9 The architecture of the serial port in asynchronous mode
Fig. 7.10 Circuit diagram for position feedback and position error

Fig. 7.11 Circuit diagram for current feedback and signal conditioning

Fig. 7.12 Circuit diagram for control signal conditioning
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(a) Diagram showing the $\delta^{-1}$-operator in terms of shift $z^{-1}$-operator

(b) Illustration of the operation flow

Operation flow for the $\delta$-operator:

1. Fetch a data from RAM, in which a previous sum $U_o$ is stored;
2. Add ACC and $U_i$, which is available in the latest sample;
3. Store the result $U_o$ in RAM for the next sample period.

Fig. 7.13 Principle of the $\delta^{-1}$-operator
(a) The first-order controller

(b) The second-order controller

Fig. 7.14 Diagram of Canonic form $\delta$-controller
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Fig. 7.15 The modified canonic $\delta$-controller

(a) The first-order controller

(b) The second-order controller
Fig. 7.16 Development of schedule table
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(a) position response

\[ \theta(t) \text{ (deg)} \]

\[ \theta = 0 \]

\[ t = t_0 \]

\[ \text{20 ms} \]

Application of gain-scheduled controller

(b) nonlinear stiffness

\[ \frac{d}{dt} k(\theta) \text{ (Nm/deg)} \]

\[ \text{maximum gain} \]

\[ t = t_0 \]

\[ \text{20 ms} \]

Curve A

Curve B

\( k(0) \)

\( k(0) \)

\( k(0) \)

\( k(0) \)

\[ \text{minimum gain} \]

\[ \text{maximum error} \]

(c) position error

\[ \text{Err}_p \text{ (deg)} \]

\[ t = t_0 \]

\[ \text{20 ms} \]

\[ \text{minimum error} \]

\[ \text{maximum error} \]

Fig. 7.17 Synchronous control of schedule table and position response
Fig. 7.18 Overall software structure
Fig. 7.19 Program structure diagram of Interrupt Service Routines (IRS)
Fig. 7.20 Flow chart of A/D conversion
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Start

Position linear compensation

Test "SCHEDULE" = 1 ?

Yes

No

Position = 0 ?

Yes

No

the slope of position > 0 ?

Yes

Set flag bit "SCHEDULE" = 1

Gain-scheduled Controller

End

Fig. 7.21 Flow chart for position synchronous logic and position loop algorithms
Fig. 7.22 Flow chart for gain-scheduled controller
output of gain-scheduled controller is in \( U_1 \); \( v_N, w_N, x_N \) are intermediate variables; \( p_N, q_N, d_N1, \)
\( d_N2, r \) are constant coefficients initialized in INITIALIZATION

\[
v_N = U_1 - w_N - x_N
\]

\[
y_e = p_N v_N + q_N x_N + r w_N
\]

\( \delta \) operation

\[
x_N = x_N - d_{N2} w_N
\]
\[
w_N = w_N - d_{N1} w_N
\]

End

Fig. 7.23 Flow chart for notch compensator
output of notch compensator is in $U_i$; $v_{L1}$, $w_{L1}$ are intermediate variables; $P_{L1}$, $Q_{L1}$, $\delta_{L1}$ are constant coefficients initialized in \textsc{initialization}

compute intermediate variable
$v_{L1} = U_i - w_{L1}$

compute output
$y_o = P_{L1}v_{L1} + Q_{L1}w_{L1}$

$\delta$ operation
$w_{L1} = w_{L1} - d_{L1}w_{L1}$

End

\textbf{Fig. 7.24} Flow chart for lead 1 compensator

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output of lead 1 compensator is in $U_1$; $v_{i_2}$, $w_{i_2}$ are intermediate variables; $p_{i_2}$, $q_{i_2}$, $d_{i_2}$ are constant coefficients initialized in INITIALIZATION

compute intermediate variable
$v_{i_2} = U_1 - w_{i_2}$

compute output
$y_o = p_{i_2}v_{i_2} + q_{i_2}w_{i_2}$

$\delta$ operation
$w_{i_2} = w_{i_2} - d_{i_2}w_{i_2}$

End

Fig. 7.25 Flow chart for lead 2 compensator
The output of lead 2 compensator is in $U_i$; $v_G$, $w_G$ are intermediate variables; $p_G$, $q_G$ and $d_G$ are constant coefficients initialized in INITIALIZATION

compute intermediate variable
$v_G = U_i - w_G$

compute output
$y_o = p_G v_G + q_G w_G$

δ operation
$w_G = w_G - d_G w_G$

End

Fig. 7.26 Flow chart for lag compensator
current error is in \( U \); \( v_l \), \( w_l \) are intermediate variables; \( p_l \), \( q_l \)
and \( d_l \) are constant coefficients initialized in \textit{INITIALIZATION}

\[ v_l = U - w_l \]

compute output
\[ y_o = p_l v_l + q_l w_l \]

\( \delta \) operation
\[ w_l = w_l - d_l w_l \]

End

\textbf{Fig. 7.27} Flow chart for current lead compensator
Fig. 7.28 Flow chart for D/A converter
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Internal variable

\[ V_1 \]

16 bits

\[ V_2 \]

16 bits

Coefficient

\[ C \]

15 bits

Fig. 7.29 Number format used in the program

\[ \begin{align*}
\text{Product} &= (V_1 \text{ MPY } C) \times 10^{32} \\
&+ (V_2 \text{ MPY } C) \times 10^{16}
\end{align*} \]

Fig. 7.30 Flow chart for two-word x one-word multiplication
Fig. 7.31 Flow chart for two-word addition and subtraction
Chapter 8

Experimental Studies

This chapter describes experimental studies carried out on the motor drive system developed in the previous chapters.

8.1 EXPERIMENTAL SYSTEM DESCRIPTION

In addition to the motor and built-in position transducer modules, the experimental drive system shown in Fig. 8.1 consists of a DSP-based digital controller, a feedback signal measuring and conditioning circuit board and a power amplifier. A 50 Hz sawtooth reference waveform generated from a programmable generator is applied to the drive system via the signal conditioning circuits, where the position, position error and current feedback signal are obtained, conditioned and fed to the A/D converters. The control program written in the DSP assembly language is downloaded via the PC parallel port to the in-circuit emulator (ICE), which has a built-in 'probe' head inserted into the DSP socket of the target system. Any change in the object code can be modified from the PC, where the DSP development system provides various window-based debugging facilities, such as the editor, data memory (RAM), assembled/disassembled program memory, register display and trace system. The ICE supports the code tests either at full speed (25 MHz), single-step, or with breakpoints.

8.2 EXPERIMENTAL PROCEDURE

The digital controller comprises a number of compensators in the two-loop system, and it is therefore difficult to tune. The experimental procedure followed was:

(1) test the power amplifier
(2) test the current loop system;
(3) test the position loop, with the notch and 1st-stage compensator added;
(4) test the position loop, with the 2nd-stage lead compensator added:
(5) test the position loop, with the lag compensator added;
(6) test the position loop, with the gain-scheduled controller.

The above process was clearly iterative, having to be repeated until satisfactory results were obtained. It was important that the various compensators were tuned individually, but in a coordinated manner that achieved a gradually improved overall performance.

8.3 PRACTICAL ISSUES OF THE DIGITAL CONTROLLER

Since the controller was designed in the continuous domain, the digitized effects brought about by the emulation described in chapter 7 should not be underestimated. The main practical issues of the digital controller are discussed below.

8.3.1 The Lagging Effect of the Analog-to-Digital Converter (ZOH)

The analysis of the previous chapters established that to obtain the desired performance necessitated the use of a sample rate of 10 kHz, which is 10 times the control system bandwidth of 1 kHz. However, a lagging phase shift is inevitably introduced by a sampled data system, and the overall effect of this can be conveniently examined by the sampling interval required, which is limited by the analog-to-digital conversion time, the algorithm computational time and the digital-to-analog conversion time. The analog signal is sampled and transformed to digital form by an analog-to-digital converter, then processed by the DSP, and finally converted back to analog form via the digital-to-analog converter. The data held in the digital-to-analog converter is updated at the sample rate, producing a 'staircase' waveform. The data reconstruction of the digital-to-analog conversion is represented by a zero-order-hold device (ZOH), which can be approximated by the first-order lag system

\[ G_{zoh}(s) = \frac{2/T}{s + 2/T} \]  

(8.1)
where $T$ is the sample time. With $T = 100 \mu s$, Eqn. (8.1) becomes

$$G_{zoh}(s) = \frac{20000}{s + 20000}$$ \hspace{1cm} (8.2)

It is evident from these equations that the sampling process introduces a low-pass filter characteristic, with the magnitude being reduced and the phase shift being considerably increased at high frequencies, causing a deterioration in the system performance. To compensate for this, an additional lead compensator is used in series with the existing lead compensator (defined by Eqn. 7.10(e)) in the current loop, such that the maximum leading phase offsets the lagging phase caused by ZOH, which was calculated from Eqn. 8.2 as exceeding $17^\circ$, at frequencies above $1$ kHz. The compensator was designed as

$$G_{czoh}(s) = 3 \left( \frac{s + 10000}{s + 30000} \right)$$ \hspace{1cm} (8.3)

providing a phase lead of $20^\circ$, giving a net increase of $3^\circ$ in the phase lead at a frequency of $1$ kHz. This is converted to digital form using Emulation Table 7.3, and then tuned directly in the experimental system.

### 8.3.2 Limited Wordlength representations for the Digital Controller

Generally, when converted to digital form, the wordlength of the digital controller should be sufficiently long to represent accurately its continuous equivalent. However, the longer the wordlength that is necessary, the more time is required to compute the related algorithms. In practice, this is in conflict with the limited sample time, which is determined by the overall system performance (eg the closed-loop bandwidth). The initial consideration of using a 32-bit wordlength (ie two 16-bit words) for all the internal variables will result in a significant increase in the computing time and therefore the sample time. Table 8.1 shows the estimated time for computing the compensations.
It is seen from the table that, if a fixed time of 15 µs is needed for the analog-to-
digital conversions and other I/O operations, even with a 16-bit wordlength for both
the internal variables and coefficients, the total computing time exceeds the required
sample time of 100 µs. It was decided therefore to implement the position feedback
lead compensator (the 1st position lead) using analog amplifiers. This provided extra
time for the digitized compensators, with a 32-bit wordlength representation for some
internal variables, which had significant influence over the computing accuracy.

Table 8.1 Computing time for compensators

<table>
<thead>
<tr>
<th>Compensation type</th>
<th>Computing time required</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>16-bit coefficient</td>
</tr>
<tr>
<td></td>
<td>16-bit variable</td>
</tr>
<tr>
<td>(1) 1st current lead $G_1(\delta)$</td>
<td>12 µs</td>
</tr>
<tr>
<td>(2) 2nd current lead $G_{czo}(\delta)$</td>
<td>12 µs</td>
</tr>
<tr>
<td>(3) Position notch $G_N(\delta)$</td>
<td>18 µs</td>
</tr>
<tr>
<td>(4) 1st position lead $G_{L1}(\delta)$</td>
<td>10 µs</td>
</tr>
<tr>
<td>(5) 2nd position lead $G_{L2}(\delta)$</td>
<td>10 µs</td>
</tr>
<tr>
<td>(6) Position lag $G_{G}(\delta)$</td>
<td>10 µs</td>
</tr>
<tr>
<td>(7) Gain-scheduled $G_s(\delta)$</td>
<td>16 µs</td>
</tr>
<tr>
<td><strong>Subtotal</strong></td>
<td><strong>88 µs</strong></td>
</tr>
<tr>
<td><strong>A/D conversion, I/O, etc.</strong></td>
<td><strong>15 µs</strong></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>103 µs</strong></td>
</tr>
</tbody>
</table>

8.4 RESULTS

Various results obtained from the experimental prototype system are shown in Figs.
8.2 - 8.8.
Figs. 8.2 and 8.3 show respectively the time response of the linear power amplifier with a square wave input, at both no-load and on-load. The output voltage responds extremely rapidly to changes in the input, and reaches almost instantly the steady-state of either $-35\,\text{V}$ to $+35\,\text{V}$. With the load current of 0.5 A applied to a resistor load, the output voltage on-load exhibits the same response performance as on no-load.

Fig. 8.4 shows the open-loop time response of the drive system when a sawtooth waveform is applied. Comparison between these waveforms and the simulated waveforms of Fig. 8.5 shows the effectiveness of the system model described in chapter 3.

Fig. 8.6 shows the closed-loop time response of the drive system employing the linear controller, but without the second current lead compensator required to compensate for the ZOH. It is seen that the response waveforms are similar to the simulated waveforms shown previously in Fig. 4.21, with the position response being able to track the reference. However, the existence of the oscillations indicates that the phase margin is insufficient for the digitized control system [30,37].

Fig. 8.7 shows the closed-loop time response of the drive system employing the linear controller, together with the additional current compensator used to compensate for the ZOH. A clear improvement in the system stability is seen by the absence of the previous oscillations, and the reference now being more accurately tracked.

Fig. 8.8 shows the close-loop time response of the drive system employing both linear and gain-scheduled controller. The overall tracking performance in terms of the position error and stability is considerably improved, and the careful examination of the position response gives a linearity of $\pm0.05^\circ$ for the active linear scanning period of 16 ms.
Fig. 8.1 A complete experimental drive system
(a) Input frequency = 1 kHz

(b) Input frequency = 2 kHz

Fig. 8.2 Response of the amplifier output voltage at the no-load condition
Fig. 8.3 Response of the amplifier output voltage and current at the on-load condition

(a) Input frequency = 1 kHz

(a) Input frequency = 1 kHz
Fig. 8.3 Response of the amplifier output voltage and current at the on-load condition (continued)

(b) Input frequency = 2 kHz
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Figure 8.4 Open-loop response of the experimental drive system
Fig. 8.5 Open-loop response of the simulated drive system
Fig. 8.6 Closed-loop response of experimental drive system employing linear controller without the ZOH compensation
Fig. 8.6 Closed-loop response of experimental drive system employing linear controller without the ZOH compensation (continued)
Fig. 8.7 Closed-loop response of experimental drive system employing linear controller with the ZOH compensation
Fig. 8.7 Closed-loop response of experimental drive system employing linear controller with the ZOH compensation (continued)
Fig. 8.8 Closed-loop response of experimental drive system employing both linear controller and gain-scheduled controller.
Fig. 8.8 Closed-loop response of experimental drive system employing both linear controller and gain-scheduled controller (continued)
Chapter 9

Conclusions and Further Work

This chapter presents conclusions on the research described in this thesis and makes remarks and suggestions for further work.

9.1 CONCLUSIONS

A high performance DSP-based drive system was successfully developed to control a limited-angle torque motor, so that it followed precisely a 50 Hz reference sawtooth waveform. The drive system uses a multi-compensator, multi-loop linear controller, combined with a nonlinear gain-scheduled controller to both implement tight control on the motor and ensure system stability.

The digital controller provides great flexibility in implementing adaptive control, facilitates efficient tuning of the algorithms, and permits easy changes in the control software to suit different specifications. The TI TMS320E14 DSP was used as the core of the controller, due to its high speed, optimum architecture and the various on-chip control peripherals, and 12-bit high speed analog-to-digital and digital-to-analog converters were used to minimize the sampling and quantisation errors. The performance of the digital control system showed substantial improvement when the \( \delta \)-operator (rather than the conventional \( z \)-operator) and the filter structure in modified canonical form (rather than in the direct form), were used to convert the continuous controller to a discrete form with a high sample rate. Minimization of the algorithm errors required the wordlength used to be sufficiently long to represent the filter internal variables and coefficients.

The power amplifier was vitally important to the drive system performance, and a linear operational amplifier provided a superior overall performance to a switch-mode amplifier, both in terms of bandwidth and speed of response. For the same rated current (eg 0.5 A), the settling time of the linear amplifier of 0.01 ms following a large step change in output voltage between \(-35\) and \(+35\) V (Fig. 8.3, chapter 8)
was much better than the 0.6 ms \([68,85]\) obtained from a switch-mode amplifier for the similarly large step change in the output voltage. The bandwidth of the linear amplifier is clearly demonstrated by the drive voltage waveforms (Figs. 8.4 to 8.8, Chapter 8), which showed the capability to reproduce faithfully the control signals computed from the DSP containing the high frequency signals in the flyback period. This was also in contrast to the switch-mode amplifier, which in the same application was incapable of responding sufficiently quickly to control signals \([85]\).

Practical results obtained were in excellent agreement with simulated results, demonstrating the effectiveness of both the proposed control scheme and the experimental drive system. A linearity of \(\pm 0.05^\circ\) was achieved throughout the 16 ms forward scanning of the motor position, with the drive voltage being limited to the required \(\pm 35\) V. The discrepancies between the simulated and practical results may be accounted for by the limitations in the experimental system.

### 9.1.1 Design Method Review

To drive a rotary electromagnetic actuator to follow precisely a periodic waveform input presents a significant technical challenge. The lack of published literature in this field has stimulated an in-depth exploration of the appropriate design method, which must be effective, reliable and applicable to engineering applications requiring satisfactory practical results. The method developed during the course of this research can be summarized as

1. Detailed modelling and dynamic analysis are both needed to provide insight and understanding of the controlled actuators. The development of an experimentally-based motor model is desirable, as this establishes a good basis for the design of a reliable control system.

2. A multi-loop structure, which contains current, position and/or speed loops is essential for the control system. The inclusion of, for example, notch, lead and lag compensations are needed to reshape substantially the original actuator
characteristics to obtain the required response performance. The use of
dynamic feedforward and feedback control, in both the inner and outer loops,
then enables the demanding transient and steady-state responses to be met
simultaneously and with little compromise.

(3) The design of a nonlinear controller depends on the characteristics of the
controlled actuators, and it must ensure overall system stability when it is
introduced. A first-order gain-scheduled controller was used to control the
nonlinearities that exist in the torque motor, and which were identified in the
experimental modelling studies. Various other advanced adaptive control
methods (e.g., model reference adaptive control, self-tuning control, etc.) are
possible, but in practice they would require considerably longer computing
time.

(4) The use of Bode plots provide a very effective approach to controller design
in the frequency domain, and by manipulating the magnitude and phase
response plots with respect to the same frequency variables, a complex multi-
compensator multi-loop high-order system can be synthesized. Inherently well
defined relationships exist between the frequency and the time response
performances and, no matter whether or not they can be expressed
analytically, the time response performance can be dependably predicted from
the frequency response. In designing the control system for the torque motor,
the following observations were made.

- The speed of the time response depends mainly on the open-loop gain-
crossover frequency $\omega_c$. In order to track a periodic waveform, comprising
many harmonics of the fundamental frequency, $\omega_c$ is inevitably high, which
normally results in a correspondingly high closed-loop bandwidth.

- The position tracking error is determined by the open-loop gain over a wide
frequency range (not just a single frequency), for which the term "low-
medium frequency range" was used in defining the loop gain frequency
characteristics. The smaller the error, the higher is the loop gain needed.

- Relative stability is most appropriately indicated by the phase margin and the gain margin, as well as by the slope and frequency bandwidth of the frequency response characteristics near the gain-crossover point (0 dB). It is essential that the phase margin is in excess of 45°, the gain margin is at least 10 dB, the gain crossover slope is around 20 dB/dec., and the bandwidth is as wide as possible. When the system does not satisfy these conditions, the time response will show high frequency oscillations superimposed on the normal waveforms. For example, in the position response oscillations appear at the beginning of the linear scanning period (see Fig. 8.4, Chapter 8), while in the drive voltage and current waveforms, excessively large pulses (> ±35 V) occur in the flyback period.

- The filtering capability (i.e., rejection of the high frequency noise) is best indicated by the slopes of the open-loop and closed-loop gain characteristics in the high frequency range, which should ideally be at least −60 dB/dec. However, the closed-loop bandwidth \( \omega_{bw} \) should not be excessively large, or else high frequency noise will appear in the drive voltage and current (see position loop design of Chapter 4).

(5) The controller is designed in the frequency domain, checked with respect to the various frequency performance criteria outlined in Chapter 4, and finally verified by time domain simulations. This is an iterative process, and the transfer function of the resultant controller will normally have an order much higher than that of the controlled actuators.

9.2 REMARKS ON EXPERIMENTAL DRIVE SYSTEM

While the practical results were in excellent agreement with the theoretically predicted results, the required linearity of the position response has not yet been achieved. This can be accounted for by the limitations of the experimental drive system, considered
(1) Non-ideal power amplifier

Although the linear power amplifier has an overall performance superior to that of the switch-mode alternative, it still exhibits a limitation in terms of the full power response. Fig. 9.1 shows practical measurements of the input-to-output voltage transfer characteristic, when a series of large sinusoidal signals are applied to the amplifier. It is seen that a reduction in the voltage gain and a lagging phase shift both become evident above 1 kHz. This indicates that the amplifier is not the ideal constant gain, zero phase shift device assumed in the simulations.

(2) Limitations of the DSP

The TMS320E14 DSP is capable of operating at a clock frequency of 25 MHz and, with the hardware multiplier, a 16-bit x 16-bit multiplication can be completed within a single instruction cycle of 160 ns. However, it has been shown in Chapter 8 that the DSP still does not meet the very stringent timing requirement of the present application, with some of the compensations having to be implemented by analog amplifiers, and most of the internal variables and coefficients having to be represented by 16-bit words. Although a compromise might be made by using a slower sample rate (ie, a longer sample time) to accommodate the extra computing load, with the aim of improving the computation accuracy by using a longer wordlength, this is in conflict with the requirement of a fast sample rate from the considerations of the overall system performance. Furthermore, it is very difficult to guarantee the performance when the sample time is increased to 150 μs, as indicated in table 8.1.

(3) Insufficient Resolution of the A/D and D/A Converters

Another source of error arises in analog-to-digital and digital-to-analog devices, due to their limited resolution. Nonlinearities are introduced when an analog signal is converted to a 12-bit digital signal, due to the need to
truncate the 4 least significant bits for the DSP processing in 16-bit format.

(4) Limitations of the General-Purpose Operational Amplifiers
The feedback signal conditioning circuit uses a considerable number of operational amplifiers TL071 and TL072, and the performance of these is rather limited for the present application. For example, the unity-gain bandwidth (discussed in Chapter 5) is only 3 MHz.

A further limitation of the present research was that the controller design was carried out in the s-domain. This was necessary, since one of the primary objectives of the research was to seek an effective control strategy unavailable in the published work, and designing for continuous control allows the use of various well developed frequency response techniques. However, it has certain shortcomings when the controller has to be converted to digital form by an approximate method, one of which is that the sample rate has to be sufficiently high to minimize the conversion error. The use of a high sample rate imposes a heavy burden on the microprocessors.

9.3 SUGGESTIONS FOR FURTHER WORK

Based on the above analysis, investigations were made on further work that could be carried out, as detailed below.

(1) Use of the new generation of DSPs to replace the TMS320E14. One option is to choose the TMS320C240 [86,87], which is the updated version of TMS320E14. The main advantage that would arise is the considerably improved speed, with only a 50 ns instruction cycle (compared to the 160 ns of the TMS320E14). Furthermore, the control software developed for the TMS320E14 can be used, as software compatibility is maintained throughout the TI TMS320 DSP family.

(2) Replacing the existing power amplifier SGS L465 with either BB OPA541 or OPA241 [88,89], will considerably improve the overall drive performance.
due to the much greater power bandwidth (55 kHz at the output voltage of 20 V rms), higher voltage rating (±40 V), larger open-loop gain (90 dB at 10 Hz), larger gain-bandwidth (1.6 MHz), and much lower input bias current (50 pA).

(3) Replacement of the present 12-bit A/D AD7870 with a higher resolution device, such as the 14-bit converter AD7871, or the BB 16-bit ADS7805P. The D/A converter AD767 may be updated to a 16-bit device, such as the AD766.

(4) Operational amplifiers TL071/TL072 can be substituted directly by the MOT LF411CN/LF412CN, which has a greater unity-gain bandwidth, and lower a input bias current.

The cost of the drive system will have to increase to meet the upgrading of the components, and this is necessary if the extremely demanding specifications have to be met. It is suggested that the final drive system electronics should be implemented using the special customer design method, to obtain maximum performance/cost effectiveness.

To find an optimum sample rate, the controller may be re-designed in the z-domain, or the w-plane [77,80], which will allow the sampling effects to be taken into account in the controller design stage. Either of these is inefficient in comparison with the frequency method used in this research. With a high-order multi-loop control system, the z-domain design is inherently limited to a unity cycle and requires more computational efforts, while the w-plane design involves the introduction of extra positive zeros that should be dealt with carefully, due to the potential stability problem caused. Nevertheless, design data given by the present continuous controller should provide a good basis for either method, by which a low sample rate beneficial for the overall digital control system may be obtained.
Fig. 9.1 Measured frequency characteristics of linear power amplifier with output voltage magnitude = 40V p-p and load current magnitude = 1 A p-p
REFERENCES


[79] *Digital Control Application with the TMS320 family -- selected application notes*, Texas Instruments, 1990


[88] *High power monolithic operational amplifier OP541*, Burr-Brown Data Sheet.

[89] *Dual power operational amplifier OPA2541*, Burr-Brown Data Sheet.
# Appendix A

## Specifications of FMS-S526 Frame Scan Motor System

### 1. Motor/Transducer Unit L-503

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak torque</td>
<td>$T_m$</td>
<td>0.16 Nm</td>
</tr>
<tr>
<td>Torque constant</td>
<td>$K_t$</td>
<td>0.125 Nm/A</td>
</tr>
<tr>
<td>Back e.m.f constant</td>
<td>$K_b$</td>
<td>0.125 V/rad·s$^{-1}$</td>
</tr>
<tr>
<td>Magnetic stiffness constant</td>
<td>$K_s$</td>
<td>0.25 Nm/rad</td>
</tr>
<tr>
<td>Frictional constant</td>
<td>$K_f$</td>
<td>$10^{-4}$ Nm/rad·s$^{-1}$</td>
</tr>
<tr>
<td>Resistance</td>
<td>$R$</td>
<td>16 Ω</td>
</tr>
<tr>
<td>Inductance</td>
<td>$L$</td>
<td>0.045 H</td>
</tr>
<tr>
<td>Rotor inertia</td>
<td>$J$</td>
<td>$3 \times 10^{-7}$ kg·m$^2$</td>
</tr>
<tr>
<td>Operational temperature range</td>
<td>$T$</td>
<td>$-46^°C/ +100^°C$</td>
</tr>
<tr>
<td>Angular displacement</td>
<td>$\theta$</td>
<td>$\pm 10^°$</td>
</tr>
<tr>
<td>Scan efficiency*</td>
<td>$\eta$</td>
<td>80%</td>
</tr>
</tbody>
</table>

* When driven by 50 Hz

### 2. Signal Conditioner Module D527

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>$\theta_s$</td>
<td>50 mV/°</td>
</tr>
<tr>
<td>Zero drift*</td>
<td>$\theta_z$</td>
<td>0.15°</td>
</tr>
<tr>
<td>Gain drift*</td>
<td>$G_0$</td>
<td>±1% total</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>$BW$</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Linearity*</td>
<td>$\Delta \theta$</td>
<td>±0.2% over ±10°</td>
</tr>
<tr>
<td>Carrier ripple</td>
<td>$G_r$</td>
<td>20 mV rms</td>
</tr>
</tbody>
</table>

* Applicable over full specified operating temperature range
Appendix A Specifications of FMS-S526 Frame Scan Motor System

3. Electrical Connection of Frame Scan System S526

Connector type: 838-17-MY1-022N Dean Technitron

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+12 V</td>
</tr>
<tr>
<td>2</td>
<td>-12 V</td>
</tr>
<tr>
<td>3</td>
<td>0 V</td>
</tr>
<tr>
<td>4</td>
<td>Motor lead screen</td>
</tr>
<tr>
<td>5</td>
<td>Motor lead A</td>
</tr>
<tr>
<td>6</td>
<td>Connected to 4</td>
</tr>
<tr>
<td>7</td>
<td>Motor lead B</td>
</tr>
<tr>
<td>8</td>
<td>0 V</td>
</tr>
<tr>
<td>9</td>
<td>0 V</td>
</tr>
<tr>
<td>10</td>
<td>0 V</td>
</tr>
<tr>
<td>11</td>
<td>0 V</td>
</tr>
<tr>
<td>12</td>
<td>0 V</td>
</tr>
<tr>
<td>13</td>
<td>0 V</td>
</tr>
<tr>
<td>14</td>
<td>0 V</td>
</tr>
<tr>
<td>15</td>
<td>0 V</td>
</tr>
<tr>
<td>16</td>
<td>Transducer output*</td>
</tr>
<tr>
<td>17</td>
<td>0 V</td>
</tr>
</tbody>
</table>

* Polarity of the transducer: - with + Vo voltage connected to Pin 5 wrt Pin 7, the motor shaft shall rotate clockwise when viewed from the front, and the transducer output shall be negative.
Appendix B

Continuous Controller Design Data

The continuous controller comprises a number of compensators as given below.

1. Current Lead Compensator

\[ G_I(s) = 6000 \left( \frac{s + 345}{s + 3450} \right) \]  \hspace{1cm} (B1)

2. Position Notch Compensator

\[ G_N(s) = \frac{s^2 + 1333s + 980400}{s^2 + 2404s + 980400} \]  \hspace{1cm} (B2)

3. First Position Lead Compensator

\[ G_{L1} = 2.3 \left( \frac{s + 18725}{s + 27785} \right) \]  \hspace{1cm} (B3)

4. Second Position Lead Compensator

\[ G_{L2} = 13.3 \left( \frac{s + 81409}{s + 113320} \right) \]  \hspace{1cm} (B4)
5. Position Lag Compensator

\[ G_G = 5 \left( \frac{s + 119}{s + 0.453} \right) \]  \hspace{1cm} \text{(B5)}

6. Gain-Scheduled Controller

\[ G_s = \frac{s + 426k(\theta)}{s + 426} \]  \hspace{1cm} \text{(B6)}

where

\[ k(\theta) = 10 \frac{d}{d\theta} (T_s(\theta)) \]  \hspace{1cm} \text{(B7)}

\[ T_s(\theta) = \left( \frac{0.034 + 7.4\theta^2}{1 - 5.7\theta^2} \right) \theta \]  \hspace{1cm} \text{(B8)}
Appendix C

Operational Power Amplifier SGS L465

1. Connection Diagram (top view)

![Connection Diagram]

2. Main Features

- Output current to 4 A
- Supply voltage to $\pm 20$ V
- Large common-mode range
- Large differential mode range
- Large bandwidth
- Low saturation
- SOA protection
- Short circuit protection
- Thermal protection

3. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_s$</td>
<td>Supply voltage</td>
<td>$\pm 20$ V</td>
</tr>
<tr>
<td>$V_{icm}$</td>
<td>Input voltage</td>
<td>$V_s$</td>
</tr>
<tr>
<td>$V_{diff}$</td>
<td>Differential input voltage</td>
<td>$\pm 15$ V</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Peak output current (internal limited)</td>
<td>4 A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>Power dissipation at $T_{case} = 90^\circ C$</td>
<td>20 W</td>
</tr>
<tr>
<td>$T_{stg}, T_j$</td>
<td>Storage and junction temperature</td>
<td>-40 to 150 °C</td>
</tr>
</tbody>
</table>
4. Electrical Characteristics

\( (V_s = \pm 15V, T_{amb} = 25^\circ C \) unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>( V_s ) power voltage</td>
<td></td>
<td>± 3</td>
<td>± 20</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_q ) Quiescent drain current</td>
<td></td>
<td></td>
<td>45</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_b ) Input bias current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{os} ) Input offset voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{os} ) Input offset current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR slew rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_o ) Output voltage swing</td>
<td>( f = 1 ) kHz</td>
<td>26</td>
<td>27</td>
<td>( V_{pp} )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_p = 0.5 ) A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_p = 4 ) A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f = 10 ) kHz</td>
<td>27</td>
<td>24</td>
<td></td>
<td>( V_{pp} )</td>
</tr>
<tr>
<td></td>
<td>( I_p = 0.5 ) A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_p = 4 ) A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW Power bandwidth</td>
<td>( V_o = 1V )</td>
<td>100</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>( R_L = 4 ) ( \Omega )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_I ) Input resistance (pin 1)</td>
<td>( f = 1 ) kHz</td>
<td>100</td>
<td>500</td>
<td></td>
<td>k( \Omega )</td>
</tr>
<tr>
<td>( G_v ) Voltage gain (open loop)</td>
<td>( f = 1 ) kHz</td>
<td></td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( e_n ) Input noise voltage</td>
<td>( B = 10 ) to ( 10 ) kHz</td>
<td>2</td>
<td>6</td>
<td>( \mu )V</td>
<td></td>
</tr>
<tr>
<td>( i_n ) Input noise current</td>
<td>( B = 10 ) to ( 10 ) kHz</td>
<td>100</td>
<td></td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>CMRR Common mode rejection</td>
<td>( R_g \leq 10 ) k( \Omega )</td>
<td>70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>( G_v = 30 ) dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SVR supply voltage rejection</td>
<td>( R_g = 22 ) k( \Omega )</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>( G_v = 10 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{ripple} = 0.5 ) Vrms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f_{ripple} = 100 ) Hz</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>( G_v = 100 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \eta ) Efficiency</td>
<td>( f = 1 ) KHz</td>
<td>66</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>( I_p = 3 ) A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tsdl Thermal shutdown junction temperature</td>
<td></td>
<td>145</td>
<td></td>
<td></td>
<td>°C</td>
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</table>

240
Appendix D

The List of the DSP Assembly Source Code

File title 'system6'

* This code implements a two-loop multi-compensator drive control for a limited-angle torque motor
* A lead compensator is used in the current loop. A linear controller, comprising a notch, a lead, a lag, is used
* in series with a first-order adaptive gain-scheduled controller controller in the position forward path, while a
* second lead compensator is realized using analog amplifiers.
* An additional lead compensator is used in the current loop to compensate for the ZOH.
* The bilinear transform with the δ-operator is used to convert continuous transfer functions to digital ones, with
* the sample time chosen to be 100 µs.
* Define the DSP banks and ports

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
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<tbody>
<tr>
<td>BSR</td>
<td>EQU</td>
<td>7</td>
</tr>
<tr>
<td>IOP</td>
<td>EQU</td>
<td>0</td>
</tr>
<tr>
<td>IOP</td>
<td>EQU</td>
<td>0</td>
</tr>
<tr>
<td>DDR</td>
<td>EQU</td>
<td>1</td>
</tr>
<tr>
<td>BBSET</td>
<td>EQU</td>
<td>2</td>
</tr>
<tr>
<td>BCLEAR</td>
<td>EQU</td>
<td>3</td>
</tr>
<tr>
<td>IFLAG</td>
<td>EQU</td>
<td>4</td>
</tr>
<tr>
<td>IM</td>
<td>EQU</td>
<td>5</td>
</tr>
<tr>
<td>FCLEAR</td>
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<tr>
<td>WDBANK</td>
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<td>1</td>
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<td>WPER</td>
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</table>
Appendix D

The List of DSP Assembly Source Code

* Define the addresses for A/D and D/A converter

* BKFFFF EQU 255
  SADC1 EQU 0
  RADC1 EQU 1
  SADC2 EQU 2
  RADC2 EQU 3
  DAC1 EQU 3

* Define the internal variables used in the control algorithms
  
* 1. Controller coefficients

* 1.1 the first current lead compensator
  PL EQU >0
  QL EQU >1
  DL EQU >2

* 1.2 the second current lead compensator
  PL2 EQU >3
  QL2 EQU >4
  DL2 EQU >5

* 1.3 the position notch compensator
  P EQU >6
  Q EQU >7
  D1 EQU >8
  D2 EQU >9

* 1.4 the position lead compensator
  PPL EQU >A
  PQL EQU >B
  PDL EQU >C

* 1.5 the position lag compensator
  PG EQU >D
  QG EQU >E
  DG EQU >F

* 1.6 the gain-scheduled controller
  PS EQU >10
  QS EQU >11
  DS EQU >12

* 2. Controller internal variables

* 2.1 the first current lead compensator
  ACTUL1 EQU >13
  REH10 EQU >14
  REHI1 EQU >15
  MI2W0 EQU >16
  MI2W1 EQU >17
  ERRH0 EQU >18
  ERRH1 EQU >19
  VL0 EQU >1A
  VL1 EQU >1B
  WL0 EQU >1C
  WL1 EQU >1D

* 2.2 the second current lead compensator
  VL20 EQU >1E
  VL21 EQU >1F
  WL20 EQU >20
  WL21 EQU >21

* 2.3 the position notch compensator
  V0 EQU >22
  V1 EQU >23
  W1 EQU >24
  W2 EQU >25
  X0 EQU >26
  X1 EQU >27

* 2.4 the position lead compensator
  PVLO EQU >28
Appendix D

The List of DSP Assembly Source Code

PVL1 EQU > 29
PWLO EQU > 2A
PW1 L EQU > 2B

* 2.5 the position lag compensator
VG0 EQU > 2C
VG1 EQU > 2D
WG0 EQU > 2E
WG1 EQU > 2F

* 2.6 the gain-schuled controller
VS0 EQU > 30
VS1 EQU > 31
WS0 EQU > 32
WS1 EQU > 33

* 2.7 the position input variables
ACTLP0 EQU > 34
ERRP0 EQU > 35
ERRP1 EQU > 36
POSIP0 EQU > 37
POSIP1 EQU > 38

* 2.8 the other variables
HWORD EQU > 39
MWORD EQU > 3A
U00 EQU > 3B
U01 EQU > 3C
U10 EQU > 3D
U11 EQU > 3E
VLO EQU > 3F
VL1 EQU > 40
V0 EQU > 41
V1 EQU > 42
X0 EQU > 43
X1 EQU > 44
WL0 EQU > 45
WL1 EQU > 46
W0 EQU > 47
W1 EQU > 48
FLAG EQU > 49

* 3. Intermediate and output results
RTMP00 EQU > 4A
RTMP01 EQU > 4B
RTMP10 EQU > 4C
RTMP11 EQU > 4D
TEMP EQU > 4E
TMP00 EQU > 4F
TMP01 EQU > 50
TMP10 EQU > 51
TMP11 EQU > 52
CNTRL EQU > 53
CNTRL0 EQU > 54
CNTRL1 EQU > 55
DRIVE0 EQU > 56
DRIVE1 EQU > 57

* 4. Constants
* 4.1 position loop gain constant
KP EQU > 58
KPS EQU > 59
KG EQU > 5A

* 4.2 current loop gain constant
KI EQU > 5B
KIFS EQU > 5C

* 4.3 shift operation constant
SIGN EQU > 5D
H8000 EQU > 5E
H7FFF EQU > 5F
HIGH EQU > 60
Appendix D

The List of DSP Assembly Source Code

LOW EQU > 61
* 4.4 other constants
SPRIOD EQU > 62
ZERO EQU > 63
ONE EQU > 64
TWO EQU > 65
BANK EQU > 66
TCONF EQU > 67
LOWACC EQU > 68
HIHACC EQU > 69
BKSAVE EQU > 6A
IMASK EQU > 6B
IFIMAG EQU > 6C
CLINT1 EQU > 6D
INTCLR EQU > 6E
H800 EQU > 6F
FFFF EQU > 70
IOP3 EQU > 71
IOP4 EQU > 72
IOP5 EQU > 73
IOP6 EQU > 74
IOP7 EQU > 75
IOP9 EQU > 76
TABLE0 EQU > 77
TABLE EQU > 78
COUNT EQU > 79
SUBINT EQU > 7A
MINTER EQU > 7B
AINTER EQU > 7C
RSOFLW EQU > 7D
INTCNT EQU > 7E
*
*
Program Memory
*
AORG > 00
*
RESET and Interrupt branch instruction
B INIT
B IRS

INIT
DINT
LDPK 0
LARK AR0, 255
SOVM
*
clear RAM data
ZAC
LARP AR0
*
SACL * LOOP
BANZ LOOP
*
initialize the constants
ZAC
SACL ZERO
SACL FLAG
SACL 1
SACL ONE
SACL 2
SACL TWO
*
set up the offset constant
LACK > 8
SACL H800
LAC H800, 8
SACL H800
*
shift operation constant
LACK > 80
SACL H8000
LACK > 00
ADD H8000, 8
### Appendix D

**The List of DSP Assembly Source Code**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Register</th>
<th>Value</th>
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<td>SACL</td>
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* Position loop gain constant

<table>
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<th>Register</th>
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* Current loop constant

* The current forward gain

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* The feedback scaling factor

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* Current lead controller coefficients

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* Notch controller

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</table>
The List of DSP Assembly Source Code

Appendix D

LACK > 8C
ADD Q, 8
SACL Q

LACK > 1C
SACL D1
LACK > FD
ADD D1, 8
SACL D1

LACK > 7
SACL D2
LACK > 18
ADD D2, 8
SACL D2

position lead controller coefficients
LACK > 7F
SACL PPL
LACK > D2
ADD PPL, 8
SACL PPL

LACK > 24
SACL PQL
LACK > FB
ADD PQL, 8
SACL PQL

LACK > 7
SACL PDL
LACK > 9C
ADD PDL, 8
SACL PDL

position lag controller coefficient
LACK > 7F
SACL KG
LACK > FF
ADD KG, 8
SACL KG

LACK > 0C
SACL PG
LACK > D4
ADD PG, 8
SACL PG

LACK > 0
SACL DG
LACK > 03
ADD DG, 8
SACL DG

the second current controller coefficients
LACK > 5B
SACL PL2
LACK > 6E
ADD PL2, 8
SACL PL2

LACK > 47
SACL QL2
LACK > 1C
ADD QL2, 8
SACL QL2
Appendix D

The List of DSP Assembly Source Code

LACK > 52
SACL DL2
LACK > 49
ADD DL2,8
SACL DL2

* the gain-schedule controller coefficients
LACK > 7F
SACL QS
LACK > FF
ADD QS, 8
SACL QS

LACK > 00
SACL DS
LACK > 5F
ADD DS, 8
SACL DS

* set up the look-up table for the reference current
LACK > 5
SACL TABLE
LAC TABLE, 8
SACL TABLE
SACL TABLE0

* (TABLE) = > 300, the starting address of the reference position
* COUNT = (300)H + (C7) = (3C7)H

* set up clear bit for timer1 interrupt int1 in interrupt flag
LAC ONE, 4
SACL CLINT1

* Initialization of the control peripherals
* I/O port initialization
LACK > FF
SACL TEMP
LAC TEMP, 8
SACL TEMP
LACK > FF
ADD TEMP
SACL TEMP
SACL FFFF

* IO PORT configured as outputs
LACK IOBANK
SACL BANK
OUT BANK, BSR
OUT TEMP, DDR

* IOP3 = 0, Channel 0, position error
* IOP3 = 1, Channel 1, position error

* IOP4 = 0, enable the A/D converter
* IOP4 = 1, disable the A/D converter

* IOP5 = 0, enable the A/D converter
* IOP5 = 1, disable the A/D converter

* IOP6 = 1, green LED on
* IOP7 = 1, red LED on

* Arithmetic constant
LACK > 5E
SACL RSOFLOW
LACK > FC
Appendix D  The List of DSP Assembly Source Code

ADD RSOFLW, 8
SACL RSOFLW

* Interrupt Mask register initialization
LACK > FF
SACL TEMP
LAC TEMP, 8
SACL TEMP
LACK > EF
ADD TEMP
SACL TEMP
LACK IBANK
SACL BANK
OUT BANK, BSR
OUT TEMP, IM

* Timer1 period register initialization
LACK > 2
SACL SPRIOD
LAC SPRIOD, 8
SACL SPRIOD
LACK > 71
ADD SPRIOD
SACL SPRIOD
LACK TBANK
SACL BANK
OUT BANK, BSR
OUT SPRIOD, TPR1

* Set up the timer control register
LACK > FF
SACL TCONF
LAC TCONF, 8
SACL TCONF
LACK > C6
ADD TCONF
SACL TCONF
LACK TBANK
SACL BANK
OUT BANK, BSR
OUT TCONF, TCON

* initialize INTCNT
LACK > A
SACL INTCNT

* Initialization of D/A converter
LACK > 08
SACL TEMP
LAC TEMP, 8
SACL TEMP

* LACK BKFFFF
SACL BANK
OUT BANK, BSR
OUT TEMP, DAC1

EINT

* Forever loop and awaiting for interrupt
LOOP1
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
B LOOP1

* set up the IM register as
* 1111 1111 1110 1111
* mask all the bits except INT1 bit

* (37D)h=(893)d
* 893*.160=142.88us
* 142.88*140=20.0032ms

* load timer1 period reg

* TCONF = FFC6

* initial REFP = (1000 0000 0000) = OV

* output initial REF to D/A converter

* enable the INTM bit
Appendix D

The List of DSP Assembly Source Code

* ** Interrupt Routine Service (IRS)
* AORG > 100

IRS
SACL LOWACC
SACH HIHACC
IN BKSAVE, BSR

* store the (ACC) and BSR

*************** Sample Position and Current ***************

* 1. Obtain the feedback samples
* 1.1 start A/D conversions for current and position error

LACK BKFFFF
SACL BANK
SACL FFFF
OUT BANK, BSR
OUT FFFF,SADC1

* start A/D converter 1 for current

LACK IOBANK
SACL BANK
OUT BANK, BSR
OUT IOP3,BCLEAR

* set the channel for position error

NOP
NOP
NOP
NOP

LACK BKFFFF
SACL BANK
SACL FFFF
OUT BANK, BSR
OUT FFFF,SADC2

* start A/D converter 2 for position error

* 1.2 Wait for A/D conversions
ZAC
SACL TEMP
AD1
LAC TEMP
ADD ONE
SACL TEMP
LAC INTCNT
SUB TEMP
BNZ AD1

* 1.3 Read the A/D converter 2 for position error sampling

LACK IOBANK
SACL BANK
OUT BANK, BSR
OUT IOP9,BCLEAR

* enable the ADC 2 chip select(CS)

LACK BKFFFF
SACL BANK
OUT BANK, BSR
IN ERRP0,RADC2

* NOTE: (CS) is independent from
* (CONVST)

LACK IOBANK
SACL BANK
OUT BANK, BSR
OUT IOP9,BITSET

* Disable the ADC2

* 1.4 Read the A/D Convert 1 for current sampling

LACK IOBANK
SACL BANK
OUT BANK, BSR
OUT IOP4,BCLEAR

* enable the A/D 1 chip select(CS)

LACK BKFFFF
SACL BANK

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Appendix D  The List of DSP Assembly Source Code

OUT   BANK, BSR
IN    ACTULI, RADC1

LACK   IOBANK
SACL   BANK
OUT    BANK, BSR
OUT    IOP4, BITSET

* 1.5  start A/D converter 2 for position
LACK   IOBANK
SACL   BANK
OUT    BANK, BSR
OUT    IOP3, BSET

NOP
NOP
NOP
NOP

LACK   BKFFFF
SACL   BANK
SACL   FFFF
OUT    BANK, BSR
OUT    FFFF, SADC2

* 1.6  convert position sample into a 16-bit variable
LAC    ACTLP0, 4
SACL   ERRP0

* convert ACTLP0 into a two

* 1.7  Scale position error KPs*ERRp, KPs is predefined, and implemented in 16-bit x 16-bit
LT     KPS2
MPY    ERRP0
PAC
SACH   ERRP0, 1
SACL   ERRP1
ZALH   ERRP1
SACH   ERRP1, 4
ZALH   ERRP1
SACH   ERRP1, 1

* 2.  Position Loop Algorithms
* 2.1  Compute notch compensator

ZALH   ERRP0
ADDS   ERRP1
LST    RSOFLW
SUBS   W1
SUBH   W0
SACH   V0
SACL   V1
BV     OFLW1
OFLW1  NOP

* 2.1  IST SUBTRACTION

ZALH   V0
ADDS   V1
LST    RSOFLW
SUBS   X1
SUBH   X0
SACH   V0
SACL   V1
BV     OFLW2
OFLW2  NOP
* 2.2 Read the A/D converter 2 for position sampling

```
LACK IOBANK
SACL BANK
OUT BANK.BSR
OUT IOP9.BCLEAR

LACK BKFFFF
SACL BANK
OUT BANK.BSR
IN POS10.RADC2

LACK IOBANK
SACL BANK
OUT BANK.BSR
OUT IOP9.BITSET
```

* 2.3 Compute position lead compensator

```
ZALH REFI0
ADDS REFI1
LST RSOFLW
SUBS PWL1
SUBH PWLO
SACH PVLO
SACL PVL1
BV PFLW1
```

PFLW1

```
LT PPL
NOP
MPY PWLO
PAC
```

* 251
Appendix D  The List of DSP Assembly Source Code

SACH  REFI0,1
SACL  REFI1

*  LT   PQL
    NOP
    MPY  PWL0
    PAC
    SACH  RTMP10,1
    SACL  RTMP11

*  ZALH  REFI0
    ADDS  REFI1
    LST   RSOFILW
    SUBS  WG1
    SUBH  WG0
    SACH  REFI0
    SACL  REFI1
    BV    PFW1

PFW1  NOP
*  2.4 Compute lag compensator
*  ZALH  REFI0
    ADDS  REFI1
    LST   RSOFILW
    SUBS  WG1
    SUBH  WG0
    SACH  REFI0
    SACL  REFI1
    BV    PFW1

PFWG1  NOP
*  LT   PG
    NOP
    MPY  VG0
    PAC
    SACH  REFI0,1
    SACL  REFI1
    ZALH  REFI1
    SACH  REFI1,1

*  ZALH  REFI0
    ADDS  REFI1
    LST   RSOFILW
    ADDS  REFI1
    ADDH  REFI0
    SACH  REFI0
    SACL  REFI1
    BV    OFLWG

OFLWG  NOP
*  ZALH  REFI0
    ADDS  REFI1
    LST   RSOFILW
    ADDS  REFI1
    ADDH  REFI0
    SACH  REFI0
    SACL  REFI1
    BV    OFLWG1

OFLWG1 NOP
*  LT   KG
    NOP
    MPY  REFI0
    PAC
    SACH  REFI0,1

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Appendix D  The List of DSP Assembly Source Code

** 2.5 gain-schedule control algorithms**

* Compute the gain schedule compensator
  \[ \text{Vs} = \text{REFI} \cdot \text{Ws} \]

* \[ \text{REFI} = \text{Ps} \cdot \text{Vs} + \text{Qs} \cdot \text{Ws} \]

...
Appendix D  The List of DSP Assembly Source Code

PAC
SACH       RTMP10
SACL       RTMP11
ZALH       REFI0
ADDS       REFI1
LST        RSOFLW
ADDS       RTMP10
ADDH       RTMP11
SACH       REFI0
SACL       REFI1
BV         OFLWS1
OFLWS1     NOP

* 2.6 Scale REFI KP*REFI  (2 word X 1 word) KP is predefined
*
LINEAR     LAC       POSIO
SACL       POSI1
LT         KP
NOP        
MPY        REFI0
PAC        
SACH       REFI0,1
SACL       REFI1

** left shift 1
ZALH       REFI0
ADDS       REFI1
LST        RSOFLW
ADDS       REFI1
ADDH       REFI0
SACH       REFI0
SACL       REFI1
BV         OFLWS1
OFLS1      NOP

* 3 Current Loop Algorithms
* 3.1 Scale current feedback
* 3.2 Compute ERRI = REFI - MI2W
ZALH       REFI0
ADDS       REFI1
LST        RSOFLW
SUBS       MI2W1
SUBH       MI2W0
SACH       ERRI0
SACL       ERRI1
BV         OFLW5
OFLW5      NOP

* 3.3 Compute current lead ERRI*Gl(s)
*  
ZALH       ERRI0
ADDS       ERRI1
LST        RSOFLW
SUBS       WL1
SUBH       WL0
SACH       VL0
SACL       VL1
3.4 Compute the second current controller $CNTRL^*G_I2(s)$

\[
\begin{align*}
\text{ZALH} & \quad CNTRL0 \\
\text{ADDS} & \quad CNTRL1 \\
\text{LST} & \quad \text{RSOFIL} \\
\text{SUBS} & \quad \text{WL21} \\
\text{SUBH} & \quad \text{WL20} \\
\text{SACH} & \quad \text{VL20} \\
\text{SAACL} & \quad \text{VL21} \\
\text{BV} & \quad \text{OFlW1}
\end{align*}
\]

3.4 Scale the output $CNTRL^* (K_I/N)$

\[
\begin{align*}
\text{LT} & \quad K_I \\
\text{NOP} & \\
\text{MPY} & \quad CNTRL0 \\
\text{PAC} & \\
\end{align*}
\]
Appendix D

The List of DSP Assembly Source Code

SACH   CNTRL0,1
SACL   CNTRL1

*   CNTRL*25 (=2^8)
   ZALH   CNTRL0
   ADDS   CNTRL1
   SACH   TEMP
   SACL   LOW

*   left shift entire ACC 4 bits
   SACH   HIGH,4
   ZALH   LOW
   SACH   LOW,4

*   left shift entire ACC another 4 bits
   ZALH   HIGH
   ADDS   LOW
   SACH   HIGH,4
   ZALH   LOW
   SACH   CNTRL1.4

*   recover the sign bit in the high ACC bits
   LAC   TEMP
   AND   H8000
   SACL   SIGN
   LAC   HIGH
   AND   H7FFF
   OR   SIGN
   SACL   CNTRL0

*   5   output to D/A converter
   LAC   CNTRL0,>C
   ADDH   H800
   SACH   CNTRL
   LACK   BKFFFF
   SACL   BANK
   OUT   BANK,BSR
   OUT   CNTRL,DAC1

*   6   Delta operation for position loop algorithms
*   6.1   notch compensator
   LT   D2
   NOP
   MPY   W0
   PAC
   SACH   RTMP00,1

   ZALH   X0
   ADDS   X1
   LST   RSOFL,W
   ADDS   RTMP01
   ADDH   RTMP00
   SACH   X0
   SACL   X1
   BV   OFLW8

OFLW8
   NOP

*   LT   D1
   NOP
   MPY   V0
   PAC
   SACH   RTMP00,1

*   ZALH   W0
   ADDS   W1
   LST   RSOFL,W
   ADDS   RTMP01
   ADDH   RTMP00
   SACH   W0

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The List of DSP Assembly Source Code

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* 6.2 lead compensator

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* 6.3 delta operation for position lag controller

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* 6.4 gain-scheduled controller

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LT
NOP
MPY
PAC
SACH
SACL
ZALH
SACH
ZALH
ADDS
LST
ADDS
ADDH
SACH
SACL
BV
OFLWS3
NOP

* 7 Delta operation for current loop

* 7.1 current lead compensator

ZALH
BGEZ
ADDH
SACH
ZALH
SACH
ZALH
LPN9
ADDS
SACH
NOP
NOP
MULTN9
LT
NOP
MPY
PAC
SACH
AND
SACH
MPY
PAC
ADD
SACH
SACL
LAC
ADDS
SACL
NOP

+ OFLW10
NOP

* 7.2 second current compensator

ZALH
LST
ADDS
LST
ADD
SACH
SACL
BV
OFLW10
NOP

+ OFLW10
NOP

* 7.2 second current compensator

ZALH
ADDS
LST
ADDS

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The List of DSP Assembly Source Code

\begin{verbatim}
ADDH   VL0
SACH   VL0
SACL   VL1
BV     OVFI

OVFI   NOP
* multiply by DL2/2
  LT   DL2
  NOP
  MPY   VL20
  PAC
  SACH   RTMP00,1
  SACL   RTMP01

  ZALH   WL20
  ADDS   WL21
  LST   RSOFILW
  ADDS   RTMP01
  ADDH   RTMP00
  SACH   WL20
  SACL   WL21
  BV     OFIW2

OFIW2   NOP
* 8. Interrupt Routine Service (IRS) is finished

  FINISH   LACK   IBANK
  SACL   BANK
  OUT   BANK,BSR
  OUT   CLINT1,FCLEAR

  OUT   BKSAVE,BSR
  ZALH   HIHACC
  ADDS   LOWACC
  EINT   RET

* look-up table for the gain-scheduled controller

  AORG   > 500

  G1   DATA   21850
  G2   DATA   21790
  G3   DATA   21614
  G4   DATA   21327
  G5   DATA   20938
  G6   DATA   20457
  G7   DATA   19897
  G8   DATA   19274
  G9   DATA   18600
  G10  DATA   17890
  G11  DATA   17157
  G12  DATA   16412
  G13  DATA   15665
  G14  DATA   14925
  G15  DATA   14199
  G16  DATA   13491
  G17  DATA   12807
  G18  DATA   12149
  G19  DATA   11519
  G20  DATA   10919
  G21  DATA   10348
  G22  DATA   9807
\end{verbatim}
The List of DSP Assembly Source Code

| G23 | DATA | 9295 |
| G24 | DATA | 8812 |
| G25 | DATA | 8356 |
| G26 | DATA | 7926 |
| G27 | DATA | 7522 |
| G28 | DATA | 7142 |
| G29 | DATA | 6784 |
| G30 | DATA | 6448 |
| G31 | DATA | 6132 |
| G32 | DATA | 5834 |
| G33 | DATA | 5554 |
| G34 | DATA | 5291 |
| G35 | DATA | 5044 |
| G36 | DATA | 4811 |
| G37 | DATA | 4591 |
| G38 | DATA | 4384 |
| G39 | DATA | 4189 |
| G40 | DATA | 4005 |
| G41 | DATA | 3831 |
| G42 | DATA | 3668 |
| G43 | DATA | 3513 |
| G44 | DATA | 3366 |
| G45 | DATA | 3228 |
| G46 | DATA | 3097 |
| G47 | DATA | 2972 |
| G48 | DATA | 2855 |
| G49 | DATA | 2743 |
| G50 | DATA | 2638 |
| G51 | DATA | 2537 |
| G52 | DATA | 2442 |
| G53 | DATA | 2351 |
| G54 | DATA | 2265 |
| G55 | DATA | 2183 |
| G56 | DATA | 2105 |
| G57 | DATA | 2031 |
| G58 | DATA | 1960 |
| G59 | DATA | 1893 |
| G60 | DATA | 1829 |
| G61 | DATA | 1767 |
| G62 | DATA | 1709 |
| G63 | DATA | 1653 |
| G64 | DATA | 1599 |
| G65 | DATA | 1548 |
| G66 | DATA | 1499 |
| G67 | DATA | 1453 |
| G68 | DATA | 1408 |
| G69 | DATA | 1365 |
| G70 | DATA | 1324 |
| G71 | DATA | 1285 |
| G72 | DATA | 1248 |
| G73 | DATA | 1211 |
| G74 | DATA | 1177 |
| G75 | DATA | 1144 |
| G76 | DATA | 1112 |
| G77 | DATA | 1081 |
The List of DSP Assembly Source Code

G78 DATA 1052
G79 DATA 1024
G80 DATA 997
G81 DATA 970
G82 DATA 1081
G83 DATA 1211
G84 DATA 1365
G85 DATA 1548
G86 DATA 1767
G87 DATA 2031
G88 DATA 2351
G89 DATA 2743
G90 DATA 3228
G91 DATA 3831
G92 DATA 4591
G93 DATA 5554
G94 DATA 6784
G95 DATA 8356
G96 DATA 10348
G97 DATA 12807
G98 DATA 15665
G99 DATA 18600
G100 DATA 20938
G101 DATA 21850
G102 DATA 20938
G103 DATA 18600
G104 DATA 15665
G105 DATA 12807
G106 DATA 10348
G107 DATA 8356
G108 DATA 6784
G109 DATA 5554
G110 DATA 4591
G111 DATA 3831
G112 DATA 3228
G113 DATA 2743
G114 DATA 2351
G115 DATA 2031
G116 DATA 1767
G117 DATA 1548
G118 DATA 1365
G119 DATA 1211
G120 DATA 1081
G121 DATA 970
G122 DATA 997
G123 DATA 1024
G124 DATA 1052
G125 DATA 1081
G126 DATA 1112
G127 DATA 1144
G128 DATA 1177
G129 DATA 1211
G130 DATA 1248
G131 DATA 1285
G132 DATA 1324
Appendix D

The List of DSP Assembly Source Code

G132 DATA 1365
G133 DATA 1408
G134 DATA 1453
G135 DATA 1499
G136 DATA 1548
G137 DATA 1599
G138 DATA 1653
G139 DATA 1709
G140 DATA 1767
G141 DATA 1829
G142 DATA 1893
G143 DATA 1960
G144 DATA 2031
G145 DATA 2105
G146 DATA 2183
G148 DATA 2265
G149 DATA 2351
G150 DATA 2442
G151 DATA 2537
G152 DATA 2638
G153 DATA 2743
G154 DATA 2855
G155 DATA 2972
G156 DATA 3097
G157 DATA 3228
G158 DATA 3366
G159 DATA 3513
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G165 DATA 4591
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