DSP-based active power filter

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DSP-BASED
ACTIVE POWER FILTER

by

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September 1998

A Doctoral Thesis submitted in partial fulfilment
of the requirements for the award of the
degree of Doctor of Philosophy
of Loughborough University

Supervisor: J. G. Kettleborough

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Certificate of Originality

This is to certify that I am responsible for the work submitted in this thesis, that the original work is my own except as specified in acknowledgements or footnotes, and that neither the thesis nor the original work contained therein has been submitted to this or any institution for a higher degree.

Signature : ............................................

Date : .............................................
ACKNOWLEDGEMENTS

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Finally, I would also like to thank everybody in the Electronic and Electrical Engineering Department, namely the laboratory technicians and in particular Dr. Keith Gregory, who had contributed to the success of the project.
SYNOPSIS

Harmonics in systems are conventionally suppressed using passive tuned filters, which have practical limitations in terms of the overall cost, size and performance, and these are particularly unsatisfactory when large number of harmonics are involved.

Active power filtering is an alternative approach in which the filter injects suitable compensation currents to cancel the harmonic currents, usually through the use of power electronic converters. This type of filter does not exhibit the drawbacks normally associated with its passive counterpart, and a large number of harmonics can be compensated by a single unit without incurring additional cost or performance degradation.

This thesis investigates an active power filter configuration incorporating instantaneous reactive power theory to calculate the compensation currents. Since the original equations for determining the reference compensation currents are defined in two imaginary phases, considerable computation time is necessary to transform them from the real three-phase values.

The novel approach described in the thesis minimises the required computation time by calculating the equations directly in terms of the phase values i.e. three-phase currents and voltages. Furthermore, by utilising a sufficiently fast digital signal processor (DSP) to perform the calculation, real-time compensation can be achieved with greater accuracy.

The results obtained show that the proposed approach leads to further harmonic suppression in both the current and voltage waveforms compared to the original approach, due to considerable reduction in the computation time of the reference compensation currents.
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<thead>
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<tbody>
<tr>
<td>B</td>
<td>Number of system branches</td>
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<tr>
<td>([ \text{CBM} ] )</td>
<td>Branch / mesh current transformation matrix</td>
</tr>
<tr>
<td>([ \text{CBM} ]' )</td>
<td>Transpose of ([ \text{CBM} ] )</td>
</tr>
<tr>
<td>([ \text{CR} ], [ \text{CC} ] )</td>
<td>Rectifier and converter conduction pattern matrices</td>
</tr>
<tr>
<td>d</td>
<td>(d / dt) Rate-of-change of current</td>
</tr>
<tr>
<td>(\text{di} / \text{dt})</td>
<td>Rate-of-change of current</td>
</tr>
<tr>
<td>(e_a, i_a)</td>
<td>Real a-axis voltage and current</td>
</tr>
<tr>
<td>(e_b, i_b)</td>
<td>Real b-axis voltage and current</td>
</tr>
<tr>
<td>(e_c, i_c)</td>
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<td>(e_\alpha, e_\beta)</td>
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<td>([ I_B ], [ I_M ] )</td>
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<tr>
<td>(i^{*}<em>{Ca}, i</em>{Ca})</td>
<td>Reference and actual real (a)-axis compensation currents</td>
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<td>(i_\alpha, i_\beta)</td>
<td>Imaginary (\alpha)-axis and (\beta)-axis currents</td>
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<tr>
<td>(i_{ap}, i_{bp})</td>
<td>Imaginary (\alpha)-axis and (\beta)-axis instantaneous active currents</td>
</tr>
<tr>
<td>(i_{aq}, i_{pq})</td>
<td>Imaginary (\alpha)-axis and (\beta)-axis instantaneous reactive currents</td>
</tr>
<tr>
<td>(i^{<em>}_{Ca}, i^{</em>}_{Cb})</td>
<td>Reference imaginary (\alpha)-axis and (\beta)-axis compensation currents</td>
</tr>
</tbody>
</table>
[L_B], [L_M] Branch and mesh inductance matrices

N Number of nodes

p, q Total instantaneous active and reactive powers

p_\alpha, p_\beta Instantaneous imaginary \(\alpha\)-axis and \(\beta\)-axis powers

p_{ap}, p_{aq} Instantaneous imaginary \(\alpha\)-axis active and reactive powers

p_{bp}, p_{bq} Instantaneous imaginary \(\beta\)-axis active and reactive powers

[R_B], [R_M] Branch and mesh resistance matrices

S Number of independent circuits i.e. not electrically connected

v_{ac}, v_{ba}, v_{cb} Supply line voltages

[V_B], [V_M] Branch and mesh voltage vectors

v_{dc}, i_{dc} DC link voltage and current

v_{load}, i_{load} Load voltage and current

[Z_B], [Z_M] Branch and mesh impedance vectors

All other symbols are defined as they appear.
CHAPTER 1

INTRODUCTION

Harmonic distortion in electrical power systems is not entirely a new phenomenon. Until the advent of thyristors in the 1950s, the problems arising from harmonics were not significant, but its introduction has led to a rapid increase in the utilisation of new types of motor controller and power conditioner, all of which have non-linear qualities.

Although power electronic converters exhibit many useful features, such as large energy handling capability and ease of control, they inevitably draw distorted currents from the supply. These currents subsequently produce harmonic voltages, which propagate throughout the supply network, polluting the sinusoidal nature of the a.c. supply.

Harmonics not only degrade the quality of the supply, they also contribute to other detrimental effects in both the power system and susceptible nearby equipment. Chapter 2 elaborates on harmonics in power systems, and a discussion on harmonic sources and their unwanted effects is also included. Furthermore, several important aspects of harmonics are also briefly explained, to provide an overview of how harmonics are represented and analysed.

In an attempt to ensure that the a.c. supply is within acceptable harmonic limits, supply authorities imposed specific regulations on the consumer. In order to comply with these regulations, it is imperative that the harmonics from the polluted supply are minimised, if not eliminated. Furthermore, the suppression scheme should at least compensate for the principal harmonic components, particularly those of low-order.

The conventional method for eliminating harmonics is by the use of passive tuned filters, consisting of combinations of capacitors, inductors and resistors. The operation of this type of filter is based on the frequency characteristic of the capacitive and inductive reactances,
which can be configured to provide a low impedance path for any specific harmonic frequency.

One filter per phase is required for each harmonic component to be compensated. Since the harmonic amplitudes are inversely proportional to the harmonic order, it is common practice to provide individual filters for the low-order harmonics and a low-pass filter for the remaining harmonics in the system.

Although the performance of passive filters is generally adequate, in practice they are not completely satisfactory. Their main drawback is the high initial cost associated with the filter components, which have to be rated for high operating voltages and have a very high Q factor to obtain a sharp tuning effect. They are often very bulky with the overall size being directly proportional to the number of harmonics to be compensated.

Unfortunately, the performance of passive filters may deteriorate due to factors such as component detuning, electromagnetic interference and resonance. Another weakness they possess is the inability to adapt continuously with the variation in the system harmonics, which may render the filter less effective when the harmonic content increases. This can only be remedied by installing additional filter units, tuned to the new harmonic frequencies.

Over the years, many alternative harmonic suppression schemes have been proposed, with varying degree of complexity and improvements. This has mainly been done to overcome the problems relating to passive filters, and to enhance the suppression performance during both steady-state and transients. However, the required suppression accuracy and flexibility of operation could not always be successfully achieved by the majority of these approaches, with the exception of active power filter schemes.

The active power filter is capable of producing compensating currents of the appropriate phase and magnitude to suppress the harmonic currents in the supply. Using the distorted supply
currents and voltages, these currents are usually determined using an algorithm, and they are generated using a pulse-width modulation (PWM) power converter acting as an external current source, e.g. a voltage-source or current-source converter.

These compensation currents are injected at the common coupling point, which is typically midway between the harmonic source and the supply. Figure 1.1 shows the general arrangement for an active power filter compensation scheme, with the filter injecting compensation currents which are equal in magnitude but in anti-phase with the harmonic currents produced by the non-linear load, in order to eliminate harmonics at the supply.

This scheme offers several advantages over other methods. Only one item of plant is required to achieve continuous compensation of all harmonics, without needing to update the filter as the system harmonics vary. Any changes in the harmonic components, either in magnitude or frequency, can be accounted for by simple control adjustment, rather than by costly and time consuming equipment changes.

There is theoretically no limit to the maximum number of harmonics that this type of filter can suppress, and the practical limit is imposed mainly by the switching scheme and converter employed. Another advantage of utilising active filters is that some VAR compensation may also be achieved simultaneously, since the absence of harmonics restores the lagging power factor to at least near unity.

Despite their superiority over passive filters, active filters are still not ideal. Most of the early schemes are often either too complex to be implemented, or they do not compensate the harmonics satisfactorily. Chapter 3 discusses several aspects of filtering techniques, with particular emphasis given to the proposed scheme employed in this research.

The main objective of the current research is to develop a novel active filter configuration based on instantaneous reactive power theory [1,2]. The fundamental theory which is
explained in Chapter 4, was initially intended for VAR compensation purposes. The original equations for calculating the compensation currents in a three-phase three-wire power system were defined in an imaginary two phase system, which is referred to as method A throughout this thesis. Inevitably, this method requires considerable computation time in transforming from two to three phases.

The computation time may be minimised by avoiding the transformation stages, by calculating directly using the phase value of the currents and voltages. This method is referred to as method B in the thesis, and it is shown that the apparent benefit of reduced computation time is a superior real time suppression performance, due to almost instantaneous harmonic cancellation effect.

Calculation of the required compensation currents is achieved using a specialised high-speed microprocessor chip, to provide a sufficiently fast numerical computation for real time compensation. The Texas Instrument TMS320C50x DSP Starter Kit (DSK) was employed, with a typical operating speed of 40 MHz and an instruction execution time of 50 ns. The use of a DSP enhances the flexibility of the filter operation, because the algorithm can be programmed directly via a personal computer and any modification or upgrade can be made immediately.

Injection of the compensation currents is achieved using a PWM voltage source converter operating at a switching frequency of 8 kHz. IGBTs are used as the power switches due to the their high energy rating, ease of control and relatively low price. They are switched using a fixed-frequency hysteresis current controller to modulate currents as close as possible to the required compensation currents, as determined by the instantaneous reactive power theory equations.

In order to validate the theory, a computer program was written in Prospero Fortran 77 to simulate the power system, which can be operated with or without the filter for comparison.
purposes. Chapter 5 discusses in detail the various aspects of the simulations, particularly the mathematical models involved.

An active filter experimental rig was constructed for the use in the research, and this can be classified into three main sections: power, control and calculation circuits. Chapter 6 explains the hardware implementation for the power and control circuits, detailing the function of each individual circuit within these two sections. The power circuit consists of the PWM converter and rectifiers, and all associated circuits, and the control circuit comprises the remaining electronic circuits which control the operation of the converter and handles the input/output data to the calculation circuit.

The purpose of the calculation circuit is to implement the actual computation of the proposed equations and to generate the reference signals representing the required compensation currents, which is discussed in Chapter 7. It consists of the TMS320C50x DSK with the purpose-built input/output interface circuit, and the computation algorithm and the converter control strategy are also included.

The practical experiments carried out using the experimental system are explained in Chapter 8. Three different conditions were investigated: a balanced load without an active filter, a balanced load with an active filter using method A and a balanced load with an active filter using method B. A discussion section is also included to explain the analytical interpretation made through inspection of the simulation and experimental results obtained, to enable the performance of the proposed active power filter scheme will be evaluated.

Chapter 9 concludes the thesis, giving the final verdict on the research work done and suggesting further development work that could be undertaken.
AC supply \rightarrow \text{Non-linear load} \leftarrow \text{Active power filter}

**Figure 1.1**: General arrangement for an active power filter scheme
Harmonics in a.c. electrical power systems are often produced by non-linear loads such as saturated transformers and rotating electrical machines. In addition, the rapidly expanding use of power electronic converters for motor drives, electro-chemical and heating processes etc, is accompanied by the corresponding increase in harmonic levels.

Other sources of disturbances exist which alter the sinusoidal nature of currents and voltages, such as voltage spikes or flicker [3], outage or blackout [4], overvoltage, chopped voltage waveform, undervoltage or brownout and electromagnetic interference.

Other disturbances often result from defects, malfunctions or improper system design. They inherently introduce effects that are intermittent and uncharacteristic in nature, which are complex to predict or compensate and are best prevented.

2.1 NATURE OF HARMONICS

By definition, the term harmonic applies to the sinusoidal components of a repetitive waveform, such as the a.c. supply, that are exact multiples of the basic repetition frequency (the fundamental component).

Any non-sinusoidal a.c. supply can be investigated using Fourier analysis (Appendix 1). An important concept in this approach is that no energy transfer can take place through voltages and currents that are of different frequencies. For example, the net power per cycle resulting from a fundamental voltage and a 5th harmonic current is zero.
In any balanced three-phase system, the general expression for the current at any frequency is given by:

\[ I_n = I_a + I_b + I_c \]

\[ = I_0 \sin n(\omega t) + I_0 \sin \left(\omega t + \frac{2\pi}{3}\right) + I_0 \sin \left(\omega t + \frac{4\pi}{3}\right) \]  

(2.1)

where  

- \( I_n \) = Neutral phase current  
- \( I_a \) = a-phase current  
- \( I_b \) = b-phase current  
- \( I_c \) = c-phase current  
- \( n \) = Harmonic order

It follows from Equation 2.1 that the third and all the other triplen current harmonics are cophasal. This implies the need to provide a proper path to allow these currents to flow, which is normally accomplished by providing either an additional delta-connected winding on a transformer or by a neutral connection to give a 4-wire system.

In general, lower-order harmonics tend to be the dominant components in producing heating effect, particularly in rotating machines, with the temperature rise being approximately proportional to the square of the magnitude of the voltage distortion [5]. This generalisation is however less true when considering variable-speed motors controlled by inverters, where the heating is caused mainly by high-frequency components produced by the inverter drive.

Unbalanced loads, such as single-phase rail traction, have a major affect on the phase balance of the harmonics. All the harmonics are composed of both positive and negative phase sequence components, and the r.m.s. total of all the negative phase sequence components is an important aspect in determining the internal heating of rotating machines.
2.2 SPECTRA AND ORDER OF HARMONICS

The harmonic spectra produced by non-linear devices usually comprise characteristic harmonics e.g. the 3rd or 5th in transformer magnetising currents [6] and mainly the 5th in television receivers [7]. Symmetrical phase control of current (e.g. using a triac) produces primarily odd harmonics, whereas asymmetrical phase control (e.g. using a thyristor) generates both odd and even harmonics, and also a d.c. component [8]. At any given power level, the harmonic content when under asymmetrical control is significantly higher than when under symmetrical control.

The pulse number (p) of a power converter is defined as the number of non-simultaneous commutations per cycle of the fundamental frequency, and the principal output harmonics in power electronics converters have a characteristic order of \((pk \pm 1)\), where k is any positive integer. Thus, a 6-pulse converter generates 5th and 7th order components as its principal output harmonics. The converter will also generate characteristic voltage harmonics of order \((pk)\) on the d.c. side.

The derivation of the characteristic harmonic is usually based on the assumptions that:

a) The commutation impedances are equal in all three phases, which means that all the overlap angles are the same.

b) Device conduction commences at the same time in each cycle and the conduction pattern is symmetrical.

c) The d.c. current contains no significant frequency components.

d) The a.c. supply voltages are balanced.

In practice, small levels of uncharacteristic harmonics are present, at frequencies other than
pk or pk ± 1. These occur in a random manner and cannot easily be expressed analytically because they are caused by imperfections [9] or faults. Probable causes include transients, device firing errors, remote modulation of d.c. current and unequal converter commutation reactances.

Under normal steady-state conditions, the harmonic amplitudes tend to be inversely proportional to the harmonic order. Consequently, the low-order components are usually important because their amplitudes contribute significantly to degradation of the supply quality.

2.3 FERRORESONANCE

Ferroresonance [6,10] is a harmonic phenomenon resulting from the interaction between the non-linear inductance of, for instance, a transformer and the system capacitance. It is caused by the ferromagnetic-cored inductor being energised abnormally while interchanging stored energy with the capacitance, producing core saturation and large overvoltages, and it may also exhibit subharmonic effects.

Subharmonics and superharmonics typically caused by power system resonance, switching generators and fault conditions, are at frequencies significantly below and above the system fundamental frequency.

Subharmonic frequencies of one-third and one-fifth of the fundamental frequency are particularly harmful, and cause considerable vibration in machines, maloperation of protection equipment, overcurrents and overvoltages. Superharmonic frequencies are however normally suppressed due to high frequency damping.
2.4 HARMONIC SOURCES

The non-linear loads that are responsible for harmonic distortion may be categorised into three main groups:

a) Supply systems: HVDC converter stations, thyristor controlled static VAR compensators and power transformers.

b) Industrial: Electric arc furnaces, traction loads, discharge lightings, large rectifiers (e.g. aluminium smelters), controlled converters (e.g. mine winders and rolling mills), motor soft-start units, cycloconverters, pulse burst heating, induction machines and synchronous machines.

c) Domestic: Television sets, fluorescent lamps, light dimmers, radio, computer equipment, ballast inductors in light fittings and uninterruptable power supplies (UPS).

Applications involving power electronic devices make up a large proportion of the harmonics disturbances that are generated, but the contributions of other sources cannot be overlooked. The magnitudes of the harmonics produced by individual television sets and fluorescent lamps may be considerably smaller than those produced by for instance, HVDC converter stations, but the very large number of units in service leads to significant distortion.

2.5 EFFECTS OF HARMONICS

The widespread and undesirable presence leads to:
a) Heating of the conductors and iron of electrical machines.

b) Additional eddy current losses at harmonic frequencies.

c) Harmonic resonant effects, giving rise to excessive voltages and currents, in high Q circuits.


e) Pulsating harmonic torques in rotating machines that increase the machine vibration noise level, and may cause problems if they coincide with the natural frequencies of the system.

f) Overstressing and overheating of the dielectrics in high voltage cables.

g) Increased levels of corona on high-voltage transmission lines.

h) Interference with communication, control, protection and signalling circuits, either through electromagnetic induction or the flow of ground currents.

i) Erroneous meter readings.

j) Malfunctioning of sensitive devices, such as communication and computer equipment.

k) Burning out of small auxiliary components, such as fluorescent lamp capacitors.

l) Ferroresonance effects can lead to subharmonic phenomenon, causing both overvoltages and overcurrents.

m) Lamp flickering, particularly when subharmonics are involved.
2.6 ANALYSING HARMONICS

There are several ways of analysing harmonics and their effects, and these are outlined in the following sections.

2.6.1 FOURIER REPRESENTATION OF HARMONICS

Provided that the distorted waveform is repetitive, it can be decomposed using Fourier analysis (Appendix 1) into separate sinusoidal components of the fundamental and harmonic frequencies. Subsequently, the system behaviour due to each harmonic component can be studied separately, and the overall effect obtained by superposition.

2.6.2 HARMONIC IMPEDANCE

In assessing the susceptibility of power systems to harmonics, it is essential to know the harmonic impedance behaviour at the common coupling point. The numerical values of the harmonic impedances are obtained using the voltage obtained at this point, when a 1 p.u. current is injected there.

In general, the harmonic impedance of an a.c. network as measured at the common coupling point exhibit the following characteristics:

a) An increase in fault level tends to increase the impedance.

b) The maximum impedance is lower at high loads than at low loads.

c) A line outage will cause a significant impedance change.
d) The fundamental short-circuit level bears no relationship to the harmonic impedances.

e) Damping effect can be provided by certain type of loads, whose impedance increases with harmonic frequency.

f) The impedances of cables are lower than those of overhead lines, where higher order harmonics (15th to 25th) are concerned.

In practice, filters themselves generate harmonic currents, which in turn introduce harmonic voltages into the system they are compensating. This is unacceptable above a certain level, and filters are therefore required to provide low impedance paths for the harmonic currents in order to limit the voltage distortion.

2.6.3 TOTAL VOLTAGE DISTORTION

One filter design criterion is the total voltage distortion caused by all the harmonic components in the voltage waveform. It is defined by:

\[ V_{TD} = \sqrt{\sum_{n=2}^{\infty} V_{hn}^2} \]  

(2.2)

where \( V_{hn} \) = Harmonic voltage of order \( n \)

2.6.4 TELEPHONE INFLUENCE FACTOR

The telephone influence factor (TIF) defines the effect of the distorted voltage or current waveform of a power line on the voice-frequency communication network. This may result from either electromagnetic or electrostatic induction, or both.
All harmonic frequencies within the human audible range are given high weighting factors, even if their magnitudes are small, since they may cause unacceptable telephone noise. The C-message weighting curve shown in Figure 2.1 provides a graphical representation of the relative weighting factors of speech impairment due to an interfering signal of frequency \( f \), as heard through a modern telephone system. Using this curve, the TIF may be expressed as:

\[
\text{TIF} = \frac{1}{X_t} \sqrt{\sum (5f P_f X_f)^2}
\]

where:
- \( X_t \) = Total effective or r.m.s. of current or voltage.
- \( X_f \) = Single-frequency effective current or voltage at frequency \( f \), including the fundamental.
- \( P_f \) = C-message weighting at frequency \( f \), obtained from the C-message weighting curve.

### 2.6.5 TOTAL HARMONIC DISTORTION

The total harmonic distortion (THD) indicates the cumulative distorting effect that the harmonics have on the fundamental waveform. It is normally stated in terms of the amplitudes of the fundamental and the harmonic components as:

\[
\text{THD (\%)} = \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1^2} \times 100
\]

where:
- \( A_1 \) = Amplitude of the fundamental
- \( A_n \) = Amplitude of the harmonic of order \( n \)
2.7 HARMONIC STANDARDS AND LIMITS

The limitation on the acceptable levels of current and voltage harmonics are given by standards, such as the Electricity Council in document G5/3 (September 1976). Other relevant national and international harmonic standards are summarised in Appendix 2.

Harmonic limits are closely related to the maximum unbalance that may be imposed on rotating electrical machines [6]. For example, the maximum negative phase sequence voltage at the terminals of an induction motor should not exceed 0.01 p.u.

For generators, the negative phase sequence current should not exceed 0.05 p.u., and usually trips are provided to operate if this current reaches 0.08 p.u. - 0.1 p.u. When considering harmonics and unbalance limits, it is important to analyse and impose the limits at the weakest point of the system.

2.8 HARMONIC SUPPRESSION

The suppression of harmonics can be achieved in several different ways:

a) Incorporating detuning capacitors.
b) Increasing the pulse number of converters.
c) Moving the harmonic source to a higher voltage source.
d) Modifying transformers.
e) Separate neutral conductors for non-linear loads.
f) Filtering.

In a weak system, power-factor correction capacitors may induce resonance, and result in harmonic current magnification. The capacitors must therefore be detuned using series-
connected reactors, where the reactance is inductive at the lowest principal harmonic frequency and above.

Increasing the pulse number reduces the generation of characteristic harmonics in a static conversion process [12]. Many schemes [13]-[15] enable the pulse number to be increased, but their utilisation is often hindered by the accompanying increase in the number and complexity of the transformers, and by associated insulation problems.

Moving the harmonics to a higher voltage source reduces the effect of the distortion, because this increases the relative magnitude of the fundamental voltage compared with the harmonics voltages.

Utilising non-standard zig-zag transformer configurations [16] and derating of transformers [17] can provide some harmonic suppression. Since this results in low efficiency of operation and increased heat losses, these schemes are uneconomical in practice. Another alternative is to utilise the expensive K-factor transformers [18], which are specifically designed to reduce harmonics.

Using separate neutral conductors for non-linear loads, and avoiding shared neutral conductors, particularly with the susceptible parts of the circuit can help to reduce harmonics. However, this approach is only suitable when such isolation is permissible, without incurring major design modifications.

Filtering is a common method for suppressing harmonics, and it may be employed either to minimise harmonic voltages or to eradicate system resonance conditions. Nevertheless, the application of filters is not straightforward, since it is possible for a filter to reduce one harmonic and to increase another, and their application should always be subjected to a thorough harmonic system study.
Figure 2.1: C-message weighting curve
CHAPTER 3
FILTERING HARMONICS

Even though eliminating power system harmonics using filters is less complicated and expensive than certain harmonic suppression schemes, it is still costly, particularly if the number of harmonics involved is large. The typical cost can be up to 15% of the total cost of a HVDC converter station, due mainly to the need for the filter to be rated for a high operating voltage and at the same time to have a high Q factor to ensure accurate frequency tuning.

The filtering process in power systems is considerably different from that in electronic circuits, particularly due to the magnitude of the harmonic currents that have to be eliminated. Power filters provide harmonic suppression by supplying suitable currents at a common coupling point, which reduces the harmonics when they interact with the supply currents. The type of filter is determined by the mechanism by which these currents are obtained, and how they are manipulated to produce the required result.

Section 3.1 highlights the critical power filter design criteria, and the different types of power filter are explained in Section 3.2. The compensation current injection techniques are discussed in Section 3.3, while the proposed scheme is presented later in Chapter 4.

3.1 FILTER DESIGN CRITERIA

The ultimate aim in power filter design is to eliminate completely all harmonics, and so remove all detrimental effects that result from distorted current and voltage waveforms. Moreover, the filter has to be robust so as to perform equally well in either the steady-state or during transient operation, regardless of changes in the magnitude, phase and number of
harmonics in the system.

These requirements can be achieved if the filter is continuously adaptive, and produces exactly the currents that are required to compensate the harmonics, without introducing any of disturbances in the process. However, this ideal filter criterion has not yet been successfully achieved in practice, particularly because the high specifications required are beyond the present state of the relevant component technology. Accurate forecasting of the flow of harmonic currents throughout the a.c. network is also difficult, except for small power systems.

Furthermore, it is uneconomic to attempt to achieve the ideal operating performance, because certain harmonic related problems are more cost effectively solved by taking appropriate preventive measures. The problem of telecommunication interference, for instance, can be solved successfully within the telephone network itself by incorporating proper cable shielding, equipment screening, audio filters etc.

Since an ideal power filter is not achievable, the practical design of a filtering scheme aims typically at compensating the principal harmonic components and any additional components, so as to comply with the relevant harmonic standards (Appendix 2). Moreover, particular consideration is given to suppressing the lower-order components, which tend to be of harmful high amplitudes.

### 3.2 DESIGN FACTORS

There are two major filter design concerns; the rating and the quality. The rating of a power filter is defined as the reactive power it supplies at the system frequency. On the other hand, the term quality (or Q-factor) refers to the sharpness of the frequency tuning, and is defined differently for tuned, low pass and high pass filters, due to the different current or voltage
A thorough understanding of the harmonic sources and the harmonic impedance of the network is essential in designing a satisfactory filter. For effective suppression, the filter needs to have a much lower impedance than the a.c. network at the harmonic frequencies, to provide a path through which the harmonic currents can flow. Moreover, it is preferable that the filter does not resonate with the network impedance, which may cause the filter to produce excessive reactive current and to become a harmonic source.

Filters may be arranged in either a series or a shunt configuration, and the choice depends primarily on the type of filtering scheme and the waveforms to be compensated, i.e. series and shunt filters for voltage and current waveforms, respectively. Shunt or parallel filters are common in power systems, because of the need to suppress harmonic currents, and they are also easy to install and protect from short-circuit faults.

The typical design criteria used to define the needs and performance of power filters are the telephone influence factor (Section 2.6.4) and the total voltage distortion (Section 2.6.5). For d.c. side filters in HVDC schemes, additional features such as the maximum permissible noise to ground in telephone lines and the maximum induced noise in a parallel test line one kilometre away, have also to be considered.

### 3.3 FILTER CLASSIFICATIONS

A variety of harmonic filter designs exists, but even though certain topologies exhibit sophisticated hybrid arrangements, filters can be classified into two main groups according to their operational characteristics. The two groups are termed passive and active filters, and are discussed in the following sections, with particular consideration given to the former group.
3.3.1 PASSIVE FILTERS

Passive filters are often more simple to implement, although they do not necessarily provide the best approach to suppressing harmonics. The filter does not require a separate power supply to operate, and it 'borrows' the power from the system it is compensating.

The main circuit consists of only passive components; resistors, capacitors and sometimes inductors. In principle, the operation is based on the frequency varying characteristic of the capacitive and inductive reactances, which may be configured to provide a low impedance path for the chosen harmonic frequencies.

Passive filters are often closely tuned to a specific harmonic frequency, with an allowance made to tolerate the detuning effects as the components age. One filter unit per phase is commonly required for each low-order harmonic component to be eliminated, while the overall suppression of the high-order components is achieved by a low-pass filter for each phase [19].

Even though the performance and reliability of passive filters was acceptable in the past, modern power systems with ever increasing harmonic levels demand more from filtering schemes. Many disadvantages of passive filters are now becoming apparent, and these can be summarised as:

a) Considerable bulk, particularly due to the physical size of high voltage capacitors.

b) The overall size increases with the number of harmonics to be compensated.

c) High installation costs associated with the high voltage ratings and small tuning tolerances.
d) They may act as a sink for the distortion components generated by nearby equipment.

e) Filtering is incomplete if the system harmonic impedance is not much greater than the filter impedance.

f) They tend to detune if the system operating frequency changes, or if the filter component values change due to ageing or temperature variations.

g) There is a risk of overloading a.c. side filters if the harmonic sources are on the a.c. system.

h) Overvoltages can result, since the filters may supply more VARs than are required by the converter when the power flow on the d.c. side is low.

3.3.2 ACTIVE FILTERS

Active filters comprise a combination of power electronic components designed to generate appropriate currents to reduce harmonics by injecting harmonic currents in anti-phase with the harmonic currents in the system. The filter operates as an ideal current source [20], supplying currents at the coupling point, and is normally shunt connected to the system.

Even though the use of active filters in electronics is common, their applications in power systems are still limited. The advantages they offer compared to their passive counterparts can be summarised as:

a) Only one unit is needed to compensate for all the harmonics, and this results in a relatively small overall size.
b) There is no theoretical limit to the maximum order of harmonic the filter can suppress, and the practical limit is mainly determined by the performance of the switching devices and scheme.

c) Changes in harmonic components in either frequency, phase or magnitude can be accounted for automatically, or by simple control adjustments, rather than by costly equipment upgrade.

d) An effective suppression performance during both transients and steady-state conditions is less dependent on the system harmonic impedance, component detuning, frequency changes or temperature variations.

When an active power filter approach was first considered [21] in the 1970s, component technology was not sufficiently advanced to ensure successful implementation. This was due mainly to the main circuit of an active filter requiring a high-speed current response and the need for a high-accuracy frequency converter.

The present day technology of fast and accurate computational electronic devices, has made feasible the concept of active power filtering. Moreover, the advent of high-speed and high-power switches, such as gate-turn-off thyristors (GTOs), insulated gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field effect transistors (MOSFETs) has made it possible to operate frequency converters with considerable accuracy.

Many prototype schemes have been proposed and researched in recent years, but the fundamental principles remain unchanged. The first of these is the detection of the phase and amplitude of the harmonic currents and voltages at the transmission line terminals, and the next is the injection of the appropriate anti-phase currents at the harmonic frequencies. If the detection and current injection processes can be achieved sufficiently quickly and accurately, the distortion can be almost instantaneously eliminated. In addition, reactive power
compensation can sometimes be achieved using certain active filter schemes.

The magnetic flux compensation method [21] uses a current transformer to detect the harmonic components in the source. The output is fed into the tertiary winding of a transformer through an amplifier, such that the harmonic currents in the primary are reduced. This method has the advantage that it handles uncharacteristic harmonics, but it is unable to remove significantly large magnitude low-order characteristic harmonics without the inclusion of a large power feedback amplifier.

A technique termed harmonic current injection involves modifying the rectangular current waveform at a converter input, by the introduction of a harmonic current from an external source. This scheme was originally proposed by Bird [22], and was further developed by Ametani [23], but it suffers from many disadvantages such as the need for a synchronised triplen harmonic current generator, an inability to nullify more than one harmonic order at any operating point, difficulty in the adjustment of the phase and amplitude of the injected current to match the operating condition, and a poor efficiency due to ineffective dissipation of the triplen harmonic power injected.

Ripple reinjection [13]-[15] involves developing a triple frequency current whose amplitude is determined by the magnitude and shape of the d.c. current. This current is injected into the neutral of the main transformer secondary and flows through the transformer winding, which contains only 12-pulse related current harmonics for a bridge rectifier (6-pulse). Overrating of the individual bridges by up to 25% is necessary to compensate for the unequal power sharing between parallel bridges. Other problems are a lack of control of the compensation under varying operating conditions, and the need for separate 5th and 7th harmonic filters. The existing 12-pulse HVDC system will not gain considerable improvement from adoption of this scheme [13].

Developments in technology have led to many schemes being proposed since the 1980s that
incorporate an external current source, through the use of inverters and particularly the PWM inverters. This class of active filters has a far better dynamic and transient performance, since the injected currents are approximately the current required to suppress the harmonic currents. Section 3.4 will discuss these schemes, which are similar to that investigated in the present research project.

3.4 COMPENSATION CURRENT INJECTION TECHNIQUES

These schemes involve the suppression of supply harmonics by generation of appropriate currents for injection at the common coupling point. To obtain the correct amplitude and phase for these currents, the filters are operated in a closed-loop configuration with the currents and/or voltages of the distorted supply being continuously monitored. A feedback signal to the main calculation unit leads to the production of a suitable reference signal to the power converter to modulate the required currents.

Static power converters for active power filters are commonly based on either a force-commutated pulse width modulated voltage-source inverter (PWM-VSI) connected to a d.c. capacitor, or a current-source inverter (PWM-CSI) connected to an inductor. Both inverters can operate in a self-sufficient manner and act as ideal current sources, which is an important characteristic for active filtering. Furthermore, the fast current switching capability allows the required compensation currents to be generated in real time with an acceptable level of accuracy.

Even though many schemes involving compensation current injection have been proposed, the significant difference between them is the way in which the compensation currents are derived by the current controller. Conventional methods [1] extract the phase and magnitude of these currents by passing the load current and/or voltage waveforms through discrete electronic circuits e.g. proportional integral (PI) controller, second-order band filter etc. This removes the
fundamental component of the load current, which is used to ensure that the filter output has zero gain attenuation and the phase shift is at the desired angle, typically 180°. Gating reference current signals are determined by summing this fundamental current component with the load current.

Synchronous reference frame flux-based calculation [24] is a technique which manipulates the linear relationship between the flux and current in a linear inductor. The controller ensures that the extraction of the harmonic components is obtained without any associated phase shift sensitivity. The scheme implements a hysteresis rule-based carrier-less PWM, which facilitates direct implementation of a current regulator without the explicit generation of a voltage reference for controlling the PWM inverter.

A scheme in which the line currents are actively conditioned through the leakage inductance of an isolation transformer is utilised in the sliding-mode controller [25] active filter. The wave-shaping function is achieved through the use of sliding-mode and proportional-integral (PI) controllers, which eliminate the need to calculate real or reactive power from the distorted load current. The controller constructs the desired line current through the superposition of the secondary side active filter current with the current drawn by the non-linear load, with appropriate consideration of the transformer turns ratio.

Several controllers based on the instantaneous reactive power theory [26]-[31] have been investigated; particularly due to the prospect of better compensation characteristics during steady-state and transient conditions. The compensation currents are calculated using the basic equations suggested by the theory, as discussed in depth in the next chapter. This theory determines the reference compensation currents by decomposing the three-phase load currents and voltages into two mutually orthogonal reference frames, and manipulates conventional power theory to compensate for the reactive power loss in the system. The reference currents control the PWM inverter switches, which produce compensation currents, to restore the reactive power and suppress harmonics.

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CHAPTER 4
INSTANTANEOUS REACTIVE POWER THEORY

4.1 FUNDAMENTAL THEORY

Instantaneous reactive power theory provides the equations necessary to calculate the
instantaneous values of current required to restore the reactive power and so cancel the
unwanted current harmonics. Consequently, it is suitable for active filtering operation, which
is primarily concerned with instantaneous values and not average or r.m.s values.

The original equations proposed in the theory [1,2] are defined in a mutually orthogonal \( \alpha-\beta \)
coordinate system. However, instead of using the \( \alpha-\beta \) coordinates, this research investigates
the direct implementation of the phase equations to determine the compensation currents. As
an introduction to the theory, the \( \alpha-\beta \) equations are developed, followed by the phase
equations.

The instantaneous voltages and currents of a three-phase circuit can be expressed in terms of
their instantaneous space vectors. For example, in an a-b-c coordinate system, the a, b and c
axes are fixed in the same plane, but are mutually separated by \( 120^\circ \). The individual
instantaneous space vectors \( e_m \) and \( i_m \) ( \( m = a, b \) or \( c \) ) are set on the m-axis, and their
amplitudes and polarities vary with respect to time.

These space vectors can be transformed into another chosen coordinate system i.e. the \( \alpha-\beta \)
mutually orthogonal coordinates as shown in Figure 4.1. Here, the new instantaneous space
vectors \( e_n \) and \( i_n \) ( \( n = \alpha \) or \( \beta \) ) are set on the n-axis, and their amplitudes and polarities again
vary with time.
The relationship between the initial (a-b-c) and the new (α-β) instantaneous space vectors are determined by the transformation:

\[
\begin{bmatrix}
\mathbf{e}_a \\
\mathbf{e}_\beta
\end{bmatrix} = \begin{bmatrix}
\frac{2}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\
0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}}
\end{bmatrix}
\begin{bmatrix}
\mathbf{e}_a \\
\mathbf{e}_b \\
\mathbf{e}_c
\end{bmatrix}
\tag{4.1}
\]

\[
\begin{bmatrix}
\mathbf{i}_a \\
\mathbf{i}_\beta
\end{bmatrix} = \begin{bmatrix}
\frac{2}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\
0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}}
\end{bmatrix}
\begin{bmatrix}
\mathbf{i}_a \\
\mathbf{i}_b \\
\mathbf{i}_c
\end{bmatrix}
\tag{4.2}
\]

Figure 4.2 illustrates an alternative way of visualising the new instantaneous space vectors in α-β coordinates. The instantaneous power in this system is defined as:

\[
p = \mathbf{e}_\alpha \cdot \mathbf{i}_\alpha + \mathbf{e}_\beta \cdot \mathbf{i}_\beta
\tag{4.3}
\]

which is equal to the value obtained using the a-b-c coordinate system:

\[
p = \mathbf{e}_a \cdot \mathbf{i}_a + \mathbf{e}_b \cdot \mathbf{i}_b + \mathbf{e}_c \cdot \mathbf{i}_c
\tag{4.4}
\]

Before introducing instantaneous reactive power, it is essential to define the instantaneous imaginary power space vector, which is:

\[
\mathbf{q} = \mathbf{e}_\alpha \times \mathbf{i}_\beta + \mathbf{e}_\beta \times \mathbf{i}_\alpha
\tag{4.5}
\]

\[
= \mathbf{e}_\alpha \mathbf{i}_\beta - \mathbf{e}_\beta \mathbf{i}_\alpha
\]
This vector is the imaginary axis vector, and is perpendicular to the real plane on the $\alpha$-$\beta$ coordinates. Its relative position can be obtained using the classical right-hand rule. From Figure 4.2, the conventional instantaneous power $p$ and the instantaneous imaginary power $q$ can be expressed as:

$$
\begin{bmatrix}
  p \\
  q
\end{bmatrix} =
\begin{bmatrix}
  e_\alpha & e_\beta \\
  -e_\beta & e_\alpha
\end{bmatrix}
\begin{bmatrix}
  i_\alpha \\
  i_\beta
\end{bmatrix}
\quad (4.6)
$$

The products $e_\alpha i_\alpha$ and $e_\beta i_\beta$ in Equation 4.6 have the conventional meaning of instantaneous power $p$ in Watts. However $e_\alpha i_\beta$ and $e_\beta i_\alpha$ do not represent instantaneous power because they are products of mutually perpendicular instantaneous voltages and currents. Consequently, the instantaneous power $p$ is designated as 'instantaneous real power' to avoid confusion with the 'instantaneous imaginary power' $q$.

Re-arranging Equation 4.6 leads to:

$$
\begin{bmatrix}
  i_\alpha \\
  i_\beta
\end{bmatrix} =
\begin{bmatrix}
  e_\alpha & e_\beta \\
  -e_\beta & e_\alpha
\end{bmatrix}^{-1}
\begin{bmatrix}
  p \\
  q
\end{bmatrix}
\quad (4.7)
$$

The instantaneous currents comprise two components:

$$
\begin{bmatrix}
  i_\alpha \\
  i_\beta
\end{bmatrix} =
\begin{bmatrix}
  e_\alpha & e_\beta \\
  -e_\beta & e_\alpha
\end{bmatrix}^{-1}
\begin{bmatrix}
  p \\
  0
\end{bmatrix} +
\begin{bmatrix}
  e_\alpha & e_\beta \\
  -e_\beta & e_\alpha
\end{bmatrix}^{-1}
\begin{bmatrix}
  0 \\
  q
\end{bmatrix}
\quad (4.8)
$$

$$
= \begin{bmatrix}
  i_{\alpha p} \\
  i_{\beta p}
\end{bmatrix} +
\begin{bmatrix}
  i_{\alpha q} \\
  i_{\beta q}
\end{bmatrix}
$$
where

\[
i_{\alpha p} = \frac{e_{\alpha}}{e_{\alpha}^2 + e_{\beta}^2} \cdot p ; \quad i_{\alpha q} = \frac{-e_{\beta}}{e_{\alpha}^2 + e_{\beta}^2} \cdot q ;
\]

\[
i_{\beta p} = \frac{e_{\beta}}{e_{\alpha}^2 + e_{\beta}^2} \cdot p ; \quad i_{\beta q} = \frac{e_{\alpha}}{e_{\alpha}^2 + e_{\beta}^2} \cdot q
\]

and

\[
i_{\alpha p} = \alpha\text{-axis instantaneous active current}; \quad i_{\beta p} = \beta\text{-axis instantaneous active current}
\]

\[
i_{\alpha q} = \alpha\text{-axis instantaneous reactive current}; \quad i_{\beta q} = \beta\text{-axis instantaneous reactive current}
\]

If the instantaneous powers in the \( \alpha \) and \( \beta \) axes are \( p_\alpha \) and \( p_\beta \). They can be defined as:

\[
\begin{bmatrix}
p_\alpha \\
p_\beta
\end{bmatrix} = \begin{bmatrix}
e_{\alpha}i_{\alpha} \\
e_{\beta}i_{\beta}
\end{bmatrix} = \begin{bmatrix}
e_{\alpha}i_{\alpha p} \\
e_{\beta}i_{\beta p}
\end{bmatrix} + \begin{bmatrix}
e_{\alpha}i_{\alpha q} \\
e_{\beta}i_{\beta q}
\end{bmatrix}
\]

The instantaneous real power \( p \) is obtained by substituting Equation 4.8 into Equation 4.9 giving:

\[
p = p_\alpha + p_\beta
\]

\[
= \frac{e_{\alpha}^2}{e_{\alpha}^2 + e_{\beta}^2} \cdot p + \frac{e_{\beta}^2}{e_{\alpha}^2 + e_{\beta}^2} \cdot p
\]

Equation 4.10 contains no imaginary components (q), as these sum to zero during the manipulation. An alternative way of viewing this is to say that the instantaneous power consists of the instantaneous active power and the instantaneous reactive power that adds up to zero, or:

31
\[ p = e_\alpha i_{\alpha p} + e_\beta i_{\beta p} = p_{\alpha p} + p_{\beta p} \]  

\[ 0 = e_\alpha i_{\alpha q} + e_\beta i_{\beta q} = p_{\alpha q} + p_{\beta q} \]

where

\[ p_{\alpha p} \quad \text{and} \quad p_{\beta p} \]

\[ p_{\alpha q} \quad \text{and} \quad p_{\beta q} \]

\[ p_{\alpha p} = \alpha \text{-axis instantaneous active power} \]

\[ p_{\alpha q} = \alpha \text{-axis instantaneous reactive power} \]

\[ p_{\beta p} = \beta \text{-axis instantaneous active power} \]

\[ p_{\beta q} = \beta \text{-axis instantaneous reactive power} \]

By inspection of Equation 4.11 and Equation 4.12, it follows that:

a) The sum of the instantaneous powers \( p_{\alpha p} \) and \( p_{\beta p} \) is equal to the instantaneous real power in the three-phase circuit.

b) The sum of the instantaneous powers \( p_{\alpha q} \) and \( p_{\beta q} \) cancel and make no contribution to the instantaneous power flow from the source to the load.

In order to eliminate harmonics, the second term in Equation 4.8 must be artificially forced to zero. This can be achieved by injecting currents which are of the same magnitude but in anti-phase with the unwanted harmonics.

The actual compensation currents injected by the active filter are designated as \( i_{c\alpha}, i_{c\beta} \) and \( i_{c\gamma} \).
while the reference compensation currents as calculated by the theory are designated as $i^*_{c_a}$, $i^*_{c_b}$ and $i^*_{c_c}$. From Equation 4.7, these currents in $\alpha-\beta$ coordinates are:

$$\begin{bmatrix}
i^*_{c_a} \\
i^*_{c_b}
\end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\
-e_\beta & e_\alpha \end{bmatrix}^{-1} \begin{bmatrix} 0 \\
-q \end{bmatrix}$$

which may be transformed into a-b-c coordinates:

$$\begin{bmatrix}
i^*_{c_a} \\
i^*_{c_b} \\
i^*_{c_c}
\end{bmatrix} = \begin{bmatrix} 2 \\
\frac{-1}{\sqrt{6}} \\
\frac{-1}{\sqrt{6}} \end{bmatrix} \begin{bmatrix} 0 \\
\frac{1}{\sqrt{2}} \\
\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i^*_{c_a} \\
i^*_{c_b} \\
i^*_{c_c}
\end{bmatrix}$$

The equations which determine the compensation currents are Equations 4.1, 4.2, 4.5, 4.13 and 4.14, and the procedure for determining them is given in Section 4.2.1. The next section describes the control strategy that was employed, to utilise the instantaneous reactive power equations in the proposed active power filter scheme.

### 4.2 PROPOSED COMPUTATION STRATEGY

The task is to determine the reference compensation currents ($i^*_{c_a}$, $i^*_{c_b}$ and $i^*_{c_c}$), using the distorted phase voltages ($e_a$, $e_b$ and $e_c$) and phase currents ($i_a$, $i_b$ and $i_c$), as shown in the general arrangement of the control system of Figure 4.3.

In order to operate the voltage-source PWM converter in a self-sufficient manner, it is important to take into account the d.c. voltage of the converter, so that it can be maintained.
at a suitable level by the three-phase rectifier circuit that supplies the d.c. voltage required by the capacitor.

The currents \( i_{\text{ca}}^*, i_{\text{cb}}^* \) and \( i_{\text{cc}}^* \) have to be computed very rapidly, to enable the PWM converter to reproduce them in real time. Since the overall circuit response time due to device propagation delays is not controllable, it is important to optimise the control strategy so as to minimise the computation time that is required.

Having calculated the required currents, their reference signals are supplied to the PWM current controller, which controls the switching operation of the converter to modulate the actual compensation currents \( i_{\text{ca}}, i_{\text{cb}} \) and \( i_{\text{cc}} \). Chapter 6 elaborates further on the hardware implementation side of the control strategy.

The \( \alpha-\beta \) computation approach derived in Section 4.1, will be compared with the phase component method proposed. Since the former is obtained through substitution and algebraic manipulation of the latter, as shown in Appendix 3, they should yield identical results. The main difference between the two methods is the mathematical complexity involved, which is directly linked to the computation time for the calculation.

### 4.2.1 \( \alpha-\beta \) COMPONENT METHOD

The \( \alpha-\beta \) component approach (method A) uses Equations 4.1, 4.2, 4.5, 4.13 and 4.14 defined earlier. The three-phase voltages \( e_a, e_b \) and \( e_c \) are transformed into two-phase voltages \( e_{\alpha} \) and \( e_{\beta} \) using Equation 4.1. Similarly, the three-phase currents \( i_a, i_b \) and \( i_c \) are transformed into two-phase currents \( i_{\alpha} \) and \( i_{\beta} \) using Equation 4.2.

These transformations are necessary since Equations 4.5 and 4.13 employ two-phase voltages and currents. The actual instantaneous reactive power is calculated using Equation 4.5, and
from this the two-phase compensation currents \( i_{C_a}^* \) and \( i_{C_B}^* \) are calculated by means of Equation 4.13. The three-phase compensation currents \( i_{C_a}^* \), \( i_{C_b}^* \) and \( i_{C_c}^* \) are obtained from the two-phase values using Equation 4.14.

In this method, a total of 26 mathematical operations are necessary to determine the desired compensation currents. Two of these operations are fractional division, which has a longer execution time than other mathematical operations. Although the mathematical processing is performed at very high speed using a digital signal processor (DSP), reducing the number of mathematical operations, particularly fractional division, can improve the overall compensation rate of the active filter.

Figure 4.4 shows a schematic representation of the control strategy using an \( \alpha-\beta \) component approach. Prototype active power filter schemes, based on instantaneous reactive power theory [21], [26]-[30] utilise analogue multipliers, proportional-integral controllers, etc, to compute the equations, with d.c. link voltage monitoring units. These schemes sometimes incorporate multiple voltage-source PWM converters, to provide an overall high current rating, even though the rating of each converter is relatively low.

4.2.2 PHASE COMPONENT METHOD

This approach (method B) requires only four equations to produce the required compensation currents \( i_{C_a}^* \), \( i_{C_b}^* \) and \( i_{C_c}^* \), as opposed to the five equations involved in the \( \alpha-\beta \) component method. The same input variables are used, i.e. the phase voltages \( e_a \), \( e_b \) and \( e_c \) and corresponding currents \( i_a \), \( i_b \) and \( i_c \) are obtained from the distorted a.c. supply.

The phase equations are derived by manipulation of Equations 4.1, 4.2, 4.5, 4.13 and 4.14, as given in Appendix 3. It is apparent from the equations that no transformations are necessary, since by performing the calculations using three-phase phase values, redundant
Intermediate components are avoided.

\[
M = \left[ \frac{i_a(e_c - e_a) + i_b(e_a - e_b) + i_c(e_b - e_a)}{(e_a - e_b)^2 + (e_b - e_c)^2 + (e_c - e_a)^2} \right] \tag{4.15}
\]

\[
i_{c_a}^* = (e_b - e_a)M \tag{4.16}
\]

\[
i_{c_b}^* = (e_c - e_a)M \tag{4.17}
\]

\[
i_{c_c}^* = (e_a - e_b)M \tag{4.18}
\]

In Equation 4.15 the phase voltages \( e_a, e_b \) and \( e_c \) and phase currents \( i_a, i_b \) and \( i_c \) are assembled to form the multiplier \( M \). All the three desired compensation current values \( i_{c_a}^*, i_{c_b}^*, \) and \( i_{c_c}^* \) can be determined by multiplication of \( M \) with the specific line voltage.

These equations are much simpler than the \( \alpha-\beta \) equations, with only 17 mathematical operations being needed. Only one fractional division operation is involved in the new method, compared to two in the \( \alpha-\beta \) method, and theoretically, the calculation time is reduced by about 35%.

Figure 4.5 shows the proposed control strategy for the phase component approach. The d.c. link voltage of the voltage-source PWM converter is maintained at a given operating voltage by an external circuit supplying a constant d.c. voltage to the capacitor (refer to Chapter 6 for a detailed explanation).
Figure 4.1: The $\alpha$-$\beta$ coordinate transformation

Figure 4.2: Instantaneous $\alpha$-$\beta$ space vectors
Figure 4.3: General arrangement of the proposed control strategy
Figure 4.4: Schematic of the α-β component (method A) control strategy

Figure 4.5: Schematic of the phase component (method B) control strategy
5.1 THEORETICAL SYSTEMS

Two mathematical models were developed to analyse the theoretical performance of the proposed active power filter scheme. The first of these is for the three-phase rectifier that generates harmonic voltages and currents in the power system, while the second comprises the active power filter that suppresses the harmonics produced by the rectifier. Simulations obtained from the two models used together will predict how a system behaves in practice.

5.2 RECTIFIER MODEL

The system considered is shown in Figure 5.1, with a three-phase delta-star transformer supplying a three-phase diode bridge rectifier connected to a resistive load. The supply voltage is assumed to be sinusoidal, so that any harmonics produced are a result of the static power conversion.

The modelling technique uses tensor transformations [32] to assemble the relevant mesh differential equations that describes the system, taking into account changes in the rectifier conduction pattern. The equations are integrated numerically, to obtain the time variation of the mesh currents, with the corresponding branch currents and voltages being determined by further tensor transformation. This technique, which is discussed below, requires the definition of both branch and mesh reference frames and a transformation between them.
5.2.1 BRANCH REFERENCE FRAME

The branch reference frame may be visualised as the circuit shown in Figure 5.2, with the various branch currents and voltages being related by a matrix equation given in abbreviated form as:

\[
\begin{bmatrix} E_b \\ V_b \end{bmatrix} = \begin{bmatrix} Z_b \end{bmatrix} \begin{bmatrix} I_b \end{bmatrix} \quad (5.1)
\]

where

\[
\begin{aligned}
E_b &= \text{Impressed branch voltage vector} \\
V_b &= \text{Branch voltage vector} \\
I_b &= \text{Branch current vector} \\
Z_b &= \text{Branch impedance vector}
\end{aligned}
\]

Equation 5.1 may be expressed in the expanded form

\[
\begin{bmatrix} E_b \\ V_b \end{bmatrix} = \begin{bmatrix} R_b \\ G_b \end{bmatrix} \begin{bmatrix} I_b \end{bmatrix} + \begin{bmatrix} L_b \end{bmatrix} p \begin{bmatrix} I_b \end{bmatrix} \quad (5.2)
\]

with the elements of the equation defined in the list of symbols. Since none of the inductances are time-varying \([ G_b ] = 0\), and

\[
\begin{bmatrix} E_b \\ V_b \end{bmatrix} = \begin{bmatrix} R_b \\ L_b \end{bmatrix} \begin{bmatrix} I_b \end{bmatrix} + \begin{bmatrix} L_b \end{bmatrix} p \begin{bmatrix} I_b \end{bmatrix} \quad (5.3)
\]

The branch reference frame equation is given in full in Equation 5.4 overleaf.
\[
\begin{bmatrix}
E_1 V_1 & R_1^+ p L_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_1 \\
E_2 V_2 & 0 & R_2^+ p L_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_2 \\
E_3 V_3 & 0 & 0 & R_3^+ p L_3 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_3 \\
V_1 & 0 & 0 & 0 & R_1^+ p L_4 & R_2^+ M_{45} & R_3^+ M_{46} & R_4^+ M_{47} & R_5^+ M_{48} & R_6^+ M_{49} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_4 \\
V_3 & 0 & 0 & 0 & R_1^+ M_{25} & R_2^+ M_{26} & R_3^+ M_{27} & R_4^+ M_{28} & R_5^+ M_{29} & R_6^+ M_{30} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_5 \\
V_5 & 0 & 0 & 0 & R_1^+ M_{15} & R_2^+ M_{16} & R_3^+ M_{17} & R_4^+ M_{18} & R_5^+ M_{19} & R_6^+ M_{20} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_6 \\
V_6 & 0 & 0 & 0 & R_1^+ M_{15} & R_2^+ M_{16} & R_3^+ M_{17} & R_4^+ M_{18} & R_5^+ M_{19} & R_6^+ M_{20} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_7 \\
V_7 & 0 & 0 & 0 & R_1^+ M_{15} & R_2^+ M_{16} & R_3^+ M_{17} & R_4^+ M_{18} & R_5^+ M_{19} & R_6^+ M_{20} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_8 \\
V_8 & 0 & 0 & 0 & R_1^+ M_{15} & R_2^+ M_{16} & R_3^+ M_{17} & R_4^+ M_{18} & R_5^+ M_{19} & R_6^+ M_{20} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_9 \\
V_9 & 0 & 0 & 0 & R_1^+ M_{15} & R_2^+ M_{16} & R_3^+ M_{17} & R_4^+ M_{18} & R_5^+ M_{19} & R_6^+ M_{20} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{10} \\
V_{10} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{12} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{11} \\
V_{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{12} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{12} \\
V_{12} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{13} \\
V_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{14} \\
V_{14} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{15} \\
V_{15} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{16} \\
V_{16} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{11}^+ p L_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & I_{17} \\
\end{bmatrix}
\]

(5.4)
5.2.2 MESH REFERENCE FRAME

The mesh reference frame is concerned with the meshes formed when the conducting diodes connect the supply to the load. It may be developed using linear oriented graphs, in which lines denote branches, dots denote circuit nodes and arrows show the direction of the positive branch currents.

Figure 5.3 is the linear oriented graph for the impractical situation when all six diodes conduct simultaneously. The directions of the branch currents are arbitrary, but the choice of forward diode currents as the direction of positive branch currents simplifies the solution process.

Figures 5.4, 5.5 and 5.6 are linear oriented graphs before, during and after a typical commutation, which produce 11, 13 and 11 conducting branches respectively. Before commutation, diodes D6 and D1 are conducting. During commutation, diode D2 becomes forward-biased causing diodes D6, D1 and D2 to conduct simultaneously. After commutation, diodes D1 and D2 are conducting, since diode D6 ceases to conduct due to its current reducing to zero.

From topological considerations, the total number of independent mesh equations $M$ is given by:

$$ M = B - N + S \quad (5.5) $$

where $B$ = Number of system branches

$N$ = Number of nodes

$S$ = Number of independent circuits i.e. not electrically connected

From Figure 5.4, 5.5 and 5.6, it is clear that the number of meshes varies between:

$$ M_{\text{min}} = 11 - 9 + 2 = 4 $$

and

$$ M_{\text{max}} = 13 - 10 + 2 = 5 $$

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The abbreviated form of the matrix equation relating the mesh currents and voltages is:

\[ [E_m] + [V_m] = [Z_m][I_m] \]  \hspace{1cm} (5.6)

where the elements of the equations are defined in the list of symbols. Expanding Equation 5.6 gives:

\[ [E_m] + [V_m] = [R_m + G_m][I_m] + [L_m]p[I_m] \]  \hspace{1cm} (5.7)

Since the inductances are constant \( G_m = 0 \) and Equation 5.7 may be re-written:

\[ [E_m] + [V_m] = [R_m][I_m] + [L_m]p[I_m] \]  \hspace{1cm} (5.8)

and then re-arranged as:

\[ p[I_m] = [L_m]^{-1} \{ [E_m] + [V_m] - [R_m][I_m] \} \]  \hspace{1cm} (5.9)

which is suitable for numerical integration, to obtain the mesh current vector.

5.2.3 BRANCH-MESH TRANSFORMATION

The relationship between branch and mesh currents may be obtained by inspection of the linear oriented graph. Consider the situations with diodes D6 and D1 conducting, and with diodes D6, D1 and D2 conducting, as shown respectively in Figures 5.4 and 5.5. The relationships between the branch and mesh currents are given in Figures 5.7 and 5.8, which
may be written in the abbreviated form:

\[ I_b = [C_{bn}]I_m \]  \hspace{1cm} (5.10)

The transformation matrix \([C_{bn}]\) clearly varies with the conduction pattern in the diode bridge. The first three columns are fixed, while the subsequent columns adapt to the rectifier conduction pattern, which is available from the rectifier device conduction matrix \([C_R]\), as explained in Section 5.2.4.

An important criterion for tensor analysis is the power invariance that must exist between reference frames, which can be expressed mathematically as:

\[ \left[ V_b + E_b \right]^t I_b = \left[ V_m + E_m \right]^t I_m \]  \hspace{1cm} (5.11)

where the superscript \(t\) denotes the transpose of the matrix. Substituting for Equation 5.10 in Equation 5.11 and re-arranging gives:

\[ \left[ V_b + E_b \right]^t [C_{bn}]I_m = \left[ V_m + E_m \right]^t I_m \]  \hspace{1cm} (5.12)

From the properties of matrices,

\[ [C_{bn}]^t [V_b] + [C_{bn}]^t [E_b] = [V_m + E_m] \]  \hspace{1cm} (5.13)

If Equation 5.13 holds true for any arbitrary \([I_m]\), the voltage sources and voltage drops in the two reference frames may be defined as:
\[ \mathbf{E}_m = [\mathbf{C}_{bm}]^t \mathbf{E}_b \]  
\[
\mathbf{V}_m = [\mathbf{C}_{bm}]^t \mathbf{V}_b 
\]

Since the voltages around a closed mesh sum to zero i.e. Kirchhoff's voltage law \( \mathbf{V}_m = 0 \).
[
\mathbf{C}_{bm}]

is termed the branch/mesh voltage transformation matrix, and it may also be
determined by inspection of the linear oriented graph.

Substituting Equations 5.10 and 5.14 into Equation 5.1 gives:

\[ \mathbf{E}_m = [\mathbf{C}_{bm}]^t \mathbf{Z}_b [\mathbf{C}_{bm}] \mathbf{I}_m \]  
\[
\text{and comparing Equations 5.6 and 5.16 reveals that:}
\]

\[ \mathbf{Z}_m = [\mathbf{C}_{bm}]^t \mathbf{Z}_b [\mathbf{C}_{bm}] \]

which defines the branch/mesh impedance transformation.

If the analysis above is extended further, it can be shown that the mesh resistance and
inductance matrices are related to their branch counterparts by:

\[ \mathbf{R}_m = [\mathbf{C}_{bm}]^t \mathbf{R}_b [\mathbf{C}_{bm}] \]  
\[
\mathbf{L}_m = [\mathbf{C}_{bm}]^t \mathbf{L}_b [\mathbf{C}_{bm}] \]
5.2.4 CONDUCTION PATTERN TABLE

A look-up table \([ C_R ]\) containing all possible diode conduction patterns is given in Figure 5.9. Each column of \([ C_R ]\) contains the conduction states of all the branches in the system, where '1' indicates a positive branch current, '-1' a negative branch current and '0' zero branch current.

When the rectifier topology changes, due to diodes turning-on or turning off, the columns of matrix \([ C_R ]\) are searched, to find the matching pattern to be loaded into the variable columns of the transformation matrix \([ C_{bm} ]\).

5.2.5 CURRENT DISCONTINUITY

A current discontinuity occurs whenever a conducting diode attempts to pass reverse current, and it is detected using a negative current test. Before commutation, the system is represented by the four meshes shown in Figure 5.10. However, during a commutation interval, the five meshes shown in Figure 5.11 are required. These comprise the previous four meshes and an additional one \((e)\) formed by the load and branch 7, due to the conduction of diode D2. After the commutation process, the system is represented by the four new meshes shown in Figure 5.12.

During commutation, the incoming mesh current \(I_e\) builds up, while the outgoing mesh current \(I_d\) decreases. At the end of each integration step, the load mesh currents are tested for their polarity. If a current discontinuity has occurred during the step, a negative mesh current will be detected.

Figure 5.13 shows the method for determining the point of discontinuity using linear interpolation, where the time to the discontinuity is:
\[ t_d = \frac{i_{to} \cdot h}{i_{to} - i_{tl}} \tag{5.20} \]

in which \( i_{to} \) is the current at the previous integration step, \( i_t \) is the current at the present integration step and \( h \) is the integration step length.

### 5.2.6 VOLTAGE DISCONTINUITY

A voltage discontinuity occurs whenever a non-conducting diode becomes forward-biased and commences conduction. Diode turn-on is detected by monitoring the line voltages on the a.c. side of the three-phase rectifier, and testing the bias conditions of the diodes.

The procedure begins by selecting the load voltage level as the reference value. At the end of every integration step, the six permutations of the line voltages are determined and are compared with the reference. If any of these values is equal to or exceeds the reference, a voltage discontinuity is encountered, and the forward-biased diodes are included in the new conducting pattern.

### 5.2.7 COMPUTER IMPLEMENTATION

A computer program was written in Prospero Fortran-77 V2.1 to predict the performance of the rectifier. A flow chart for this program is given in Figure 5.14.

The algorithm for the solution process is :

1. Define the branch resistance \([ R_b ]\) and inductance \([ L_b ]\) matrices, and the rectifier device conduction \([ C_R ]\) matrix, which remain unchanged throughout the simulation.
b) Determine any discontinuity, and search the columns of matrix \([ C_R ]\) for a matching conduction pattern.

c) Determine the branch/mesh current transformation \([ C_{bm} ]\) and its transpose \([ C_{bm} ]^t\).

d) Determine the mesh resistance \([ R_m ]\) and inductance \([ L_m ]\) matrices, and invert \([ L_m ]\).

e) Integrate Equation 5.9 to obtain the mesh current matrix \([ I_m ]\).

f) Determine the branch current vector \([ I_b ]\) using Equation 5.10 and the branch voltage vector \([ V_b ]\) from:

\[
[V_b] = [R_b][I_b] + [L_b] P[I_b] \quad (5.21)
\]

The solution advances on a step-by-step basis, every time operations (a) to (f) are implemented. At the end of every step, the system is tested for any changes in the rectifier conduction pattern, as explained in Sections 5.2.5 and 5.2.6.

5.3 RECTIFIER-FILTER MODEL

Figure 5.15 shows a schematic diagram for the complete system investigated, comprising a three-phase transformer/rectifier connected to an resistive load, and a three-phase PWM converter connected to the a.c. supply. As before, the supply voltage is assumed to be sinusoidal.

Since the definitions of both branch and mesh reference frames and their transformation are similar to those of the previous model, the discussion below will explain only the new aspects of this enhanced model.
5.3.1 BRANCH REFERENCE FRAME

The branch reference frame is shown in Figure 5.16, and the relationships between the various branch currents and voltages is:

\[ [E_b] + [V_b] = [R_b][I_b] + [L_b]p[I_b] \]  \hspace{1cm} (5.22)

The branch reference frame equation is given in full in Equation 5.23.

5.3.2 MESH REFERENCE FRAME

Figure 5.17 shows the linear oriented graph for the impractical situation when all the devices in the rectifier and converter are conducting simultaneously, with the forward device currents chosen to be the positive branch currents.

Figures 5.18, 5.19 and 5.20 show linear oriented graphs before, during and after rectifier commutation, producing respectively 18, 20 and 18 conducting branches. As in the previous model, rectifier diodes D6 and D1 conduct before commutation, and diodes D6, D1 and D2 during commutation. Diodes D1 and D2 conduct after commutation.

Since the converter has a bi-directional current flow, three devices always conduct simultaneously, for example D3, S4\(^*\) and S5 in Figures 5.18, 5.19 and 5.20. Using these diagrams, it is obvious that the number of meshes varies between:

\[ M_{\text{min}} = 18 - 14 + 2 = 6 \]

and

\[ M_{\text{max}} = 20 - 15 + 2 = 7 \]

The system mesh equation may be expressed as:

* Throughout the thesis devices identified by an upper case S are unidirectional power switches.
\[
[E_m] = [R_m][I_m] + [L_m]p[I_m]
\]

which may be re-arranged in the form suitable for numerical integration:

\[
p[I_m] = [L_m]^{-1} \{[E_m] - [R_m][I_m]\}
\]

### 5.3.3 BRANCH-MESH TRANSFORMATION

The branch/mesh transformations developed in Section 5.2.3 still hold true, and is therefore valid for the present model. The current transformation matrices \([C_{bm}]\) for the conditions shown in Figures 5.18 and 5.19 are given in Figures 5.21 and 5.22, and represent respectively the situation before and during rectifier commutation. As before, the transformation matrix varies with the number of system meshes, which is accounted for by changing the number of columns and device conduction states in the matrix appropriately.

The first three columns of \([C_{bm}]\) are fixed, while the fourth and fifth columns (shown in bold) are variable in size and content to adapt to the rectifier conduction pattern. However, columns six and seven (bold and italic) are fixed in size but their contents vary to cater for the converter conduction pattern. These patterns are available from the rectifier and converter device conduction matrices \([C_R]\) and \([C_C]\) respectively, as explained in Section 5.3.4.

Only one mesh current circulates in the rectifier before commutation. This produces six current meshes and, consequently, the six columns in \([C_{bm}]\) in Figure 5.21. The sixth and seventh columns are left-shifted accordingly to accommodate the absence of the second rectifier mesh current. Since two mesh currents are circulating in the rectifier during commutation, all seven mesh currents are available, which is represented by the seven associated columns in \([C_{bm}]\) in Figure 5.22.
5.3.4 CONDUCTION PATTERN TABLES

When the rectifier or converter topologies change, the columns of the matrices \([ C_R ]\) and \([ C_C ]\) are searched, to determine the matching pattern to be loaded into the relevant variable columns in the transformation matrix \([ C_{bm} ]\).

As in the previous model (Section 5.2.4), the look-up table containing all possible combinations for the rectifier diode conduction pattern (see Figure 5.9) was used, and defined as the rectifier conduction pattern matrix \([ C_R ]\). Similarly, a look-up table containing all possible combinations for the converter device conduction pattern was established as in Figure 5.23, which is defined as the converter conduction pattern matrix \([ C_C ]\).

5.3.5 DISCONTINUITIES

A current discontinuity in the rectifier occurs whenever a conducting diode attempts to pass reverse current, and is detected by the negative current test explained in Section 5.2.5. A voltage discontinuity occurs due to the diodes becoming forward-biased, and is detected, as explained in Section 5.2.6. Figures 5.24, 5.25 and 5.26 show the system mesh currents before, during and after rectifier commutation.

Unlike the rectifier, the converter current flow is bi-directional, because each half of each legs consists of a power switch and an inverse-parallel diode. Consequently, the converter has three devices conducting simultaneously, forming two independent meshes. Both current and voltage discontinuities in the converter are determined by the PWM current controller, depending on the condition.

A current discontinuity occurs whenever the output current deviates from the reference current by more than the hysteresis-band of the carrier signal, when the converter operates in the
inverter mode. These reference currents are computed using Equations 4.15 to 4.18. A voltage discontinuity occurs whenever the d.c. link voltage drops below the threshold level, and the converter is operated as a rectifier to restore the capacitor charge.

The closed-loop current control scheme compares the differences between the reference and feedback currents with an 8 kHz triangular carrier signal, and switches the devices in the top and bottom halves of the converter legs when the magnitude of the current differences exceed the instantaneous magnitude of the triangular signal.

The triangular waveform imposes a fixed frequency pseudo-band on the reference currents, so that the converter currents can be modulated within it. After each integration step, the converter output currents are tested for any discontinuities, and if necessary a new conduction pattern is formed to maintain the currents close to the reference currents.

5.3.6 COMPUTER IMPLEMENTATION

Figure 5.27 is a flow chart of a computer program written to predict the performance of the system.

The algorithm for the solution process is:

a) Define the branch resistance \( R_b \) and inductance \( L_b \) matrices.

b) Define the rectifier \( C_r \) conduction matrix

c) Determine the required compensation currents using the proposed instantaneous reactive power equations and define the converter \( C_c \) device conduction matrix.
c) Determine any discontinuity in the rectifier and converter, and search the columns of matrices \( C_R \) and \( C_C \) respectively for matching conduction patterns.

d) Determine the branch/mesh current transformation \( C_{bm} \) and its transpose \( C_{bm}' \).

e) Determine the mesh resistance \( R_m \) and inductance \( L_m \) matrices, and invert \( L_m \).

f) Integrate Equation 5.25 to obtain the mesh current matrix \( I_m \).

g) Determine the branch current vector \( I_b \) using Equation 5.12 and the branch voltage vector \( V_b \) from:

\[
[V_b] = [R_b][I_b] + [L_b] p[I_b]
\]  \( (5.26) \)

The solution advances by one step, each time operations (a) to (g) are implemented. At the end of every step, the system is tested for any changes in the rectifier and converter topologies. These discontinuities occur when the conduction pattern in either the rectifier or the converter changes its state, as explained in Section 5.3.5.

5.4 FOURIER WAVEFORM ANALYSIS PROGRAM

A computer program was written in Turbo Pascal 6.0 to extract harmonic components from the waveform data files obtained through the simulations. The flow chart for this program is given in Figure 5.28.
5.5 SIMULATIONS

The system equations for both models were assembled using the tensor methods described earlier, and solved by using the conventional fourth-order Runge-Kutta numerical integration method (Appendix 4). Consequently, the simulations were performed by executing the computer programs mentioned in Sections 5.2.7 and 5.3.6, using the system parameters given in Appendix 5.

Only method B was implemented in the rectifier-filter model because the computation accuracy of the reference compensation currents during the simulation is not method dependant, with the absence of the DSP computation and control circuits propagation delays. These delays were neglected from the simulation due to unnecessary complexity involved in modelling them reliably.

The simulation results obtained are presented later in Chapter 8, together with the relevant experimental results, to enable relative performance comparison to be made and to confirm the validity of the two mathematical models developed.
Figure 5.2: Branch reference frame equivalent circuit for the rectifier model
Figure 5.3: Linear oriented graph with all diodes conducting (rectifier model)
Figure 5.4: Linear oriented graph before commutation (rectifier model)
Figure 5.5: Linear oriented graph during commutation (rectifier model)
Figure 5.6: Linear oriented graph after commutation (rectifier model)
\[ \begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4 \\
I_5 \\
I_6 \\
I_7 \\
I_8 \\
I_9 \\
I_{10} \\
I_{11} \\
I_{12} \\
I_{13} \\
I_{14} \\
I_{15} \\
I_{16}
\end{bmatrix} =
\begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
-1 & -1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
-1 & -1 & 1 & 0 \\
-1 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1 \\
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 1
\end{bmatrix} \begin{bmatrix}
I_a \\
I_b \\
I_c \\
I_d
\end{bmatrix} \]

Figure 5.7: Branch-mesh current relationship before commutation (see Figure 5.10).
Figure 5.8: Branch-mesh current relationship during commutation (see Figure 5.11).
<table>
<thead>
<tr>
<th>Devices</th>
<th>( D_1 )</th>
<th>( D_2 )</th>
<th>( D_3 )</th>
<th>( D_4 )</th>
<th>( D_5 )</th>
<th>( D_6 )</th>
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<td>-1</td>
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</tr>
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Figure 5.9: Device conduction pattern for matrix \([ C_R ]\)
Figure 5.10: Mesh representation of the system before commutation (rectifier model). See Figure 5.7.
Figure 5.11: Mesh representation of the system during commutation (rectifier model). See Figure 5.8.
Figure 5.12: Mesh representation of the system after commutation (rectifier model)
Figure 5.13: The time to a current discontinuity
Figure 5.14: Flow chart for rectifier simulation program
Figure 5.15: Schematic diagram for the rectifier-filter model
Figure 5.16: Branch reference frame equivalent circuit for the rectifier-filter model
Figure 5.17: Linear oriented graph with all devices conducting (rectifier-filter model)
Figure 5.18: Linear oriented graph before commutation (rectifier-filter model)
Figure 5.19: Linear oriented graph during commutation (rectifier-filter model)
Figure 5.21: Branch-mesh current relationship before commutation (rectifier-filter model)
\[
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4 \\
I_5 \\
I_6 \\
I_7 \\
I_8 \\
I_9 \\
I_{10} \\
I_{11} \\
I_{12} \\
I_{13} \\
I_{14} \\
I_{15} \\
I_{16} \\
I_{17} \\
I_{18} \\
I_{19} \\
I_{20} \\
I_{21} \\
I_{22} \\
I_{23} \\
I_{24} \\
I_{25} \\
I_{26} \\
I_{27} \\
I_{28} \\
I_{29} \\
I_{30} \\
I_{31} \\
I_{32}
\end{bmatrix}
= 
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & -1 & -1 \\
0 & 1 & 0 & 0 & 0 & 1 & 0 \\
-1 & -1 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 \\
-1 & -1 & 1 & 0 & 0 & 0 & 0 \\
-1 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
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0 & 0 & 0 & 0 & 0 & 0 & 1 \\
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0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_a \\
I_b \\
I_c \\
I_d \\
I_e \\
I_f \\
I_g
\end{bmatrix}
\]

**Figure 5.22**: Branch-mesh current relationship during commutation (rectifier-filter model)
<table>
<thead>
<tr>
<th>Devices</th>
<th>Inversion</th>
<th>Free-wheeling</th>
<th>Rectification</th>
</tr>
</thead>
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<tr>
<td></td>
<td>S1 S2 S3 S4 S5 S6</td>
<td>D3 D4 D5 D6 D1 D2 S3 S4 S5</td>
<td>D1 D2 D3 D4 D5 D6</td>
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<td>b1</td>
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<td>-1 -1 0 1 1 0</td>
<td>-1 1 0 -1 -1 0</td>
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<tr>
<td>b2</td>
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<td>1 0 -1 -1 0 1</td>
<td>-1 0 1 1 0 -1</td>
</tr>
<tr>
<td>b3</td>
<td>0 1 1 0 -1 -1</td>
<td>0 .1 1 0 -1 -1</td>
<td>0 -1 -1 0 1 1</td>
</tr>
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<td>b12</td>
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<td>1 1 0 -1 -1 0</td>
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<td>0 0 0 0 0 0</td>
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<td>b21</td>
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<tr>
<td>b32</td>
<td>1 1 1 1 1 1</td>
<td>0 0 0 0 0 0</td>
<td>-1 -1 -1 -1 -1 -1</td>
</tr>
</tbody>
</table>

Figure 5.23: Device conduction pattern for matrix \([ C_c ]\)
Figure 5.24: Mesh representation of the system before rectifier commutation (rectifier-filter model)
Figure 5.25: Mesh representation of the system during rectifier commutation (rectifier-filter model)
Figure 5.26: Mesh representation of the system after rectifier commutation (rectifier-filter model)
Figure 5.27: Flow chart for rectifier-active filter simulation program
Figur4 5.28: Flow chart for Fourier analysis program
Figure 6.1 is a schematic diagram showing the functional circuit blocks of the experimental system. In general, the three-phase a.c. supply feeds the harmonic source, while the active filtering scheme, consisting of a monitoring circuit, DSP, PWM current controller and PWM converter, is connected in parallel with it.

During operation, the distorted supply produced by the harmonic source is sampled by the monitoring circuit. These instantaneous values are digitised and then supplied to the DSP for calculation, using the equations in Chapter 4. When the computation is complete, the reference compensation current signals are supplied to the PWM current controller, to control the output currents of the PWM converter, as closely as possible to the required compensation currents.

The harmonic source composed of a three-phase delta-star connected transformer supplying a three-phase full-wave rectifier connected to a resistive load, as shown in Figure 6.2. The distorted currents from the supply produce corresponding distortion in the line voltages.

The schematic of Figure 6.3 incorporates both the current and voltage monitoring circuits. These circuits monitor the amplitude and polarity of both the phase currents and line voltages of the distorted supply, and are made up of the necessary sensing circuits with their individual low-pass filters and analogue-to-digital circuits.

Figure 6.4 gives an overview of the DSP functional block, which consists of an input/output interface circuit and a TMS320C50X DSK module. Chapter 7 will discuss this block in depth, including the computer program required to perform the necessary calculation.

The current controller of Figure 6.5 was implemented to control the PWM converter. The
DAC receives the digital reference signals directly from the DSP, and converts these into the equivalent analogue signals, while the current controller uses feedback current signals from the PWM converter to ensure that the currents remain within the operating band.

Figure 6.6 shows the functional blocks of the PWM converter, incorporating a three-phase delta-star connected transformer, three-phase full-wave rectifier, d.c. link, crowbar protection circuit, voltage-source converter, snubber network and synchronous link. The three-phase supply from the unfiltered side is fed to the transformer supplying the rectifier, to maintain a stable d.c. link voltage for self-sufficient operation of the voltage-source converter.

A crowbar protection circuit is utilised for protection against overcurrent on the d.c. side of the converter. Further protection is provided by the snubber network, which prevents excessive electrical stress on the power devices, particularly during prolonged high speed operation. The synchronous link provides suppression of the switching frequency harmonics, and it is also vital for operating the converter in the inverter mode.

When operating as a full-time inverter, the converter generates compensation currents, as determined by the DSP and controlled by the PWM current controller. These are then injected back to the supply to suppress the harmonics, and they are also utilised in the closed-loop current controller as feedback signals.

In the following sections, an explanation is given of the operation and the mechanisms involved in the individual circuit, particularly within the functional blocks shown.
6.1 POWER SUPPLIES

The power requirements for the stabilised power supplies and the isolated power supplies are met by the power supply circuits shown in Figure 6.7 and Figure 6.8. The range of voltage available are +5 V and ±15 V for the stabilised supplies; and +12 V and ±15 V for the isolated supplies.

With the exception of the DSP, which has an on-board power unit, most of the electronic circuits rely on these stabilised supplies. However, the converter drive circuit requires four isolated +12 V supplies, and the isolation amplifier of the voltage monitoring circuit needs isolated supplies of ±15 V.

6.2 THREE-PHASE TRANSFORMERS

Two delta-star connected three-phase transformers are required in the experimental system, one for each of the two bridge rectifiers.

6.3 THREE-PHASE RECTIFIERS

Two three-phase full-wave rectifiers were incorporated in the system, using diodes as the power switches (30 A, 600 V). The first rectifier provides the d.c. supply for the resistive (300 Ω, 2.5 mH) load, which is the main harmonic source.

The second rectifier maintains the converter d.c. link capacitor voltage constant, by charging it through a series inductor, and also acts as a secondary harmonic source. Since it is connected to a capacitive load, it produces considerably less harmonics than the first rectifier.
6.4 THREE-PHASE CONVERTER

The three-phase PWM voltage-source converter employs IRG4BC30F medium frequency IGBT (30 A, 600 V) as power switches, STTA3006PI (25 A, 600 V) as fast-recovery diodes, a snubber network (Section 6.12.1) and a d.c. capacitor (2000 µF, 415 V dc), and is fed by the second rectifier mentioned in Section 6.3. For switching operation, the converter employs an isolated gate drive circuit (Section 6.5) to control the IGBTs.

Figure 6.9 shows the converter circuit diagram, without the d.c. link but with the snubber network. To ensure that the circuit operates reliably, it is important that a constant d.c. voltage is continuously available at the d.c. link, and this is provided from a high voltage d.c. reservoir capacitor supplied by an external d.c. voltage source (Section 6.13).

When the required compensation currents have been computed and fed to the analogue-to-digital and current control circuits, the drive circuit generates the appropriate PWM reference signals, which then switch the IGBTs in the correct sequence to produce the required converter currents.

Since the converter currents will inevitably contain PWM switching frequencies harmonics, the converter itself may be regarded as a harmonic source. These harmonics are usually of high frequency but low amplitude, and they are relatively less detrimental than those produced by the main harmonic source. They can very effectively be minimised by means of suitable series inductors connected at the output of the converter.

6.5 ISOLATED GATE DRIVE CIRCUIT

The power circuit is at a high voltage and for safety purposes, it is vital that it is isolated from the low-voltage control circuit. This was provided by a 740L6010 high-speed optocoupler,
consisting of a photo-detector and an open-collector transistor output. The input and output of the optocoupler are electrically isolated, and the gate drive circuit diagram that is required is shown in Figure 6.10.

When the PWM switching signal from the hysteresis current controller is high ( +5 V ), the optocoupler conducts and its transistor is switched on. The current from the optocoupler transistor is amplified by the Darlington transistor pair, to drive the gate of the IGBT. The use of 12 V Zener diode is necessary to clamp the amplitude of the gate voltage, since if ringing or induced voltage spikes cause it to exceed 20 V, the device will be destroyed. The 33 Ω series gate resistor limits the transient overvoltage developed across the IGBT and its fast-recovery diode during turn-on, and also reduces unacceptable ringing during recovery [33].

6.6 SYNCHRONOUS LINK

During inverter operation, the converter voltage is made to lead the supply voltage, so that the resulting current becomes sufficiently in phase with the supply voltage. This is accomplished by using the synchronous link inductors.

As mentioned previously, the switching frequency harmonics generated by the PWM voltage-source converter need to be minimised, and this is achieved using a three-phase iron-cored inductor connected in series with the output of the PWM converter. It is designed to tune to the specified switching frequency. The calculation of the required inductance was obtained using Equation 6.1 [34], and is given below:

\[
\begin{align*}
\text{Given that,} & \quad \text{Converter switching frequency,} \quad f_i = 8 \text{ kHz} \\
& \quad \text{Amplitude of switching frequency,} \quad \xi = 0.2 \text{ V} \\
& \quad \text{Converter a.c. phase voltage,} \quad V_{an} = 115 \sqrt{2/\sqrt{3}} = 94 \text{ V} \\
& \quad \text{Converter d.c. voltage} \quad V_{dc} = 115 \sqrt{6} = 282 \text{ V}
\end{align*}
\]
Since,

\[ L_{\text{link}} = \frac{V_{an} + 0.5 V_{dc}}{4\xi f_t} \quad (6.1) \]

Thus,

\[ L_{\text{link}} = \frac{94 + 0.5 (282)}{4 (0.2) (8000)} \approx 37 \text{ mH} \]

6.7 **PWM CURRENT CONTROLLER**

In many aspects, a fixed-frequency current controller is similar to a conventional hysteresis current controller, and is sometimes used for PWM converters. It is relatively simple to implement and has a good dynamic and transient responses \([35,36]\). The main difference is that the switching frequency does not vary throughout the specified band, unlike the hysteresis controllers.

In addition to having a fast-response current loop and an inherent-peak current limiting capability, this controller does not require any information about the system parameters. Moreover, the fixed switching frequency enables the switching harmonics to be suppressed more easily.

The current controller, shown in Figure 6.11, controls the converter switches so as to produce converter currents close to the required compensation currents. Digital signals representing the required compensation current values are supplied by the DSP, where they are converted into equivalent analogue reference signals before being supplied through a 3 kHz low-pass filter (Section 6.14) to remove any high frequency noise resulting from DAC operation.

The currents produced at the converter output are sensed using HTP50 Hall-effect current
transducers, and are conditioned by the TL071 voltage follower and the d.c. offset adjustment circuit. The resulting signals provide the closed-loop feedback values of the actual currents.

The current feedback and compensation current reference signals are applied to the TL071 differential amplifiers to obtain the error values. These values are compared to the high frequency triangular reference waveform using LM311 comparators, and are fed to the a 74HCT00 Hex inverter to provide complementary outputs.

The fixed switching frequency of 8 kHz is provided by 0.2 V triangular waveform using a 555 timer and a TL071 voltage follower. In order to prevent shoot-through conditions in any of the converter legs, a blanking time of approximately 2 µs was introduced using delay circuits incorporating 74HCT08 AND gates.

6.8 DIGITAL-TO-ANALOGUE CONVERTER

A digital-to-analogue converter (DAC) is required to convert the DSP reference signals to analogue voltages. Despite the 16-bit data output capability of the DSP, a solution using a DAC312HP 12-bit high-speed DAC was adopted for economic reasons.

Figure 6.12 shows the circuit diagram of the conversion circuit. When the 12-bit digital reference signal from the DSP is supplied to the DAC chip, the analogue signal is reproduced at the output by a TL071 differential amplifier. Operating the DAC chip in the bipolar offset mode enables the 2's complement digital numbers from the DSP to be directly interfaced with the DAC.

The range of the DAC output is between -10 V to +10 V, which corresponds to an operating current range of -10 A to +10 A. Consequently, a true zero voltage (0 V) is produced when the digital number 0000H is supplied at the input. When the DAC receives an input of 0001H
it will produce a 4.8 mV signal to represent 4.8 mA. To compensate for the voltage offset in the TL071 differential amplifier, particularly at digital number 0000H, a multi-turn offset adjustment trimming resistor was included.

The first two reference signals are obtained using DACs, while the third signal is produced through an inverting TL071 summing amplifier. These three analogue signals are the demand currents that the current controller has to reproduce by appropriate PWM switching in the converter.

6.9 ANALOGUE-TO-DIGITAL CONVERTER

Computation of the compensation currents is based on analogue information of the supply line voltages and phase currents, and analogue-to-digital converters (ADCs) are needed to convert them into digital form. Two identical ADC circuits were incorporated in the design of the monitoring circuit.

Figure 6.13 shows the ADC circuit diagram, which is based on the 12-bit high-speed HI5812 ADC integrated circuit. It is designed to handle two analogue sources alternately, which is achieved using two DG303 analogue switches, one for the analogue magnitude and one for the sign signal.

The sign signal is digital because the LM311 comparator in the monitoring circuit uses a pull-up resistor tied to the +5 V supply. Each signal received from the source is latched into a 74HCT74 latching flip-flop, and when the appropriate control pulse is applied the signal from the present source is transferred to the circuit output via the analogue switch and a 74HCT125 tri-state buffer.

The magnitude waveform from the monitoring circuit is conditioned to have an absolute value
using a precision rectifier circuit [37], and when the control pulse is applied the signal is transferred to the ADC chip for the conversion process. The pulse controlling the analogue switches and the latching flip-flop is generated by the ADC chip data ready (DRDY) signal via a toggling 74HCT74 data flip-flop. The circuit output terminals are defined below:

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>DEFINITION</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D&lt;sub&gt;1&lt;/sub&gt; to D&lt;sub&gt;12&lt;/sub&gt;</td>
<td>12-bit data</td>
<td>Output</td>
</tr>
<tr>
<td>Q</td>
<td>Points to present analogue source</td>
<td>Output</td>
</tr>
<tr>
<td>SIGN</td>
<td>Present analogue waveform polarity</td>
<td>Output</td>
</tr>
<tr>
<td>/DRDY</td>
<td>Digital data ready to be read</td>
<td>Output</td>
</tr>
<tr>
<td>/OE</td>
<td>Enable data output from circuit</td>
<td>Input</td>
</tr>
</tbody>
</table>

6.10 CURRENT MONITORING CIRCUIT

Sensing the instantaneous phase currents of the distorted a.c. supply is performed by the circuit of Figure 6.14. Only two measurements are made and the third current is calculated by the DSP. Current detection is achieved using HEME Hall-effect current transducers, which produce voltage signals proportional to the current being sensed. In addition, the transducer provides isolation between the measuring circuit and the power circuit.

The voltage signal is conditioned using a TL071 voltage follower, before being fed to a TL071 differential amplifier with offset adjustment. Since this signal is alternating, a precision rectifier is used to provide the absolute value. The zero-crossing detecting circuit incorporating a LM311 comparator is included so that the sign of the rectified waveform can be determined.
The absolute value signals are supplied to the 5 kHz low-pass filter to remove the switching frequency noise, and are fed together with the sign signals to the ADC, where digitisation takes place, before they are read by the DSP.

6.11 VOLTAGE MONITORING CIRCUIT

The instantaneous line voltages of the a.c. supply are sensed by the circuit of Figure 6.15. Only two voltages are sensed and the third is computed by the DSP. Voltage detection is achieved using a set of delta connected resistors, with one phase grounded as a reference point, where potential dividers provide a scaled-down value of the two line voltages.

Each signal from the delta-connected circuit is applied to a ISO122P isolation amplifier via a TL071 voltage follower. A second TL071 voltage follower at the output of the isolation amplifier ensures that the voltage variation is within the operating range (±15 V). The precision rectifier circuit provides the absolute value of the waveform detected and the LM311 zero-crossing detecting circuit identifies the sign of the rectified waveform.

As with the current sensing circuit, the absolute value signals are supplied to a 5 kHz low-pass filter to remove the switching frequency noise, before being fed to the ADC, together with the sign signals, where digitisation takes place, before they are read by the DSP.

6.12 PROTECTION CIRCUITS

In order to protect the converter, a snubber network and a crowbar protection circuit were employed, and these are both discussed below.
6.12.1 SNUBBER NETWORK

Snubbers are used to protect semiconductor power switches from excessive current and voltage stresses, which might otherwise cause permanent damage [38]. In addition to the overvoltage snubber, both turn-off and turn-on snubber circuits were incorporated in the design of the converter shown in Figure 6.9.

Overvoltage snubbers minimise voltage overshoots during turn-off due to collective stray inductance. The turn-off snubbers provide a zero voltage across the IGBT while the device current turns off, and the turn-on snubbers reduce the voltage across the device as its current builds up. Simplified calculations [39] for determining the snubber component values are presented below:

Assuming that, \( V_d = 115 \sqrt{6} = 282 \) V and \( I_o = 10 \times 1.3 = 13.0 \) A,

Since,

\[
R_s1 = \frac{5V_d}{I_o}
\]  

(6.2)

then,

\[
R_s1 = \frac{(5)(282)}{13.0} \approx 108 \Omega
\]

\[
C_s1 = 33 \text{ nF}
\]

:: The preferred values of \( R_{s1} = 100 \Omega \) and \( C_{s1} = 33 \text{ nF} \) was used. The value of \( C_{s1} \) was selected on the basis of component availability.

From IRG4BC30F IGBT data sheet, average \( t_{off} = 250 \) ns, and choosing \( R_{s2} = 36 \Omega \) for convenience,
Since,
\[ t_{\text{eff}} < \frac{2.3 \cdot L_{s2}}{R_{s2}} \]
thus,
\[ L_{s2} < \frac{t_{\text{eff}} \cdot R_{s2}}{2.3} = \frac{(250 \times 10^{-9})(36)}{2.3} \approx 4.0 \, \mu\text{H} \]

Assuming an overvoltage factor, \( k = 3.0 \),

Since,
\[ C_{ov} = 200 \, k \, C_{s1} \]  \hspace{1cm} (6.4)
thus,
\[ C_{ov} = (200)(3.0)(33.0 \times 10^{-9}) = 19.8 \, \mu\text{F} \]

6.12.2 CROWBAR OVERLOAD PROTECTION

Overcurrent protection is provided by means of the crowbar circuit shown in Figure 6.16. In general, the circuit monitors the d.c. current in the converter and compares it with a certain preset limit. When the threshold is exceeded a signal is generated, which interrupts the current by short-circuiting the converter d.c. link and blowing the fuse.

Current detection is performed using a HTP50 Hall-effect current transducer, whose output voltage signal is supplied via a TL071 voltage follower to a TL071 differential amplifier with an offset adjustment circuit.

The absolute value of the signal is obtained using a precision rectifier circuit and compared
with the preset limit. If the signal exceeds the threshold value of 10 A, a +5 V logic '1' pulse is generated by the LM311 comparator to indicate that an overload has been detected.

The comparator output is applied to the resettable overload indicator via a 74HCT76 J-K flip-flop to provide a visual warning, and to a 74LS123 monostable so that a delayed pulse with a duration of 100 µs is generated to trigger the thyristor.

Isolation between the high voltage converter and the low voltage protection circuit is achieved by a pulse transformer, which transfers the delayed triggering pulse to the thyristor terminals. When the pulse is received the thyristor conducts, and diverts the fault current to a short-circuit path via a 10 A high-rupture capacity fuse.

6.13 D.C. CAPACITOR

A high voltage reservoir capacitor is used to provide a stable power supply for the PWM converter. When the converter operates in the inverter mode, current flows from the capacitor, while in the rectifier mode current flows into the capacitor. The capacitor was selected based on component availability, with a value of 2000 µF and rated at 415 V_dC, which is appropriate for operation with the three-phase 115 V_ac supply.

The capacitor voltage is maintained by an external d.c. source using a three-phase bridge rectifier (Section 6.4) with a series-connected iron-cored inductor. The inductor limits the rate-of-current (di/dt) rise to 10 A in 1.2 ms to ensure a smooth d.c. current, and its value is calculated as follows:

\[ L = \frac{V_l}{\frac{di}{dt}} \]  

(6.5)
Since,
\[
\frac{di}{dt} = \frac{10.0}{1.2 \times 10^{-3}} = 8333.33 \text{ A/s}
\]
and,
\[
V_L = 115 \sqrt{6} = 282 \text{ V}
\]
then,
\[
L = \frac{282}{8333.33} \approx 34 \text{ mH}
\]

When the converter is turned-off, the capacitor voltage is discharged by the circuit shown in Figure 6.17, which reduces the voltage from 350 V to zero in approximately 2 minutes via a 12 kΩ wire-wound resistor. A visual indication is also included using a milliammeter connected in series with the resistor.

Since the capacitor voltage is maintained externally, the inverter may be operated as a full-time compensator i.e. in the inverter mode. It is therefore unnecessary to monitor the capacitor voltage level, and the converter switching algorithm is significantly simplified because no switching allowance need to be provided for maintaining the capacitor charge level. Nevertheless, the solution adds additional harmonics to the system associated with three-phase rectifier circuits.

### 6.14 LOW-PASS FILTERS

The main purpose of the low-pass filter is to remove all high frequency noise appearing on the control circuit signals, due to switching operations and other noise sources. As mentioned earlier, the filter is utilised in the monitoring circuit, to isolate the switching frequency noise from the sampled waveforms, and in the PWM current controller to obtain smooth output
waveforms from the DAC.

The type of filter chosen was the fourth-order Butterworth low-pass filter shown in Figure 6.14, which is relatively simple to design and implement without compromising the performance. Increasing the order of this type of filter increases the accuracy of the approximation to the flat passband of an ideal filter, and a fourth-order filter design was adopted.

The cut-off frequency is defined as the frequency at which the output power has fallen to one-half its zero-frequency level, i.e. 3.01 dB attenuation. However, the filter will not provide infinite attenuation beyond this point, and the attenuation at any frequency is given by:

$$A = 10 \cdot \log_{10} \left[ 1 + \left( \frac{f}{f_c} \right)^{2z} \right] \text{ dB} \quad (6.6)$$

where

- $f$ = Frequency at which the attenuation is required.
- $f_c$ = Cut-off frequency.
- $z$ = Filter order.

Two different filter designs were utilised, one with a cut-off frequency of 3 kHz for the PWM current controller and the other with a cut-off frequency of 5 kHz for the monitoring circuit. The filter for the current controller uses a lower cut-off frequency, because the rate at which the DAC is operating is lower than the converter switching frequency.

Both cut-off frequencies were deliberately designed to be slightly lower than the actual cut-off frequencies, to compensate for the filter non-ideal sloping passband characteristics. The simplified calculation [40] to determine the component values for this filter is given below:
If \( R_1 = 10 \, k\Omega \) and \( R_2 = 2R_1 = 20 \, k\Omega \), then

\[
K = \frac{1}{2\pi f_c R_1}
\]

\[ (6.7) \]

\[
C_1 = \frac{2}{1.8478} \cdot K
\]

\[ (6.8) \]

\[
C_2 = \frac{1.8478}{2} \cdot K
\]

\[ (6.9) \]

\[
C_3 = \frac{2}{0.7654} \cdot K
\]

\[ (6.10) \]

\[
C_4 = \frac{0.7654}{2} \cdot K
\]

\[ (6.11) \]

Giving,

<table>
<thead>
<tr>
<th>Capacitor ( (n=4) )</th>
<th>Calculated value ( (f_c = 3 , \text{kHz}) )</th>
<th>Utilised value ( (f_c = 3 , \text{kHz}) )</th>
<th>Calculated value ( (f_c = 5 , \text{kHz}) )</th>
<th>Utilised value ( (f_c = 5 , \text{kHz}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_1 )</td>
<td>5.74 nF</td>
<td>5.7 nF</td>
<td>3.45 nF</td>
<td>3.45 nF</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>4.9 nF</td>
<td>4.92 nF</td>
<td>2.94 nF</td>
<td>2.88 nF</td>
</tr>
<tr>
<td>( C_3 )</td>
<td>13.86 nF</td>
<td>13.77 nF</td>
<td>8.32 nF</td>
<td>8.3 nF</td>
</tr>
<tr>
<td>( C_4 )</td>
<td>2.03 nF</td>
<td>2.0 nF</td>
<td>1.22 nF</td>
<td>1.22 nF</td>
</tr>
</tbody>
</table>
Figure 6.1: Experimental system schematic diagram
Figure 6.2: Harmonic source schematic diagram
Figure 6.3: Monitoring circuit schematic diagram
Figure 6.4: DSP schematic diagram
Figure 6.5: PWM current controller schematic diagram
Figure 6.6: PWM converter schematic diagram
Figure 6.7: Stabilised power supply circuit
Figure 6.8: Isolated power supply circuit
Figure 6.9: PWM voltage-source converter with snubber network
Figure 6.10: Isolated IGBT gate drive circuit
Figure 6.11 : Current controller
Figure 6.12: Digital-to-analogue converter
Figure 6.14: Current sensing circuit
Figure 6.15: Voltage sensing circuit
Figure 6.16: Crowbar protection circuit
Figure 6.17: D.c. link with discharge path circuit
Figure 6.18: Fourth-order low-pass Butterworth filter
7.1 DIGITAL SIGNAL PROCESSOR

The Texas Instruments TMS320C5x DSP Starter Kit that incorporates a 40 MHz fixed-point TMS320C50 digital signal processor (DSP) was used to determine the required instantaneous compensation currents. This device is capable of executing more than 28 MIPS (million instructions per second), and provides a cost-effective DSP solution using a stand-alone application board for real-time signal processing. It offers the operational flexibility of a high-speed microcontroller and the numerical capability of an array processor.

The use of a DSP is essential, due to the need to determine the instantaneous reactive power equations as quickly and accurately as possible. Although the overall harmonic compensation rate of the active filter is not governed by the calculation alone, the high-speed computation ensures that the PWM converter is able to reproduce the required currents sufficiently accurate and thus, suppressing more harmonics. In addition, the fast response would compensate for the device and circuit propagation delays, which are not controllable parameters.

Since compensation of a three-phase system is involved, the DSP receives digital input data from four different analogue sources, two line voltages and two phase currents, in which the third phase values are determined by calculation. The format for these input signals is given in Figure 7.1. Similarly, two sets of digital output data are sent from the DSP to the PWM current controller with the format given in Figure 7.2, representing the first two phases of the required compensation currents, and the third phase current is obtained using a summing inverting amplifier in the current controller circuit, as explained in Section 6.8.

Communication between the DSP and other analogue circuits are achieved via the DAC and ADC circuits, which are controlled by the interface circuit described in the following section.
The TMS320C5x application board is equipped with a 16-bit digital input/output data port, that is capable of addressing a maximum of 64 external input/output devices sequentially. Consequently, to manage simultaneously the data flow from several input/output devices, an interface circuit is necessary to select which device will have the access to the data bus, as determined by the program.

Figure 7.3 presents the functional schematic diagram of the interface circuit, highlighting the circuit control signals and their interconnections with the relevant input/output devices. A total of four input and two output circuits must be controlled, via two ADCs and DACs respectively, to provide appropriate timing to access the 16-bit data bus. Each ADC is automatically toggled between its two analogue sources after the data is successfully relayed to the DSP, to achieve the effect of operating with four parallel ADCs (Section 6.10).

The interface circuit identifies the device and operation requested by the program, using the control signals and address data received from the DSP. The active low signals /WR and /RD are the output and input enable signals respectively, while the address signals A₀ and A₁ are used to represent the selected input/output device. The circuit acknowledges receipt of these signals by sending active low signals /OEₙ (n = A, B, C and D) to the relevant device, giving it the exclusive access to the data bus. These signals are summarised in the tables of Figure 7.4 and 7.5 respectively.

For input operations, the tri-state latches connected to the output devices hold the previous digital value, and their input terminals are placed in a high impedance state, so that the new data on the data bus does not modify them. The data from the specific addressed input device is then transferred to the data bus by activating its built-in ADC latches, through either /OEᵣ or /OEₐ signals.
During output operations, the latches of the input devices are disabled to prevent their data having access to the data bus. At the same time, the inputs to the latches of the specific output device are activated to enable the data on the data bus to be transferred to them, using either /OE_A or /OE_B signals.

Figure 7.6 shows the interface circuit, which decodes the input signals from the DSP, activates the requested input/output device and provides a common data bus connection to all external devices. The circuit identifies the demanded input/output device through a 2-to-4 line multiplexer (74HCT139), which is directly fed by the device address signals A_0 and A_1 from the DSP address bus.

The control signals /RD and /WR are conditioned using X-OR (74HCT86) and NOR (74HCT02) logic gates, to ensure that only complementary logic states will activate the output of the multiplexer with logic '0'. This effectively eliminates two modes of operation being simultaneously selected by the circuit, due to noise interference.

The outputs from the multiplexer feed the NOR (74HCT02) and OR (74HCT32) logic gates with /RD and /WR signals respectively, producing the signals /OE_n (n = A, B, C or D) with logic '1' and '0' to disable and enable respectively the input/output devices.

As mentioned earlier, the connections of the 16-bit DSP data bus are common to all external devices via latching mechanisms, which allow only the requested data onto the data bus, and prevent data passing to and from the bus from being available to other devices. Since the input devices ADC chips (H18112) have built-in tri-state latches for the purpose, the interface circuit provides only the latching operation for the output device DAC circuits. This is accomplished using two octal D-type transparent latches (74HCT573) for each output device, which are controlled by either /OE_A and /OE_B signals.
Calculation of the compensation currents by both methods is achieved via two specific DSP assembly language programs, with the flowchart shown in Figure 7.7. The program listings for methods A and B are given in Appendices 6 and 7 respectively, while the general computation algorithm implemented in the programs is explained as follows:

a) Define program and data memory start addresses, memory locations for program variables and global DSP registers.

b) Initialise DSP to microcomputer mode, set wait states and set for signed arithmetic operation.

c) Read the instantaneous a-phase ($I_a$) and b-phase ($I_b$) current values from input port PA2 via ADC$_1$.

d) Read the instantaneous a-c line-voltage ($V_{ac}$) and b-c line-voltage ($V_{bc}$) values from input port PA3 via ADC$_2$.

e) Condition and scale the digital input signals, and determine the values of the c-phase current ($I_c$) and a-b line-voltage ($V_{ab}$), which have not been sampled previously.

f) Calculate the required compensation currents using the input phase currents and line-voltages, and scale them to match the output gain of the DAC.

g) Write the required compensation currents i.e. $I_{*c8}$ to output port PA0 and $I_{*cb}$ to output port PA1, via DAC$_1$ and DAC$_2$ respectively.

h) Steps (c) to (h) are repeated, provided no program halting event has taken place.
Figure 7.1: Data format for ADC output signals

Figure 7.2: Data format for DAC input signals
Figure 7.3: Schematic of the input/output interface circuit function
### Figure 7.4: Definition of the interface circuit input signals

<table>
<thead>
<tr>
<th>Description</th>
<th>/RD</th>
<th>/WR</th>
<th>A₁</th>
<th>A₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input enable signal for reading Iₐ or Iₚ</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Input enable signal for reading Vₐc or Vₜc</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Output enable signal for writing Iₚₑₜ₁</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Output enable signal for writing Iₚₑₜ₂</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### Figure 7.5: Definition of the interface circuit output signals

<table>
<thead>
<tr>
<th>Description</th>
<th>/OEₐ</th>
<th>/OEₜ</th>
<th>/OEₜ</th>
<th>/OEₜ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable input from data bus to DAC¹ latches.</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Enable input from data bus to DAC² latches.</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Enable output from ADC¹ to data bus latches.</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Enable output from ADC² to data bus latches.</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Figure 7.6: Input/output interface circuit diagram
Define registers and memory locations for program variables

Initialise DSP and set processor mode to microcomputer

Read phase currents $I_x$ and $I_y$ from PA2

Read line-voltages $V_a$ and $V_b$ from PA3

Condition input values and calculate $I_e$ and $V_t$

Calculate compensation currents, $I_{cs}$ and $I_{cb}$

Write compensation current $I_{cs}$ to PA0

Write compensation current $I_{cb}$ to PA1

No

DSP halt?

Yes

END

Figure 7.7 : Flowchart for DSP program
CHAPTER 8
EXPERIMENTATION

8.1 EXPERIMENTS

Three independent studies were conducted using the prototype rig described in Chapter 6, with the main system parameters involved in these studies being summarised in Appendix 6. In the first study, the basic system of Figure 8.1, comprising a three-phase delta-star connected transformer supplying a three-phase rectifier with a resistive load was investigated. The other two studies included the prototype active filter with the basic system, as in Figure 8.2.

One of the latter studies (method A) used the original $\alpha-\beta$ transformation technique to determine the required compensation currents, while the other (method B) used the phase equations involving the instantaneous reactive power equations developed in Chapter 4. To implement the two techniques, assembly language programs were executed by the DSP, and their source-codes are presented in Appendices 6 and 7 respectively.

Only the simulation and experimental results from one phase are presented in the thesis, due to the symmetry of the balanced three-phase system investigated, to enable a comparison to be made of their suppression performances and to validate the mathematical models developed in Chapter 5.

8.2 DISCUSSION

Figure 8.3(a) shows the experimental line-voltage waveform without the filter, and reveals that the waveform supply is slightly distorted by the harmonic voltages generated by the bridge rectifier. The resulting harmonic spectrum seen in Figure 8.3(b) has a THD of 4.4%, caused
mainly by the 5th and 7th order harmonics.

The results of Figure 8.3 are consistent with the simulated waveform of Figure 8.4(a), in which the 5th and 7th order harmonics are significant. In both cases the distortion in the line-voltage is particularly evident during commutation periods when the rectifier topology changes. However, the harmonic spectrum of the line-voltage in Figure 8.4(b) is slightly different from that of the corresponding practical results. The practical line-voltage waveform has a higher 5th harmonic component (6.2 V compared with 5.4 V) and a lower 7th harmonic component (2.3 V compared with 2.9 V), and the THD for the practical waveform is 20% higher at 4.4% than the 3.6% of the simulated results. A possible explanation for this is the difference between the assumed and actual values of the system source impedance.

Line-voltage waveforms for the system when the active filter was introduced are given in Figures 8.5(a) and 8.6(a) respectively, and these show that a slight compensation effect is achieved. Figure 8.6(a) shows that the line-voltage waveform is relatively smoother using method B, with less superimposed high-frequency low-amplitude components than in method A, due to improved accuracy of the compensation current calculation.

For both compensation methods, the injected currents have little effect on the low-order harmonic components, and induce converter switching frequency harmonics in the line-voltage waveforms. The harmonic spectra for the two methods, shown in Figures 8.5(b) and 8.6(b), exhibit similar results to those for the uncompensated line-voltage in Figure 8.3(b), with a slight reduction in the THD to 3.8% and 2.9% from the 4.4% for the uncompensated line-voltage.

Using method A the magnitude of the harmonic components are slightly reduced, giving 5.8 V for the 5th order and 0.8 V for the 7th order harmonics, compared to 6.2 V for the 5th order and 2.9 V for the 7th order harmonics from the uncompensated system. However, method B produces a further reduction in the 5th order component with a magnitude of 4.2
V, while producing 1.2 V in the 7th order.

Figure 8.7(a) shows that the compensated line-voltage waveform predicted by the rectifier-filter simulation indicates a better harmonic suppression than that obtained practically, due to the better reproduction of the required compensation currents. Furthermore, the magnitude of the main harmonic components (the 5th and 7th) in Figure 8.7(b) are further reduced, with the THD falling to 2.5%. Compared to 3.6 V for the 5th order and 0.9 V for the 7th order harmonics predicted by the simulation, the practical line-voltage waveforms obtained using the two filter strategies still contain the 5th and 7th order harmonics. The discrepancies between the simulation and experimental results are probably due to the inability of the converter to follow accurately the demanded compensation currents.

Examination of the supply current waveform for the system without a filter, given in Figure 8.8(a), reveals the expected distortion. The non-linear currents are particularly significant during commutation periods, when the delayed current changeover of the forward-biased diodes occurs. The THD of 2.1% for the harmonic spectrum of Figure 8.8(b) is again caused predominantly by the 5th and 7th order harmonics.

The experimental waveform of Figure 8.8(a) agrees with the simulated waveform shown in Figure 8.9(a). However, the harmonic spectrum for the supply current waveform given in Figure 8.9(b), shows the magnitudes of the harmonic components to be slightly different for the simulated supply current waveform, with THD of 23.2%. The measured components of 0.25 A and 0.13 A for the 5th and 7th harmonics are lower than that achieved by the rectifier simulation, which predicts 0.36 A and 0.14 A respectively. This slight variation may again be a consequence of the difference between the assumed and actual values of the system impedance.

The supply current waveforms when the active filter was introduced are given in Figures 8.10(a) and 8.11(a), and indicate that both methods are effective in suppressing harmonic
currents. It is evident that the supply current is more sinusoidal with method B than with method A, again due to the improved accuracy and speed in generating the reference compensation currents.

In both cases, the currents injected by the filter suppress most of the low-order harmonic components, without introducing noticeable switching frequency harmonics in the supply current. The harmonic spectra for both methods A and B, given in Figures 8.10(b) and 8.11(b) respectively, show reduced principal harmonic components, resulting in a reduction of the THD to 10.8 % and 9.3 % from the 21.1 % for the uncompensated system.

The simulated supply current waveform from the rectifier-filter model shown in Figure 8.12(a) shows the compensated supply current to be more sinusoidal than the experimental waveforms, using methods A and B, shown in Figures 8.10(a) and 8.11(a). The THD of 8.2 % shown in Figure 8.12(b) predicts that the filter almost totally suppresses the 5th and 7th harmonics, while giving rise to uncharacteristic harmonics of 0.04 A, 0.12 A and 0.06 A for the 2nd, 3rd and 4th order components respectively, which may occur during intervals when the converter currents are used to maintain sufficient charge in the d.c. link capacitor.

The practical supply current harmonic spectrum obtained using method A contains a small 5th harmonic (0.12 A) and almost no 7th harmonic, as compared with 0.25 A for the 5th order and 0.13 A for the 7th harmonic components for the uncompensated system. In addition, the waveform exhibits an increase in non-characteristic harmonics of 0.14 A and 0.05 A for the 3rd and 4th harmonic components. The supply current waveform using method B has almost no 5th and 7th order harmonics, but there are noticeable non-characteristic harmonics of 0.13 A and 0.1 A for the 2nd and 3rd harmonic components. In both methods, the undesirable increase in the non-characteristic harmonics may be a consequence of the compensating currents departing momentarily from the reference.

In comparison with the THD of 21.1% with the uncompensated system, the supply current...
results show that method B achieved a better harmonic suppression than method A. Method A has a THD of 10.8 %, representing a reduction of 48 %, whereas method B with a THD of 9.3 % produces a reduction of 56 %. These values are however less than those predicted, which reduces the THD from 23.2 % to 8.5 %, giving a reduction of 63 %.

In addition to the difference between the assumed and actual system impedance, the performance variation between the simulated and experimental results may be attributed to factors which are not included in the mathematical models developed, such as the converter losses, digital quantisation and rounding errors, the control propagation and computation delays, the possible amplification of residual d.c. offsets in the control circuits, signal noise, electromagnetic interference etc. Furthermore, the provision of an extra rectifier to maintain the voltage of the d.c. link capacitor may have contributed to the increase in the harmonic currents that the filter has to compensate, leading to the impression of an inferior suppression performance by the filter. Such discrepancies may also be due to partial suppression of synchronous link inductor and the stray inductances in the practical system.

The apparent improvement of method B over method A is mainly due to the absence of the transformation stages, which increases the efficiency of the calculation process implemented by the DSP. Computing in the phase equations simplifies the computation algorithm by requiring fewer arithmetic operations, which may cause considerable digital rounding errors in fixed-point processors, particularly when several large digital numbers are multiplied and rounded.

Even though floating-point processors may not be significantly affected by the rounding errors, the reduced computation steps of method B can still provide a shorter program source-code and a reduction in the overall execution time. When the program is rapidly executed by the DSP, the rate at which the filter samples the distorted supply and computes the reference compensation currents increases, and allows more harmonics to be suppressed. This improvement is evident in Figures 8.10(a) and 8.11(a), which indicate a relatively more
sinusoidal current waveform using method B.

Figures 8.13 and 8.14 show the reference and actual compensation currents for the system with the filter. These indicate that the compensation currents generated by the converter followed their reference values, but not as precisely as predicted by the rectifier-filter simulation, probably due to the finite synchronous link inductor current response (\(\frac{di}{dt}\)). The compensation current using method A (Figure 8.13) is less accurate than that using method B (Figure 8.14), which was found to be increasingly significant at higher voltage and current operations due to increases in the digital quantisation and rounding errors.

The simulated compensation current of Figure 8.15(b) follows closely the reference current of Figure 8.15(a), which explains why the predicted suppression was better than the practical results. Without the propagation and computation delays a more accurate reference compensation currents can be achieved, and the compensation currents can be made instantaneously available for injection. Furthermore, the simulated compensation currents are not subjected to the various losses occurring in a practical PWM converter.

The experimental load voltage and current waveforms given in Figures 8.16(a) and 8.16(b), for the system without the filter are consistent with the simulation results given in Figures 8.17(a) and 8.17(b). Similarly, the load voltage and current waveforms when using method A, and when using method B given in Figures 8.18 and 8.19 agree with the rectifier-filter simulation results in Figure 8.20(a) and 8.20(b). In both simulated and experimental results the switching frequency from the compensation currents is superimposed on the d.c. load voltage and current waveforms.

The d.c. link voltage and current waveforms for the system using both methods given in Figures 8.22 and 8.23 also show a relative consistency with the rectifier-filter simulation results in Figure 8.21. However, the experimental d.c. link voltages are higher than predicted by the rectifier-filter simulation, because the system utilises an external d.c. source to maintain
constant charge in the reservoir capacitor. These load and d.c. link waveforms verify that the mathematical models developed were adequate to study the general active filter suppression performance for the proposed system.
Figure 8.2: Experimental system with the active filter
Figure 8.3:  
(a) Experimental line-voltage waveform without active filter  
(b) Line-voltage harmonic spectrum without active filter

Figure 8.4:  
(a) Simulated line-voltage waveform without active filter.  
(b) Line-voltage harmonic spectrum without active filter.
Figure 8.5:  
(a) Experimental line-voltage waveform with active filter using method A  
(b) Line-voltage harmonic spectrum with active filter using method A

Figure 8.6:  
(a) Experimental line-voltage waveform with active filter using method B  
(b) Line-voltage harmonic spectrum with active filter using method B

Figure 8.7:  
(a) Simulated line-voltage waveform with active filter  
(b) Line-voltage harmonic spectrum with active filter
Figure 8.8:  
(a) Experimental supply current waveform without active filter  
(b) Supply current harmonic spectrum without active filter

Figure 8.9:  
(a) Simulated supply current waveform without active filter.  
(b) Supply current harmonic spectrum without active filter.
Figure 8.10: a) Experimental supply current waveform with active filter using method A  
       b) Supply current harmonic spectrum with active filter using method A

Figure 8.11: a) Experimental supply current waveform with active filter using method B  
       b) Supply current harmonic spectrum with active filter using method B

Figure 8.12: a) Simulated supply current waveform with active filter  
       b) Supply current harmonic spectrum with active filter
Figure 8.13: Ch1 - Experimental reference compensation current using method A
Ch2 - Experimental compensation current using method A

Figure 8.14: Ch1 - Experimental reference compensation current using method B
Ch2 - Experimental compensation current using method B

Figure 8.15: a) Simulated reference compensation current
b) Simulated compensation current
Figure 8.16: 
(a) Experimental load voltage without active filter.  
(b) Experimental load current without active filter.

Figure 8.17: 
(a) Simulated load voltage without active filter.  
(b) Simulated load current without active filter.
Figure 8.18:  
(a) Experimental load voltage with active filter using method A  
(b) Experimental load current with active filter using method A

Figure 8.19:  
(a) Experimental load voltage with active filter using method B  
(b) Experimental load current with active filter using method B

Figure 8.20:  
(a) Simulated load voltage with active filter  
(b) Simulated load current with active filter
Figure 8.21:  
(a) Experimental d.c. link voltage with active filter using method A  
(b) Experimental d.c. link current with active filter using method A

Figure 8.22:  
(a) Experimental d.c. link voltage with active filter using method B  
(b) Experimental d.c. link current with active filter using method B

Figure 8.23:  
(a) Simulated d.c. link voltage with active filter  
(b) Simulated d.c. link current with active filter
CHAPTER 9
CONCLUSION AND FURTHER WORK

9.1 CONCLUSION

The research work reported in this thesis led to the design and construction of a successful prototype active filter for harmonic elimination in power systems. The use of a relatively fast DSP for calculating the reference compensation currents proved to be extremely valuable, when compared to a discrete component or conventional microprocessor approach, due to the high computational speed and operational flexibility offered. Two methods of defining the compensation currents, derived from the instantaneous reactive power theory [1,2], have been investigated. While the original method uses a series of transformations (method A), the proposed method bypasses this redundant stage and directly calculates the variables in their phase value form (method B).

Furthermore, two mathematical models incorporating tensor techniques were utilised to analyse the theoretical performance of the filtering scheme. Consequently, two simulations were performed to verify the harmonic generation of a typical three-phase rectifier load, and also to demonstrate the possibility of harmonic suppression using the instantaneous reactive power equations. The simulation results of the rectifier model confirm that the main harmonics generated by the 6-pulse static power converter are the 5th and 7th components, with the average THD values being about 3.6% and 23.2% for the supply line-voltages and currents respectively. Results from the rectifier-filter model verified that the proposed active filter is capable of eliminating power system harmonics, as produced by the earlier model, providing average harmonic suppression of 30% and 65%, for the supply line-voltages and currents respectively.

The experimental rig was used to confirm the theoretical results obtained using both methods,
in addition to a system without the active filter. Similar results were obtained without the filter, with average THD values of about 4.4% and 21.1% for the supply line-voltages and currents respectively. Even though the prototype active filters were adequate as harmonic compensators, the suppression performance using either method was inferior to that predicted by the rectifier-filter model. The performance improvement offered by method B is clear, with the average harmonic suppression of 14% and 48% caused by method A, increasing to 34% and 56% for the supply line-voltages and currents in method B. Calculating the reference compensation currents in phase values instead of undergoing transformation stages improves both the speed and accuracy of the required results. Although it was evident that the active filter suppresses most of the low frequency harmonics, high frequency components are inevitably present due to the PWM converter switching operation. These may be effectively compensated by incorporating suitable tuned passive filters in parallel with the active filter.

Even though the experimental results have demonstrated that the proposed compensation scheme works, the discrepancies between the experimental and theoretical results may be attributed to the idealised system parameters used in the mathematical models. Certain non-ideal aspects of the system neglected in the mathematical models, such as converter switching and snubber network losses, stray inductances, amplification of residual d.c. offsets, finite device response time and component imperfections, etc may have contributed to the slight performance differences. Furthermore, the provision of an extra rectifier to maintain a stable d.c. link voltage for the converter may also add additional harmonics in the experimental system.

9.2 FURTHER DEVELOPMENT

There are several key aspects of the prototype filtering scheme which would benefit from further research and development work. The inclusion of a faster processor featuring floating-point capability would be advantageous, to minimise the digital rounding errors for greater
accuracy, without sacrificing the computation time. For operation with higher supply voltages and currents, it is preferable to operate with at least a 32-bit processor, so that these higher values can be precisely represented, with minimum digital quantisation errors.

Another possible area for improvement lies in the equation for determining the compensation currents, so that conditions such as the unbalanced [41] and low power factor load currents can be accounted for simultaneously. This may be in the form of extended instantaneous reactive power theory equations, to include other harmonic related parameters and variables, or alternatively the introduction of an entirely different concept [42,43] for extracting the generalised compensation currents.

The PWM converter has several possibilities for improvement, because it must generate precisely the required anti-phase harmonic currents computed by the DSP. Any refinement that leads to a faster response time, more accurate modulation and less electromagnetic interference will contribute to a better harmonic suppression by the active filter. In particular, more sophisticated and perhaps superior PWM feedback or feedforward current controllers [35], such as the synchronised carrier modulation, suboscillation, optimal subcycle, space vector, predictive, field orientation and trajectory tracking methods may offer improved compensation current reproduction. A at higher switching frequency ( > 10 kHz ) is also an alternative that may be considered for producing smoother and more accurate filter currents. For schemes operating with variable switching frequencies, the solution for minimising the entire bandwidth of switching frequency harmonics should be addressed accordingly.

The converter should be adequately shielded to prevent electromagnetic interference propagating to the low voltage control circuits, or vice versa, which are particularly susceptible at higher switching frequencies. Multiple parallel converter configuration [26,28,44] are more appropriate for high filter current applications, so that each filter handles only a small proportion of the total required compensation current, thus avoiding excessive current and thermal ratings.
Another modification that may be considered is to make the converter fully self-sustaining in terms of the d.c. link voltage, providing its own d.c. voltage for the reservoir capacitor without the need for an external d.c. source. This feature requires a proportion of the switching time to be allocated to operating the converter in the rectifying mode, so that the capacitor is sufficiently charged at all times. However, the quality of suppression may be degraded, since the filter currents will not follow the reference currents at regular intervals when the capacitor voltage momentarily drops below the threshold level.

The monitoring circuits may also be enhanced such that they condition the signals to directly provide the active and reactive components of the distorted supply phase currents and the line voltages. These components offer a shorter computation algorithm than when using the instantaneous reactive power theory, or alternatively provide a different method of determining the suitable compensation current signals.

Hybrid configurations of active and passive power filters [27,30] may provide a prospect for further work, combining the superior attributes of both filters. Such a scheme may be employed where the principal harmonic components are eliminated using either the passive or active part, and the remaining harmonics are suppressed by the other. The passive part of the hybrid filter may also be operated to restore the power factor, or to suppress the residue of converter switching frequency harmonics.
FOURIER WAVEFORM ANALYSIS

An alternating waveform which is not sinusoidal is said to be complex, and can be described by a series of sine and cosine waves whose frequencies are exact integral multiples of the fundamental frequency.

Consider the waveform shown below:

![Complex waveform](image)

Figure A1.1: Complex waveform

In a Fourier series, the instantaneous value of the cyclic complex function $g(t)$ are determined by the expression:

$$g(t) = a_0 + \sum_{n=0}^{\infty} \left[ a_n \cos(n\omega t) + b_n \sin(n\omega t) \right]$$

\[(A1.1)\]
If the function repeats over a full cycle of the fundamental \(( T = 2\pi )\), then the Fourier coefficients are given by:

\[
a_0 = \frac{1}{T} \int_0^T g(t) \, dt \quad \text{(A1.2)}
\]

\[
a_n = \frac{2}{T} \int_0^T g(t) \cos(n \omega t) \, dt \quad \text{(A1.3)}
\]

\[
b_n = \frac{2}{T} \int_0^T g(t) \sin(n \omega t) \, dt \quad \text{(A1.4)}
\]

where, \( \omega = \) Fundamental frequency \( = 2\pi f \)

\( f = \) Fundamental frequency

\( n = \) Harmonic order
HARMONIC STANDARDS

1. Australia : AS2279, "Disturbances in mains supply networks. ".


8. USA : "IEEE guide for harmonic control and reactive compensation of static power convertors. ".

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DERIVATION OF PHASE VALUE EQUATIONS

The phase equations are obtained by manipulating the $\alpha$-$\beta$ equations. For convenience, the original form of the equations are repeated below:

\[ \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \]  
(A3.1)

\[ \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \]  
(A3.2)

\[ q = e_\alpha i_\beta - e_\beta i_\alpha \]  
(A3.3)

\[ \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} = \begin{bmatrix} e_\alpha & e_\beta \\ -e_\beta & e_\alpha \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ -q \end{bmatrix} \]  
(A3.4)

\[ \begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = \begin{bmatrix} \frac{2}{\sqrt{6}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} \]  
(A3.5)
For simplicity, let

\[ E_{ab} = (e_a - e_b) \]
\[ E_{bc} = (e_b - e_c) \]
\[ E_{ca} = (e_c - e_a) \]

Equations (A3.1 to A3.5) can be expanded to provide nine simultaneous equations, the solution of which can be achieved by successive substitution and simplification:

\[ e_\alpha = \frac{1}{\sqrt{6}} (2e_a - e_b - e_c) = \frac{1}{\sqrt{6}} (E_{ab} - E_{ca}) \]  
(A3.6)

\[ e_\beta = \frac{1}{\sqrt{2}} (e_b - e_c) = \frac{1}{\sqrt{2}} E_{bc} \]  
(A3.7)

\[ i_\alpha = \frac{1}{\sqrt{6}} (2i_a - i_b - i_c) \]  
(A3.8)

\[ i_\beta = \frac{1}{\sqrt{2}} (i_b - i_c) \]  
(A3.9)

\[ i_{ca}^* = \frac{qe_\beta}{(e_\alpha^2 + e_\beta^2)} \]  
(A3.10)

\[ i_{c\beta}^* = \frac{-qe_\alpha}{(e_\alpha^2 + e_\beta^2)} \]  
(A3.11)

\[ i_{ca}^* = \frac{1}{\sqrt{3}} (\sqrt{2} i_{ca}^*) \]  
(A3.12)

\[ i_{cb}^* = \frac{1}{\sqrt{3}} \left( \frac{-i_{ca}^* + \sqrt{3} i_{c\beta}^*}{\sqrt{2}} \right) \]  
(A3.13)

\[ i_{cc}^* = \frac{1}{\sqrt{3}} \left( \frac{-i_{ca}^* - \sqrt{3} i_{c\beta}^*}{\sqrt{2}} \right) \]  
(A3.14)
Substituting Equations A3.6 to A3.9 into Equation A3.3 and simplifying:

\[ q = e_a i_B - e_b i_A \]

\[
= \left[ \frac{1}{\sqrt{6}} (2e_a - e_b - e_c) \right] (i_b - i_c) \left[ \frac{1}{\sqrt{2}} (e_b - e_c) \right] \left[ \frac{1}{\sqrt{6}} (2i_b - i_a - i_c) \right] 
\]

\[
= \frac{1}{\sqrt{12}} \left[ + (2e_a - e_b - e_c)(i_b - i_c) - (e_b - e_c)(2i_b - i_a - i_c) \right]
\]

\[
= \frac{2}{\sqrt{12}} \left[ e_a i_b - e_a i_c - e_b i_a + e_b i_c + e_c i_a - e_c i_b \right]
\]

\[
= -\frac{1}{\sqrt{3}} \left[ i_a (e_b - e_c) + i_b (e_c - e_a) + i_c (e_a - e_b) \right]
\]

\[
= -\frac{1}{\sqrt{3}} \left[ i_a E_{bc} + i_b E_{ca} + i_c E_{ab} \right]
\]

Next, Equations 4.6 and 4.7 are substituted into the common denominator of Equations A3.10 and A3.11:

\[
(e_a^2 + e_b^2) = \left[ \frac{1}{\sqrt{6}} (2e_a - e_b - e_c) \right]^2 + \left[ \frac{1}{\sqrt{2}} (e_b - e_c) \right]^2
\]

\[
= \frac{(2e_a - e_b - e_c)^2}{6} + \frac{(e_b - e_c)^2}{2}
\]

\[
= \frac{(2e_a - e_b - e_c)^2}{6} + \frac{3(e_b - e_c)^2}{2}
\]

\[
= \frac{1}{3} \left[ 2e_a^2 + 2e_b^2 + 2e_c^2 - 2e_a e_b + 2e_a e_c + 2e_b e_c \right]
\]

\[
= \frac{1}{3} \left[ (e_a - e_b)^2 + (e_b - e_c)^2 + (e_c - e_a)^2 \right]
\]

\[
= \frac{1}{3} \left[ E_{ab}^2 + E_{bc}^2 + E_{ca}^2 \right]
\]

Equations A3.10 and A3.11 can be expanded in terms of the phase values quantities, using Equations A3.6, A3.7 and A3.16:
\[ i_{ca}^* = \frac{qe_\beta}{(e_a^2 + e_\beta^2)} \]

\[ = -\frac{1}{\sqrt{3}} \left( i_a E_{bc} + i_b E_{ca} + i_c E_{ab} \right) \frac{1}{\sqrt{2}} E_{bc} \]

\[ = \frac{1}{3} \left( E_{ab}^2 + E_{bc}^2 + E_{ca}^2 \right) \]

\[ = -\sqrt{\frac{3}{2}} \left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] E_{bc} \]

\[ i_{cb}^* = \frac{-qe_a}{(e_a^2 + e_\beta^2)} \]

\[ = \frac{1}{\sqrt{3}} \left( i_a E_{bc} + i_b E_{ca} + i_c E_{ab} \right) \frac{1}{\sqrt{2}} (E_{ab} - E_{ca}) \]

\[ = \frac{1}{3} \left( E_{ab}^2 + E_{bc}^2 + E_{ca}^2 \right) \]

\[ = \frac{1}{\sqrt{2}} \left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] (E_{ab} - E_{ca}) \]

Finally, the required phase values can be derived using Equation A3.17 and A3.18:

\[ i_{ca}^* = \frac{1}{\sqrt{3}} (\sqrt{2} i_{ca}^*) \]

\[ = \frac{1}{\sqrt{3}} \frac{\sqrt{2} q e_\beta}{(e_a^2 + e_\beta^2)} \]

\[ = \left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] (e_b - e_c) \]

\[ = (e_b - e_c) M \]
\[ i_{cb}^* = \frac{1}{\sqrt{3}} \left( \frac{-i_{\alpha \epsilon}^* + \sqrt{3} i_{\epsilon \beta}^*}{\sqrt{2}} \right) \]

\[ = \frac{q}{\sqrt{6}(e_\alpha^2 + e_\beta^2)} \left( -e_\beta - \sqrt{3} e_\alpha \right) \]

\[ = -\left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] \left[ \frac{-E_{bc} - E_{ab} + E_{ca}}{2} \right] \]

\[ = -\left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] \left[ \frac{-e_b^2 - (e_a - e_b) + (e_c - e_a)}{2} \right] \]

\[ = \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \left( e_c - e_a \right) \]

\[ = (e_c - e_a) M \]

\[ i_{cc}^* = \frac{1}{\sqrt{3}} \left( \frac{-i_{\epsilon \alpha}^* - \sqrt{3} i_{\epsilon \beta}^*}{\sqrt{2}} \right) \]

\[ = \frac{q}{\sqrt{6}(e_\alpha^2 + e_\beta^2)} \left( -e_\beta + \sqrt{3} e_\alpha \right) \]

\[ = -\left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] \left[ \frac{-E_{bc} + E_{ab} - E_{ca}}{2} \right] \]

\[ = -\left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] \left[ \frac{-e_b^2 + (e_a - e_b) - (e_c - e_a)}{2} \right] \]

\[ = \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \left( e_a - e_b \right) \]

\[ = (e_a - e_b) M \]

where

\[ M = -\left[ \frac{i_a E_{bc} + i_b E_{ca} + i_c E_{ab}}{E_{ab}^2 + E_{bc}^2 + E_{ca}^2} \right] \]

\[ = \frac{i_a (e_c - e_b) + i_b (e_a - e_c) + i_c (e_b - e_a)}{(e_a - e_b)^2 + (e_b - e_c)^2 + (e_c - e_a)^2} \]

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FOURTH-ORDER RUNGE-KUTTA

The Fourth-Order Runge-Kutta algorithm is a numerical integration method for determining the solution of differential equations of the form:

\[ \frac{dy}{dt} = f(t,y) ; \quad y(t_0) = y_o \quad (A4.1) \]

where \( y(t_0) \) is the initial value of the function e.g. at \( t_0 = 0 \). The value of the function \( y(t) \) at a time \( t = (t_0 + h) \), where \( h \) is the integration step-time, is:

\[ y(t) = y(t_0) + h \left( \frac{k_1}{6} + 2k_2 + 2k_3 + k_4 \right) \quad (A4.2) \]

where

\[ k_1 = f(t_0, y_o) \quad (A4.3) \]
\[ k_2 = f(t_0 + \frac{h}{2}, y_o + \frac{hk_1}{2}) \quad (A4.4) \]
\[ k_3 = f(t_0 + \frac{h}{2}, y_o + \frac{hk_2}{2}) \quad (A4.5) \]
\[ k_4 = f(t_0 + h, y_o + hk_3) \quad (A4.6) \]

The step-time \( h \) should be sufficiently short in order to produce accurate and stable results.
APPENDIX 5

MAIN SIMULATION PARAMETERS

1. Supply line-voltage, \( V_s = 115 \text{ V} \)
2. Supply frequency, \( f_s = 50 \text{ Hz} \)
3. Supply phase resistance, \( R_s = 0.1 \Omega \)
4. Supply phase inductance, \( L_s = 10 \text{ mH} \)
5. Load resistance, \( R_{\text{load}} = 300 \Omega \)
6. Load inductance, \( L_{\text{load}} = 2.5 \text{ mH} \)
7. Synchronous link resistance, \( R_{\text{link}} = 0.5 \Omega \)
8. Synchronous link inductance, \( L_{\text{link}} = 37 \text{ mH} \)
9. DC link capacitance, \( C_{dc} = 2000 \mu\text{F} \)
10. DC link resistance, \( R_{dc} = 0.01 \Omega \)
11. DC link inductance, \( L_{dc} = 50 \mu\text{H} \)
12. Converter switching frequency, \( f_c = 8 \text{ kHz} \)
13. Amplitude of switching frequency, \( \xi = 0.2 \text{ V} \)
APPENDIX 6

MAIN EXPERIMENTAL PARAMETERS

1. Supply line-voltage, \( V_s = 115 \) V
2. Supply frequency, \( f_s = 50 \) Hz
3. Load resistance, \( R_{\text{load}} = 300.5 \) \( \Omega \)
4. Load inductance, \( L_{\text{load}} = 2.52 \) mH
5. Synchronous link resistance, \( R_{\text{link}} = 0.5 \) \( \Omega \)
6. Synchronous link inductance, \( L_{\text{link}} = 36.8 \) mH
7. DC link capacitance, \( C_{\text{dc}} = 2000 \) \( \mu F \)
8. Converter switching frequency, \( f_s = 8 \) kHz
9. Amplitude of switching frequency, \( \xi = 0.2 \) V
APPENDIX 7

DSP PROGRAM USING METHOD A

:mmregs
.ds 0400h ; Defining the TMS320 registers
Ia .set 0014h ; Start data at address 400h
Ix .set 0012h ; Address of la from I/P port
Iy .set 0016h ; Address of lb from I/P port
lb .set 0018h ; Address of lb
lc .set 001ah ; Address of lc
Ex .set 001eh ; Address of Eac from I/P port
Eac .set 001eh ; Address of Eac (I/P)
Eca .set 0022h ; Address of Eca
Ey .set 0024h ; Address of Ebc from I/P port
Ebc .set 0026h ; Address of Ebc (I/P)
Ecb .set 0028h ; Address of Ecba
Eba .set 002ah ; Address of Eba
Iab .set 002eh ; Address of lab
lac .set 0032h ; Address of lac
Ibc .set 0034h ; Address of Ibc
Ed .set 0036h ; Address of Ed
Eq .set 0038h ; Address of Eq
Id .set 003ah ; Address of Id
lEdqL .set 003eh ; Address of [ld(Eq)] (low)
IEdqH .set 0042h ; Address of [ld(Eq)] (high)
EqqL .set 004ch ; Address of [6*Eq*A2] (low)
EqqH .set 004eh ; Address of [6*Eq*A2] (high)
Ez1 .set 0052h ; Address of [2*Eq] (low)
Ez2 .set 0054h ; Address of [Ed-Eq] (low)
Ax .set 0056h ; Address of [la(Ecb) + lb(Eac)+ lc(Eab)]
Bx .set 0058h ; Address of [Ebc^2 + Eac^2 + Eba^2]
AAbs .set 005ah ; Address of ABS ( Mx x Ax )
BAbs .set 005ch ; Address of ABS ( Nx x Bx )
ABBSign .set 005eh ; Address of sign of ( Xx/Yx )
Zx .set 0062h ; Address of ( Xx/Yx )
Qx .set 0064h ; Address of ( Xx/Yx )
ICa  .set 0066h ; Address of ICa
ICb  .set 0068h ; Address of ICb

------------------------------------------------------------------------- DSP Initialisation -------------------------------------------------------------------------

.ps 0a00h ; Start program address at 0a00h

START :
  ldp #0 ; Set Data Page = 0
  spik #8b4h, PMST ; Use 9K on-chip RAM in program &
                   data space. Microcomputer mode.
  lacc #0h ; Load ACC = 1h ( for 1 wait states )
  samm CWSR ; Software wait states = 1
  samm PDWSR ; Program wait states = 1
  lacc #7h ; Load ACC = 4h ( for 4 wait states )
  samm IOWSR ; I/O wait states = 4
  setc OVM ; Reset overflow mode
  clrc SXIM ; Set for signed arithmetic operation

------------------------------------------------------------------------- Input from Digital Ports ( 52h & 53h ) -------------------------------------------------------------------------

Rpt1 :
  ldp #8 ; Set Data Page = 8
  in Ix,PA2 ; Read Ix from port 52h
  bit Ix,0 ; Test bit 16
  bcond Rpt1,TC ; If TC=0 repeat input
  bit Ix,2 ; Test bit 14
  bcond Rpt1,NTC ; If TC=0 repeat input

Rpt2 :
  in Iy,PA2 ; Read Iy from port 52h
  bit Iy,0 ; Test bit 16
  bcond Rpt2,TC ; If TC=1 repeat input
  bit Iy,2 ; Test bit 14
  bcond Rpt2,NTC ; If TC=0 repeat input

Rpt3 :
  in Ex,PA3 ; Read Ex from port 53h
  bit Ex,0 ; Test bit 16
  bcond Rpt3,TC ; If TC=0 repeat input
  bit Ex,2 ; Test bit 14
  bcond Rpt3,NTC ; If TC=0 repeat input

Rpt4 :
  in Ey,PA3 ; Read Ey from port 53h
  bit Ey,0 ; Test bit 16
  bcond Rpt4,TC ; If TC=1 repeat input
  bit Ey,2 ; Test bit 14
  bcond Rpt4,TC ; If TC=0 repeat input

------------------------------------------------------------------------- Stage I Data Processing -------------------------------------------------------------------------

  bit Ix,3 ; Test bit 13 of Ix ( sign )
  lacc Ix,16 ; ACC high := Ix
  and #0fffh,16 ; Discard control bits
  rpt #1 ; REPEAT 2x
  sfl ; Shift left 1-bit
  xc 1,NTC ; IF TC = 0 THEN
  neg ; Negate ACC
  sach Ia ; Ia := ACC high = Ix
  bit Iy,3 ; Test bit 13 of Iy ( sign )
  lacc Iy,16 ; ACC high := Iy
and #0ffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach lb ; lb := ACC high = ly
bit Ex,3 ; Test bit 13 of Ex ( sign )
lacc Ex,16 ; ACC high := Ex
and #0ffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach Eac ; Eac := ACC high = Ex
neg ; Negate ACC
sach Eca ; Eca := ACC high = -Ex
bit Ey,3 ; Test bit 13 of Ey ( sign )
lacc Ey,16 ; ACC high := Ey
and #0ffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach Ebc ; Ebc := ACC high = Ey
neg ; Negate ACC
sach Ecb ; Ecb := ACC high = -Ey
setc SXM ; Set sign extension mode, SXM := 1
lacc la,16 ; ACC high := la
add lb,16 ; ACC := ACC + ACCB = la + lb
neg ; Negate ACC
sach lc ; lc := ACC high = -( lb + ia )
lacc Eac,16 ; ACC high := Eac
add Ecb,16 ; ACC := Eac + Ecb
sach Eab ; Eab := ACC high
neg ; Negate ACC := - Eab
sach Eba ; Eba := ACC high = Eba

******************************************************************************

Stage II Data Processing ******************************************************************************

lacc Eab,16 ; ACC := Eab
add Eac,16 ; ACC := Eab + Eac
sach Ed ; Ed := ACC high
lacc Ebc,16 ; ACC := Ebc
sach Eq ; Eq := ACC high
sfl ; Shift left 1-bit
sach Ez1 ; Ez1 := 2 * Eq
lacc Ed,16 ; ACC := Ed
add Eq,16 ; ACC := Ed + Eq
neg ; Negate ACC := - ( Ed + Eq )
sach Ez2 := ACC high
lt Ed := TREG0 := Ed
mpy Ed := PREG := Ed^2
pac
sfl := ACC := PREG
scl EddL := EddL := ACC low = 2 * Ed
sach EddH := EddH := ACC high = 2 * Ed
lt Eq := TREG0 := Eq
mpy Eq := PREG := Eq^2
pac := ACC := PREG
sfl := Shift left 1-bit
sacb := ACCB := ACC

rpt #1 := REPEAT 2x
sfl := Shift left 1-bit
sbb := ACC := ACC - ACCB
scl EqqL := EqqL := ACC low
sach EqqH := EqqH := ACC high
lacc la,16 := ACC high := la
sub lb,16 := ACC := la - lb
sach lab := lab := ACC high
lacc la,16 := ACC high := la
sub lc,16 := ACC := la - lc
sach lac := lac := ACC high
lacc lb,16 := ACC high := lb
sub lc,16 := ACC := lb - lc
sach lbc := lbc := ACC high
lacc lab,16 := ACC high := lab
add lac,16 := ACC := lab + lac
sach ld := ld := ACC high
lacc lbc,16 := ACC high := lbc
sach lq := lq := ACC high
lt Ed := TREG0 := Ed
mpy lq := PREG := Ed x lq
spl lEdqL := lEdqL := PREG low
sph lEdqH := lEdqH := PREG high
lt Eq := TREG0 := Eq
mpy ld := PREG := Eq x ld
spl lEqdL := lEqdL := PREG low
sph lEqdH := lEqdH := PREG high
lacc lEqdH,16 := ACC := lEqdH 00
adds lEqdL := ACC := lEqdH + lEqdL
subs lEqdL := ACC := ( lEqdH + lEqdL ) - ( 00 + lEqdL )
sub lEqdH,16 := ACC := ( lEqdH + lEqdL ) - ( lEqdH + lEqdL )
sach Ax := Ax := ACC high
abs := ACC := ABS ( Ax )
Calculate required compensation currents

lt Ax ; TREG0 := Ax
mpy Bx ; PREG := Ax x Bx
sph ABSign ; ABSign := PREG high
lacc AAbs,16 ; ACC high := AAbs
rpt #15 ; REPEAT 16x
subc BAbs ; Conditionally AAbs - BAbs
bit ABSign,0 ; Test bit 16 of QUOTIENT
scl Qx ; Qx := ACC low
lacc Qx,16 ; ACC high := Qx
xc 1,TC ; IF TC = 1
neg ; Negate ACC
sach Zx ; Zx := ACC high
lt Zx ; TREG0 := Zx
mpy Ez1 ; PREG := Zx x Ez1
pac ; ACC := PREG
sfl ; Shift left 1-bit
circ SXM ; Reset sign extension, SXM := 0
rpt #3 ; REPEAT 4x
sfr ; Shift right 1-bit
setc SXM ; Set sign extension, SXM := 1
sach ICa ; ICa := ACC low (12-bit)
mpy Ez2 ; PREG := Zx x Ez2
pac ; ACC := PREG
sfl ; Shift left 1-bit
circ SXM ; Reset sign extension, SXM := 0
rpt #3 ; REPEAT 4x
sfr ; Shift right 1-bit
setc SXM ; Set sign extension, SXM := 1
sach ICb ; ICb := ACC low (12-bit)

Output to Digital Ports (50H & 51H)
APPENDIX 8

DSP PROGRAM USING METHOD B

.mmregs
.ds 0400h ; Defining the TMS320 registers

Ix .set 0022h ; Address of la from I/P port
Ia .set 0024h ; Address of Ia
Iy .set 0026h ; Address of lb from I/P port
Ib .set 0028h ; Address of lb
Ic .set 002ah ; Address of Ic
Ex .set 002ch ; Address of Eac from I/P port
Eac .set 002eh ; Address of Eac (I/P)
Eca .set 0032h ; Address of Eca
Ey .set 0034h ; Address of Ebc from I/P port
Ebc .set 0036h ; Address of Ebc (I/P)
Ecb .set 0038h ; Address of Ecb
Eba .set 003ah ; Address of Eba
Eab .set 003ch ; Address of Eab
IEacbL .set 003eh ; Address of [la(Ecb)] (low)
IEacbH .set 0042h ; Address of [la(Ecb)] (high)
IEbacL .set 0044h ; Address of [lb(Eac)] (low)
IEbacH .set 0046h ; Address of [lb(Eac)] (high)
IEcbaL .set 0048h ; Address of [lc(Ebc)] (low)
IEcbaH .set 004ah ; Address of [lc(Ebc)] (high)
Ecb2L .set 004ch ; Address of Ecb^2 (low)
Ecb2H .set 004eh ; Address of Ecb^2 (high)
Eac2L .set 0052h ; Address of Eac^2 (low)
Eac2H .set 0054h ; Address of Eac^2 (high)
Eba2L .set 0056h ; Address of Eba^2 (low)
Eba2H .set 0058h ; Address of Eba^2 (high)
Ax .set 005ah ; Address of [la(Ecb) + lb(Eac)+ Ic(Eab)]
Bx .set 005ch ; Address of [Ebc^2 + Eac^2 + Eba^2]
AAbs .set 005eh ; Address of ABS ( Mx x Ax )
BAbs .set 0062h ; Address of ABS ( Nx x Bx )
ABSign .set 0064h ; Address of sign of ( XxYx )
Zx .set 0066h ; Address of ( XxYx )
Qx .set 0068h ; Address of ( XxYx )
ICa .set 006ah ; Address of ICa
ICb .set 006ch ; Address of ICb

*.............................. DSP Initialisation ..............................*

.ps 0a00h ; Start program address at 0a00h
START : ldp #0 ; Set Data Page = 0
splk #8b4h,PMST ; Use 9K on-chip RAM in program & data space. Microcomputer mode.
lacc #0h ; Load ACC = 1h ( for 1 wait states )
samm CWSR ; Software wait states = 1
samm PDWSR ; Program wait states = 1
lacc #7h ; Load ACC = 4h ( for 4 wait states )
samm IOWSR ; I/O wait states = 4
setc OVM ; Reset overflow mode
clrc SXM ; Set for signed arithmetic operation

**********************************************************************
Input from Digital Ports (52h & 53h)**********************************************************************
lhp #8 ; Set Data Page = 8

Rpt1 : in Ix,PA2 ; Read Ix from port 52h
bit Ix,0 ; Test bit 16
bcnd Rpt1,TC ; If TC=0 repeat input
bit Ix,2 ; Test bit 14
bcnd Rpt1,NTC ; If TC=0 repeat input

Rpt2 : in Iy,PA2 ; Read Iy from port 52h
bit Iy,0 ; Test bit 16
bcnd Rpt2,TC ; If TC=1 repeat input
bit Iy,2 ; Test bit 14
bcnd Rpt2,TC ; If TC=0 repeat input

Rpt3 : in Ex,PA3 ; Read Ex from port 53h
bit Ex,0 ; Test bit 16
bcnd Rpt3,TC ; If TC=0 repeat input
bit Ex,2 ; Test bit 14
bcnd Rpt3,NTC ; If TC=0 repeat input

Rpt4 : in Ey,PA3 ; Read Ey from port 53h
bit Ey,0 ; Test bit 16
bcnd Rpt4,TC ; If TC=1 repeat input
bit Ey,2 ; Test bit 14
bcnd Rpt4,TC ; If TC=0 repeat input

**********************************************************************
Stage I Data Processing**********************************************************************
bit Ix,3 ; Test bit 13 of Ix ( sign )
lacc Ix,16 ; ACC high := Ix
and #0fffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach Ia ; Ia := ACC high = Ix
bit Iy,3 ; Test bit 13 of Iy ( sign )
lacc Iy,16 ; ACC high := Iy
and #0fffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach lb ; lb := ACC high = ly
bit Ex,3 ; Test bit 13 of Ex (sign)
lacc Ex,16 ; ACC high := Ex
and #0fffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach Eac ; Eac := ACC high = Ex
neg ; Negate ACC
sach Eca ; Eca := ACC high = -Ex
bit Ey,3 ; Test bit 13 of Ey (sign)
lacc Ey,16 ; ACC high := Ey
and #0fffh,16 ; Discard control bits
rpt #1 ; REPEAT 2x
sfl ; Shift left 1-bit
xc 1,NTC ; IF TC = 0 THEN
neg ; Negate ACC
sach Ebc ; Ebc := ACC high = Ey
neg ; Negate ACC
sach Ecb ; Ecb := ACC high = -Ey
setc SXm ; Set sign extension mode, SXm := 1
lacc la,16 ; ACC high := la
add lb,16 ; ACC := ACC + ACCB = la + lb
neg ; Negate ACC
sach lc ; lc := ACC high = -(lb + la)
lacc Eac,16 ; ACC high := Eac
add Ecb,16 ; ACC := Eac + Ecb
sach Eab ; Eab := ACC high
neg ; Negate ACC
sach Eba ; Eba := ACC high = Eba

Stage II Data Processing

lt la ; TREG0 := la
mpy Ecb ; PREG := la x Ecb
spl IEacbL ; IEacbL := PREG low
sph IEacbH ; IEacbH := PREG high
lt lb ; TREG0 := lb
mpy Eac ; PREG := lb x Eac
spl IEbacL ; IEbacL := PREG low
sph IEbacH ; IEbacH := PREG high
lt lc ; TREG0 := lc
mpy Eba ; PREG := lc x Eba
spl IEcbaL ; IEcbaL := PREG low
sph IEcbaH ; IEcbaH := PREG high
lt Ecb ; TREG0 := Ecb
mpy Ecb ; PREG := Ecb^2
spl Ecb2L ; Ecb2L := PREG low
sph Ecb2H ; Ecb2H := PREG high
lt Eac ; TREG0 := Eac
mpy Eac ; PREG := Eac\^2
spl Eac2L ; Eac2L := PREG low
sph Eac2H ; Eac2H := PREG high
lt Eba ; TREG0 := Eba
mpy Eba ; PREG := Eba\^2
spl Eba2L ; Eba2L := PREG low
sph Eba2H ; Eba2H := PREG high
lacc IEacbH, 16 ; ACC := IEacbH 00
adds IEacbL ; ACC := IEacbH + IEacbL
adds IEbacL ; ACC := ( IEacbH + IEacbL )
  + ( 00 + IEbacL )
add IEbacH, 16 ; ACC := ( IEacbH + IEacbL )
  + ( IEbacH + IEbacL )
adds IEcbaL ; ACC := ( IEacbH + IEacbL )
  + ( IEbacH + IEbacL )
  + ( 00 + IEcbaL )
add IEcbaH, 16 ; ACC := ( IEacbH + IEacbL )
  + ( IEbacH + IEbacL )
  + ( IEcbaH + IEcbaL )
sach Ax ; Ax := ACC high
abs ; ACC := ABS ( Ax )
sach AAbs ; BAbs := ABS ( Ax )
lacc Ecb2H, 16 ; ACC high := Ecb2H
adds Ecb2L ; ACC := ( Ecb2H + Ecb2L )
adds Eac2L ; ACC := ( Ecb2H + Ecb2L )
  + ( 00 + Eac2L )
add Eac2H, 16 ; ACC := ( Ecb2H + Ecb2L )
  + ( Eac2H + Eac2L )
adds Eba2L ; ACC := ( Ecb2H + Ecb2L )
  + ( Eac2H + Eac2L )
  + ( 00 + Eba2L )
add Eba2H, 16 ; ACC := ( Ecb2H + Ecb2L )
  + ( Eac2H + Eac2L )
  + ( Eba2H + Eba2L )
sach Bx ; Bx := ACC high
abs ; ACC := ABS ( Bx )
sach BAbs ; BAbs := ABS ( Bx )

***************************************************************************** Calculate required compensation currents *****************************************************
sacom  Qx ;  Qx := ACC low
lacc  Qx,16 ;  ACC high := Qx
xc  1,TC ;  IF TC = 1
neg ;  Negate ACC
sach  Zx ;  Zx := ACC high
lt  Zx ;  TREG0 := Zx
mpy  Ebc ;  PREG := Zx x Ebc
pac ;  ACC := PREG
sfl ;  Shift left 1-bit
clrc  SXM ;  Reset sign extension, SXM := 0
rpt  #3 ;  REPEAT 4x
sfr ;  Shift right 1-bit
setc  SXM ;  Set sign extension, SXM := 1
sach  ICa ;  ICa := ACC low (12-bit)
mpy  Eca ;  PREG := Zx x Eca
pac ;  ACC := PREG
sfl ;  Shift left 1-bit
clrc  SXM ;  Reset sign extension, SXM := 0
rpt  #3 ;  REPEAT 4x
sfr ;  Shift right 1-bit
setc  SXM ;  Set sign extension, SXM := 1
sach  ICb ;  ICb := ACC low (12-bit)

----------------------------------- Output to Digital Ports (50H & 51H) -----------------------------------
clrc  SXM ;  Set sign extension, SXM := 1
out  ICa,PA0 ;  Output ICa to port 50h
out  ICb,PA1 ;  Output ICb to port 51h
b  Rpt1 ;  REPEAT from start
REFERENCES


